A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications

Seyed Rasool Hosseini, Mehdi Saberi, and Reza Lotfi

***Abstract*— This brief presents a fast and power-efficient voltage level-shifting circuit capable of converting extremely low levels of input voltages into high output voltage levels. The efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit. Postlayout simulation results of the proposed circuit in a 0.18-μm technology demonstrate a total energy per transition of 157 fJ, a static power dissipation of 0.3 nW, and a propagation delay of 30 ns for input frequency of 1 MHz, low supply voltage level of $V_{\mathrm{DDL}} = 0.4$ V, and high supply voltage level of $V_{\mathrm{DDH}} = 1.8$ V.**

***Index Terms*— Level converter, low power, subthreshold operation, voltage level shifter.**

I. Introduction

One of the most effective ways to reduce dynamic and short-circuit power consumption of digital circuits is lowering the value of the power supply voltage [1]–[3]. On the other hand, reducing the supply voltage increases the propagation delay of the circuits. Moreover, less headroom in analog circuits decreases signal swings and therefore increases the sensitivity to noise. Hence, in moderate-speed mixed-signal circuits or in digital circuits where different parts operate at different speeds, dual-supply architectures are introduced in which a low voltage (i.e., V_{DDL}) is supplied for the blocks on the noncritical paths while a high supply voltage (i.e., V_{DDH}) is applied to the analog and the high-speed digital blocks [2], [3]. In a system with dual supply voltages, level-shifting circuits are needed to convert the lower logic levels into the higher ones to provide correct voltage levels for the next digital blocks. In order to alleviate the degradation of the overall performance of the circuit, the required level shifters must be designed with minimum propagation delay, power consumption, and silicon area. In addition, in order to have more power saving in the low-supply blocks, the employed level shifters must be able to convert the extremely low values of V_{DDL} to even lower than the threshold voltage of the input transistors. Hence, in this brief, a fast and power-efficient voltage level shifter is proposed, which is able to convert extremely low values of the input voltages.

The rest of this brief is organized as follows. In Section II, some of the recently reported high-performance voltage level shifters are reviewed. The proposed circuit is introduced in Section III. Section IV presents the simulation results of the designed circuit verifying the efficiency of the proposed structure. Finally, this brief is concluded in Section V.

II. Literature Survey

One of the conventional level-shifting architectures is shown in Fig. 1(a). The operation of this circuit is as follows. When the input signal *IN* is "$High = V_{\mathrm{DDL}}$," $\mathrm{M_{N1}}$ and $\mathrm{M_{N2}}$ are ON and OFF, respectively. Therefore, $\mathrm{M_{N1}}$ tries to pull the node Q_1 down. Consequently, $\mathrm{M_{P2}}$ is gradually turned on to pull the node Q_2 up to V_{DDH} and to turn $\mathrm{M_{P1}}$ off. Similarly, when the input signal is changed to "$Low = V_{\mathrm{SS}}$," the operation is forced to reverse states. It is noticeable that, in this structure, there is a contention at the nodes Q_1 and Q_2 between the pull-up devices (i.e., $\mathrm{M_{P1}}$ and $\mathrm{M_{P2}}$) driven with V_{DDH} and the pull-down devices (i.e., $\mathrm{M_{N1}}$ and $\mathrm{M_{N2}}$) driven with V_{DDL}. As a result, when the voltage difference between V_{DDL} and V_{DDH} is high and particularly when the input voltage is in subthreshold range, this circuit will no longer be able to convert the voltage levels. This is because the currents of the pull-down transistors are smaller than those of the pull-up devices.

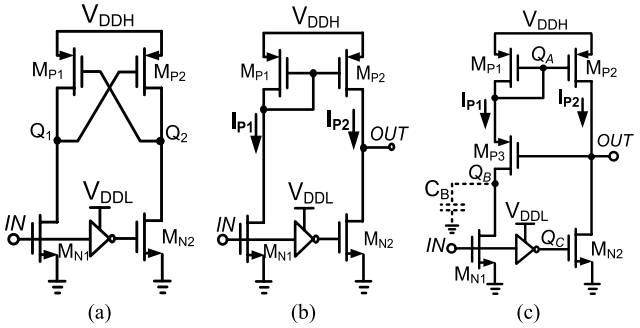

Fig. 1. Schematic of the (a) conventional level shifter, (b) level shifter with a semi-static current mirror, and (c) level shifter with a dynamic current mirror (Wilson current mirror) [5].

To solve this problem, several attempts have been reported. One approach is to exploit technology-based strategies, e.g., employing strong pull-down devices using low-V_{th} transistors and/or weak pull-up networks by using high-V_{th} transistors [4]. Another approach is to use strong pull-down devices by enlarging their width, leading to an increase in both the delay and the power consumption. The last solution is to reduce the strength of the pull-up device when the pull-down device is pulling down the output node [5]–[9]. The structure illustrated in Fig. 1(b) uses a semistatic current mirror to limit the current and therefore the strength of the pull-up device (i.e., $\mathrm{M_{P2}}$) when the pull-down device is pulling down the output node. However, this structure suffers from the static current flowing through $\mathrm{M_{N1}}$ and $\mathrm{M_{P1}}$ during the "*High*" logic levels of the input signal. In order to decrease the static power consumption, a dynamic current generator, which turns on only during the transition times, can be used [5]–[9]. The structure shown in Fig. 1(c) employs a dynamic current generator implemented by $\mathrm{M_{P3}}$ [5]. In this circuit, when the input signal *IN* goes from "*Low*" to "*High*," $\mathrm{M_{N2}}$ turns off and $\mathrm{M_{N1}}$ turns on and pulls the node Q_B down. Since the node *OUT* had been *"Low"* (before the transition), during the time interval in which *OUT* is not corresponding to the logic level of the input signal *IN*, $\mathrm{M_{P3}}$ will be turned on. Therefore, a transition current flows through $\mathrm{M_{N1}}$, $\mathrm{M_{P3}}$, and $\mathrm{M_{P1}}$. This current is mirrored to $\mathrm{M_{P2}}$ (i.e., I_{P2}) leading to pull the node *OUT* up. Finally, when *OUT* is pulled up to V_{DDH}, $\mathrm{M_{P3}}$ is turned off and therefore no static current flows through $\mathrm{M_{N1}}$, $\mathrm{M_{P3}}$, and $\mathrm{M_{P1}}$. On the other hand, when the input signal *IN* is changed

Manuscript received January 9, 2016; revised April 26, 2016 and July 14, 2016; accepted August 23, 2016.

S. R. Hosseini and M. Saberi are with the Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad 9177948974, Iran (e-mail: seyedrasool.hosseini@stu-mail.um.ac.ir; msaberi@um.ac.ir).

R. Lotfi is with the Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad 9177948974, Iran, and also with the Electronics Research Laboratory, Department of Microelectronics, Delft University of Technology, 2628 Delft, The Netherlands (e-mail: rlotfi@ieee.org).

Digital Object Identifier 10.1109/TVLSI.2016.2604377

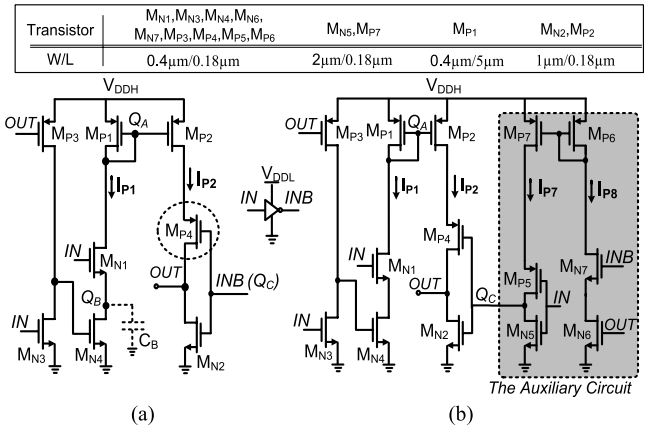

Fig. 2. (a) Principle of the proposed level shifter. (b) Schematic of the proposed level shifter.

from "*High*" to "*Low*," M_{N1} turns off and M_{N2} turns on trying to pull the node *OUT* down. As the node *OUT* is gradually pulled down, M_{P3} is turned on trying to charge the node Q_B, which is already discharged to the ground, meaning that a transition current (i.e., I_{P1}) flows through M_{P1} and M_{P3} to charge node Q_B. This current is mirrored to M_{P2} (i.e., I_{P2}) and therefore tries to pull the node *OUT* up, while M_{N2} is trying to pull this node down. This means that there is still a contention between the pull-up and the pull-down devices in the high-to-low transition of the input signal, leading to increase in the delay and consequently the power consumption of the circuit, especially the power of the next stage.

III. Proposed Voltage Level Shifter

In order to reduce the existing contention at the high-to-low transition of the structure shown in Fig. 1(c), the transition current of I_{P1} and therefore I_{P2} must be suppressed when M_{N2} is pulling down the output node. For this purpose, the structure shown in Fig. 2 is proposed. The operation of the proposed circuit, shown in Fig. 2(a), is as follows. When the input signal changes from "*Low*" to "*High*," M_{N1} is turned on and M_{N4} is turned off. During the transition time in which *OUT* is not corresponding to the logic level of the input, M_{N4} will be turned on, because the overdrive voltage of M_{P3} (i.e., V_{DDH}) is larger than that of M_{N3} (i.e., V_{DDL}). Therefore, a transition current flows through M_{N4}, M_{N1}, and M_{P1} (i.e., I_{P1}). This current is mirrored into M_{P2} (i.e., I_{P2}) and tries to pull up the output node. Finally, when *OUT* is pulled up, M_{P3} is turned off and consequently the gate of M_{N4} is pulled down by M_{N3} meaning that no static current flows through M_{N4}, M_{N1}, and M_{P1}. It should be noted that in order to minimize the power consumption, the aspect ratio of M_{P1} is chosen smaller than that of M_{P2}. As for the high-to-low transition of the input signal, M_{N2} is turned on trying to pull down the output node. At the same time, M_{N1} is turned off meaning that, in contrast to the structure shown in Fig. 1(c), roughly no transition current flows through M_{P1} (i.e., $I_{P1} \approx 0$) reducing the strength of M_{P2} when M_{N2} is pulling down the output node. However, it should be noted that the node Q_A is pulled up just to $V_{DDH} - |V_{th}|$, where V_{th} is the threshold voltage of M_{P1}. This means that the current of M_{P2} (i.e., I_{P2}) is not completely close to zero and consequently a weak contention still exists.

In order to further reduce the value of I_{P2}, another device, i.e., M_{P4} in Fig. 2(a) is used. For more details, when M_{N2} is pulling down the output node, the gate of M_{P4} is "*High*" with the value of V_{DDL} and therefore the drain–source voltage of M_{P2} is decreased. As a result, as shown in Fig. 3, the propagation delay and therefore the

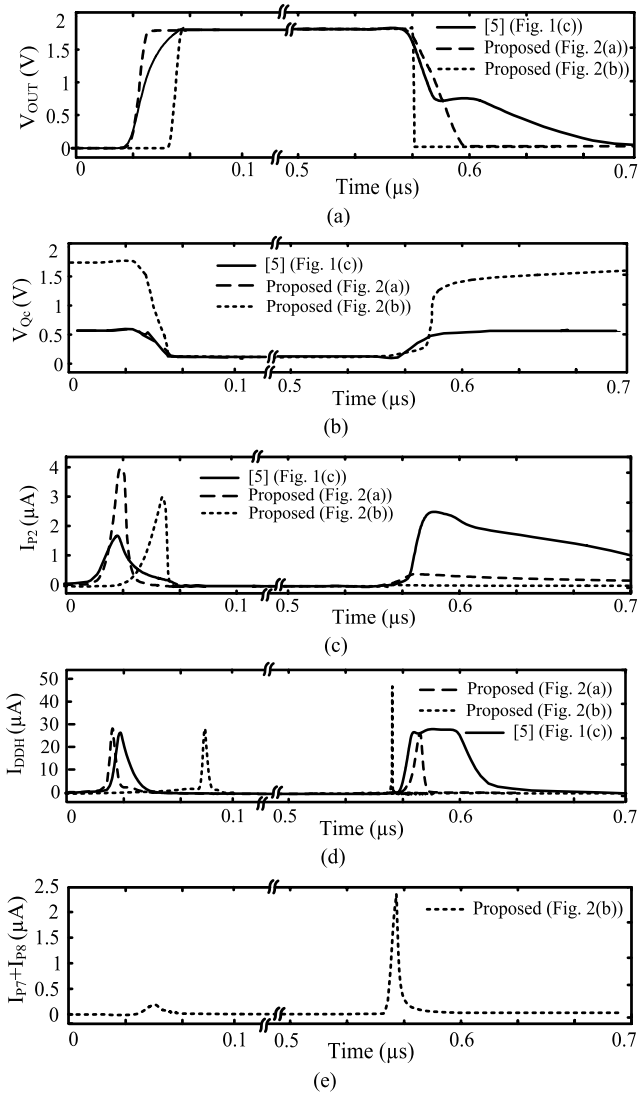

Fig. 3. Simulated waveforms of the level-shifter structures for low-to-high and high-to-low transitions of the input signal. (a) Voltage of the output node (i.e., V_{OUT}). (b) Voltage of the node Q_C. (c) Current of the output branch (i.e., IP2). (d) Entire current of the level shifter supplied by V_{DDH} (i.e., I_{DDH}). (e) Current of the auxiliary circuit (i.e., $I_{P7}+I_{P8}$) of the proposed structure. The values of V_{DDH} and V_{DDL} are 1.8 V and 0.4 V, respectively. An inverter is also added as a load circuit ($C_L \approx 2.5$ fF) to all the structures.

power dissipation of the circuit will be decreased. It should be noted that if the gates of M_{N2} and M_{P4} are driven with a voltage higher than V_{DDL}, not only the current of the pull-up device (i.e., I_{P2}) is drastically reduced, but also the strength of the pull-down device (i.e., M_{N2}) is increased. Thus, the contention and therefore the delay and the power (especially the power consumption of the next stage) are significantly reduced. Moreover, the level shifter will be able to operate correctly even for subthreshold input voltages. In order to apply this technique to the proposed structure, as shown in Fig. 2(b), an auxiliary circuit (i.e., M_{P5}, M_{P6}, M_{P7}, M_{N5}, M_{N6}, and M_{N7}) is used. This auxiliary circuit turns on only in the high-to-low transition of the input signal to pull up the node Q_C to a value larger than V_{DDL}. The operation of this part of the circuit is as follows. When *IN* changes from "*High*" to "*Low*" and *OUT* is not still corresponding to the input logic level, M_{N6}, M_{N7}, and M_{P6} are turned on and M_{N5} is turned off. Therefore, a transition current flows through M_{N6}, M_{N7}, M_{P6}, and mirrors to M_{P7} (i.e., I_{P7}) pulling up the node Q_C.

This means that M_{P4} is turned off and M_{N2} is turned on with a voltage higher than V_{DDL}, as shown in Fig. 3(b), leading to a significant reduction in the aforementioned contention. Finally, when *OUT* is pulled down, M_{N6} is turned off and consequently no current flows through M_{N6}, M_{N7}, and M_{P6} meaning that the auxiliary circuit is turned on only during the high-to-low transition of the input signal, as shown in Fig. 3(e). It should be noted that since it is not needed to charge Q_C up to the exact value of V_{DDH}, the auxiliary circuit is designed such that the current flowing through M_{P7} (i.e., I_{P7}) is very small. This means that the existing contention in this branch will be negligible, reducing the propagation delay and the power consumption of the auxiliary circuit. As a result, using the auxiliary circuit, as shown in Fig. 3(c), the power consumption of the main circuit including the output load circuit (an inverter is added as a load circuit to all the structures) is considerably decreased such that the entire power consumption of the proposed structure is only about 30% of that of the structure without the auxiliary circuit (see Fig. 2(a)). It can be concluded that the efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit.

Finally, in order to reduce the short-circuit power of the required inverter (i.e., M_{P3} and M_{N3}), instead of the output signal, the input is used to drive the gate of M_{N3}. In other words, in the conventional inverter, both low-to-high and high-to-low short-circuit currents exist whereas in the proposed structure, only a small current at the low-to-high transition exists. Moreover, this current is reduced due to the fact that the gate of M_{N3} is driven by V_{DDL} not V_{DDH}.

IV. Simulation Results

In order to verify the performance of the proposed voltage level shifter, the proposed structure (see Fig. 2(b)) and also some other state-of-the-art works have been simulated in a standard TSMC 0.18-μm 1P6M CMOS technology. Targeting the minimum power-delay-product (PDP), all the circuits have been optimally designed to be functional in all process, voltage, and temperature (PVT) corners for $V_{DDL} = 0.4$ V, $V_{DDH} = 1.8$ V, and the input frequency of $f_{in} = 1$ MHz. In the proposed circuit, the transition current of I_{P2} (in Fig. 2) must be large enough to reduce the propagation delay of the low-to-high transition of the output voltage. On the other hand, the power consumption of the branch of M_{P1}, M_{N1}, and M_{N4} should be minimized. Therefore, the current mirror ratio (i.e., $(W/L)_{P2}/(W/L)_{P1}$) should be large. For this purpose, the length of M_{P1} has been selected to be 5 μm, whereas the lengths of the other devices are all chosen of minimum size (i.e., 0.18 μm). Moreover, the width of M_{P2} is also selected to be 1 μm. In addition, since M_{N2} is driven by a voltage lower than V_{DDH}, it must be somewhat strong to be able to pull the output node down. Hence, the width of this transistor is chosen to be 1 μm, while the widths of the other transistors are of minimum size (i.e., 0.4 μm). It is worth noting that not only the auxiliary circuit in Fig. 2, but also all the other structures, especially the one reproduced from [5] and shown in Fig. 4(a), are also designed using the same strategy.

In order to have a fair comparison between the structures, a unit buffer and an inverter are added as the load circuit and input buffer, respectively, to all the structures and the calculated power dissipation includes the power consumption of these buffers. The transistors' sizes used for the performance comparison are shown in Fig. 4. The transistor' sizes of the proposed circuit are shown in Fig. 2. Moreover, Fig. 5 shows the layout of all the structures. The following results are related to the postlayout simulations.

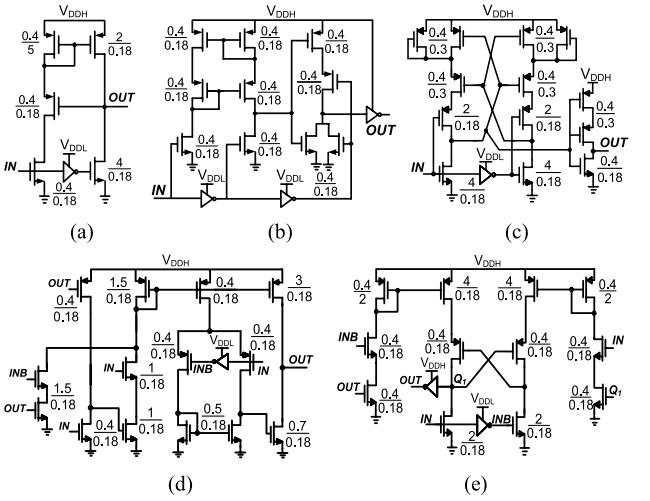

Fig. 4. Schematics and the transistor sizes of the structures presented in (a) [5], (b) [6], (c) [7], (d) [8], and (e) [9].

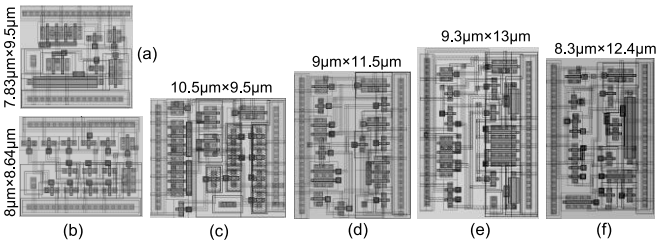

Fig. 5. Layout of the structures presented in (a) [5], (b) [6], (c) [7], (d) [8], (e) [9], and (f) the proposed circuit.

TABLE I
Simulation Results of the Proposed Circuit ($V_{DDH} = 1.8$ V)

Frequency	$V_{DDL,min}$ (V)	Power (μW)	Delay (ns)
5 MHz	0.38	0.98	45
10 MHz	0.41	1.68	24.3
20 MHz	0.44	2.77	13.65
50 MHz	0.49	5.72	5.81
100 MHz	0.54	10.2	2.86
200 MHz	0.6	17.66	1.46
500 MHz	0.72	47	0.63
1 GHz	0.9	95	0.34

In the proposed structure, the typical PVT corner involves typical-nMOS and pMOS transistors, a high supply voltage of $V_{DDH} = 1.8$ V, and a temperature of 25 °C. Moreover, slow-nMOS, fast-pMOS, $V_{DDH} = 1.8\% + 10\% = 1.98$ V, and a temperature of 0 °C were chosen as the worst corner. This is due to the fact that a larger difference between V_{DDL} and V_{DDH} as well as fast-pMOS and slow-nMOS increase the mentioned contention between the pull-up and the pull-down devices. In addition, in the subthreshold region, a lower temperature results in a smaller current for the devices leading to increase the propagation delay. On the other hand, for the best corner, simulations show that the minimum delay occurred for fast-nMOS, fast-pMOS, $V_{DDH} = 1.8\%–10\% = 1.62$ V, and a temperature of 120 °C. Fig. 6 shows the simulation results of the delay and the power dissipation of the proposed level shifter versus the value of V_{DDL}, for the typical, worst, and best PVT corners. It can be observed that the circuit works correctly at all the PVT corners for an input frequency of 1 MHz.

TABLE II
COMPARATIVE SIMULATION RESULTS (TECHNOLOGY: 180 nm, $V_{DDH} = 1.8$ V, $f_{in} = 1$ MHz, $C_L \approx 2.5$ fF)
(TECHNOLOGY: 90 nm, $V_{DDH} = 1.2$ V, $f_{in} = 1$ MHz, $C_L \approx 0.5$ fF)

		TCAS-II'10 [5]		TCAS-I'14 [6]		TVLSI'14 [7]		JSSC'12 [8]		TCAS-II'14 [9]		This work	
Technology		180 nm	90 nm	180 nm	90 nm	180 nm	90 nm	180 nm	90 nm	180 nm	90 nm	180 nm	90 nm
$V_{DDL,min}$ (V)		0.4	0.12	0.37	0.11	0.38	0.16	0.37	0.11	0.36	0.12	0.36	0.12
V_{DDL}=0.4V @ 180-nm	Delay (ns)	61	17	36	7.4	54	15	35	6	31	11	30	7
	Static Power (nW)	0.98	0.07	0.18	0.14	0.22	0.1	0.13	0.12	0.13	0.06	0.20	0.13
V_{DDL}=0.2V @ 90-nm	Total Power (nW)	2654	214	584	224	290	214	320	492	327	204	159	135
	PDP (nW.ns)	161894	3638	21024	1657	15660	3210	11200	2952	10137	2244	4770	954
Area (μm^2)		69.12	----	74.38	----	99.75	----	103.5	----	120.9	----	103	----

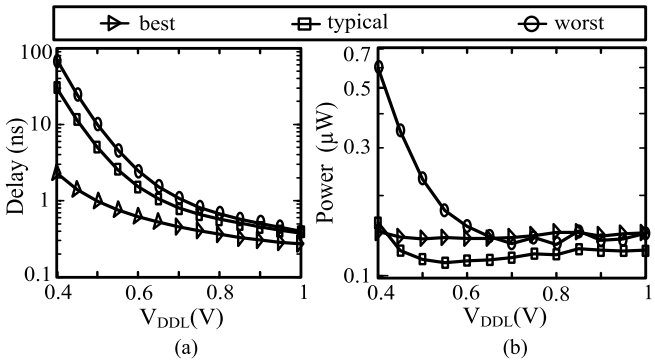

Fig. 6. Simulated values of (a) the delay and (b) the total power of the proposed level shifter for different values of V_{DDL}. The value of V_{DDH} and the input signal frequency are 1.8 V and 1 MHz, respectively.

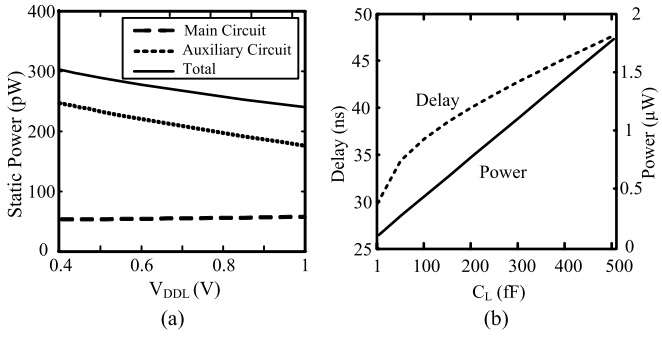

Fig. 7. (a) Simulated values of the static power dissipation of the proposed level shifter as a function of V_{DDL} when $V_{DDH} = 1.8$ V. (b) Total power dissipation and delay of the proposed structure versus the size of the capacitive load ($V_{DDL} = 0.4$ V, $V_{DDH} = 1.8$ V, and $f_{in} = 1$ MHz).

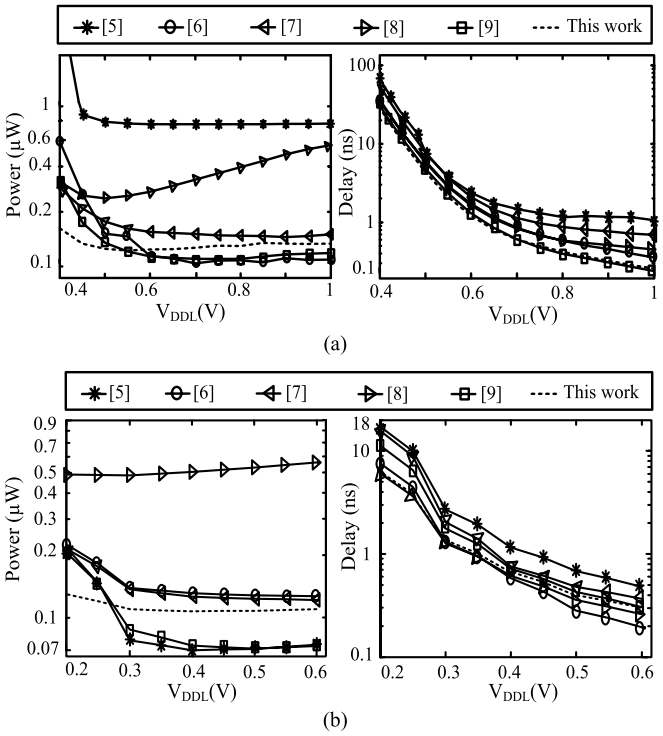

Fig. 8. Simulated values of the total power dissipation and delay of the level-shifter structures as a function of V_{DDL} in (a) 0.18-μm CMOS with $V_{DDH} = 1.8$ V and (b) 90-nm CMOS with $V_{DDH} = 1.2$ V. The input frequency is 1 MHz.

To study how the process and temperature variations as well as the mismatch between the devices affect the operation of the proposed circuit, a 1000-point Monte-Carlo simulation has been performed. The normalized standard deviation values (σ/μ) of the delay and power dissipation are 0.56 and 0.32, respectively.

In order to study the main contributor of the static current in the proposed circuit, consider the situation in which the input is "High." Since M_{N7} is OFF, the gates of M_{P6} and M_{P7} are pulled up until the value of $V_{DDH} - |V_{th}|$. Therefore, a static subthreshold current (the main contributor of the static current) flows through M_{P7}, M_{P5}, and M_{N5}. It should be noted that as V_{DDL} (the driven voltage of the gates of M_{P5} and M_{N5}) increases, the drain–source voltage of M_{P7} is decreased leading to a smaller current in M_{P7} and therefore a smaller static current. Fig. 7(a) compares the static power consumed by the auxiliary circuit with the main part of the circuit. It can be observed that the major part of the overall static power is consumed by the auxiliary circuit. Moreover, Fig. 7(b) shows the power consumption and the propagation delay of the proposed circuit as a function of the size of the capacitive load (i.e., C_L). As expected, the power and the delay are increased linearly with the size of the capacitive load.

Simulation results of the proposed circuit for different values of the input frequency are shown in Table I. It can be observed that with the reduction of V_{DDL}, the maximum operating frequency of

the circuit is decreased. The minimum values of V_{DDL} for which the circuit operates correctly at 100 MHz and 1 GHz are 0.54 V and 0.9 V, respectively.

In order to compare the performance of the proposed level shifter with other works, Fig. 8(a) shows the simulated values of the power dissipation and the delay of the proposed structure and the circuits presented in [5]–[9] for different values of V_{DDL}. All the structures were simulated under the same conditions at the typical PVT corner with $V_{\mathrm{DDH}} = 1.8$ V in a 0.18-μm CMOS technology. Furthermore, in order to investigate the benefits of technology scaling on the performance, all the circuits have been optimally designed and simulated in a standard TSMC 90-nm CMOS technology as well. Fig. 8(b) illustrates the simulated values of the delay and the power consumption of the circuits. From Fig. 8(a) and (b), it can be observed that, in the subthreshold region, the proposed circuit exhibits superior performance, especially from the power dissipation viewpoint. This is due to the fact that, in the proposed structure, the strength of the pull-up device is drastically reduced when the pull-down device is pulling down the output node. Finally, Table II summarizes the performance of the structures using the simulation results under the same conditions. In order to have a better comparison between the structures, the well-known PDP can be used as a figure of merit. It is clear that the proposed voltage level shifter presents the lowest PDP compared with the other counterparts.

V. Conclusion

In this brief, a fast and low-power voltage level-shifting architecture was proposed which is able to convert extremely low-input voltages. The efficiency of the proposed circuit is due to the fact that not only the current of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased. Postlayout simulation results verified the efficiency of the proposed circuit compared with other works, especially from the power consumption viewpoint.

References

[1] A. Wang and A. P. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[2] K. Usami *et al.*, "Automated low-power technique exploiting multiple supply voltages applied to a media processor," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 463–472, Mar. 1998.

[3] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for medical implant devices," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.

[4] P. Corsonello, S. Perri, and F. Frustaci, "Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology," in *Proc. IEEE Int. Conf. Comput. Design (ICCD)*, Oct. 2015, pp. 499–504.

[5] S. Lütkemeier and U. Ruckert, "A subthreshold to above-threshold level shifter comprising a Wilson current mirror," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 9, pp. 721–724, Sep. 2010.

[6] S.-C. Luo, C.-J. Huang, and Y.-H. Chu, "A wide-range level shifter using a modified Wilson current mirror hybrid buffer," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1656–1665, May 2014.

[7] M. Lanuzza, P. Corsonello, and S. Perri, "Fast and wide range voltage conversion in multisupply voltage designs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 2, pp. 388–391, Feb. 2015.

[8] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1776–1783, Jul. 2012.

[9] S. R. Hosseini, M. Saberi, and R. Lotfi, "A low-power subthreshold to above-threshold voltage level shifter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 10, pp. 753–757, Oct. 2014.