This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2016.2644721, IEEE Transactions on Device and Materials Reliability

Ultra-Low Power, Highly Reliable, and Nonvolatile Hybrid MTJ/CMOS Based Full-Adder for Future VLSI Design

Ramin Rajaei[1], Sina Bakhtavari Mamaghani

Department of Electrical Engineering, Shahid Beheshti University, Velenjak, Tehran, IRAN
{r_rajaei@, s.bakhtavari@mail.}sbu.ac.ir

Abstract

Very large-scale integrated circuit (VLSI) design, based on today's CMOS technologies, are facing various challenges. Shrinking transistor dimensions, reduction in threshold voltage, and lowering power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design challenges, hybrid MTJ/CMOS based design can resolve the issue of leakage power and bring the advantage of nonvolatility. However, radiation-induced soft error is still an issue in such new designs as they need peripheral CMOS components. As a result, these magnetic-based circuits are still susceptive to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Comparing with the previous work, the proposed MFA is capable of tolerating any particle strike regardless of the induced charge. Besides, our MFA circuit offers a lower energy consumption in write operation as compared with previous counterparts. We also suggest an incremental modification to the proposed MFA circuit to give it the advantage of full nonvolatility for future nonvolatile microprocessors.

Keywords: *Magnetic tunnel junction (MTJ), magnetic full adder (MFA), single event upset (SEU), Reliability.*

1- Introduction and Background

Along with the decrease in CMOS dimension as well as supply voltage, sensitivity to radiation effects is increasing [1-2]. Moreover, further challenges such as process variation and leakage power are becoming more and more concerning [2-4]. Decrease in threshold voltage results in leakage power increase [5-8]. When an energetic particle strikes an off-state transistor in an SRAM cell, it could alter the stored logic value. This soft error is called single event upset (SEU) [1-2]. SEU is a soft error for sequential logic and can take place more easily due to the CMOS scaling down [2, 8]. Magnetic-based logics can be an alternative choice for dealing with the mentioned challenges of the CMOS logics [4].

Magnetic tunnel junction (MTJ) is the basic element of magnetic memories and logics. MTJ is comprised of three layers including an ultra-thin oxide barrier (e.g. MgO [9]) as the mid-layer and two ferromagnetic (FM) layers in top and bottom (Fig.1). There are two possible modes for the MTJs; first, the parallel mode that refers to the case which both of the FM layers have an identical magnetic direction. And the second, the antiparallel mode that refers to the case which the FM layers are in opposite magnetic directions [6-9]. When an MTJ is in a parallel mode, it shows a lower resistance (denoted by R_P) than the case it has an antiparallel mode (with a resistance of R_{AP}) [8-9]. The difference between these two applied resistances is called tunnel magnetoresistance (TMR) ratio and is given by (1).

$$TMR = \frac{R_{AP} - R_P}{R_P} \times 100 \quad (1)$$

Higher difference between R_{AP} and R_A results in higher TMR ratio and gives a more readability and read stability [8-9]. It is notable that, for the current MgO-based MTJs, a TMR ratio of 600% (and higher) is obtained [10] at room temperature.

To configure MTJs, there are various writing techniques that the Spin Transfer Torque (STT) [5] is the most promising technique offering high power efficiency and fast writing speed [8-9]. Fig.2 shows a simple MTJ-based latch circuit and includes an STT-writing circuitry [9].

Hybrid MTJ/CMOS memory and logic design offers some distinguished features such as very low power consumption, nonvolatility, high endurance, and an easy 3D integration with CMOS technology [6-9]. Heretofore, a number of MTJ/CMOS-based logic and memory circuits are suggested in the literature [11-17]. In [11], a magnetic latch (mlatch) (shown in Fig.2) is proposed. This circuit includes a CMOS

[1] Corresponding author (r_rajaei@sbu.ac.ir)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2016.2644721, IEEE Transactions on Device and Materials Reliability

sequential logic for reading the state of MTJs (the sense amplifier), a CMOS combinational logic for reconfiguring the MTJs (the write circuit) and also two MTJ cells. The proposed mlatch circuit offers lower power consumption and also nonvolatility in comparison with the CMOS latches [16]. However, the proposed mlatch is susceptive to radiation-induced SEUs. In [12], another mlatch robust against radiation is proposed. This mlatch uses four MTJs instead of two and therefore, suffers from a high energy consumption for write operation. As discussed in [13-14], at least 90% of total energy consumption in magnetic-based memory/logic circuits is used for the write operation to reconfigure the MTJs. Other radiation hardened (rad-hard) mlatches are proposed in [13-14]. In [15-16], simple unprotected magnetic flip-flops (MFF) are proposed. In [17], a rad-hard version of MFF offering an SEU-tolerance capability in addition to the advantages of MFFs suggested in [15-16] is proposed. Magnetic full-adder (MFA) circuits are also suggested in literature [6-7]. The proposed MFA circuits offer an almost zero leakage current in standby mode. However, as we show in section II, these MFA circuits cannot guarantee a fault free operation in the presence of radiation effects. This paper proposes a rad-hard MFA (the so-called RH-MFA) that is capable of toleration particle strikes with any amount of energy level. Over the previous work, the proposed RH-MFA uses only one reconfigurable MTJ and consumes a lower write-energy. We also, suggested a serial rad-hard and also a full-nonvolatile rad-hard MFA based on the proposed RH-MFA.

The rest of this paper is organized as follows. The second section discusses the radiation effects on the previous MFA circuits. The third section proposes a rad-hard MFA circuit (RH-MFA). The fourth section proposes a serial and also a full-nonvolatile rad-hard MFAs based on the RH-MFA. The fifth section reports and discusses the simulation results. And, the last section concludes the paper.

2- Radiation Effects on Previous MFAs

Fig.3 shows a previous MFA circuit proposed in [7]. This circuit includes two sub-circuits for summation (SUM) and output Carry (Co). Each sub-circuit is comprised of three CMOS components in addition of two MTJ cells. The sense amplifier (SA) circuit is for read operation. This circuit senses the configuration and associated resistance of the MTJs and results SUM/Co outputs (and also their complements) based on them. This circuit is a sequential logic and hence, suffers from SEUs caused by radiation [2-3, 8]. The other CMOS components are combinational logic and there is no SEU concern for them [8]. It has been shown that, the current induced by particle strikes cannot change the configuration of MTJs [13] and therefore, the MTJ cells are assumed as radiation tolerant [14]. As mentioned earlier, the previous MFA circuits [6-7] suffers from radiation-induced soft errors due to their CMOS read component. To show this issue, we simulated the circuit proposed recently in [7] (shown in Fig.3). All the simulations in this paper are performed based on the simulation setup detailed in section 5-A.

Fig.4 shows the results obtained after SEU injection at output nodes of the MFA circuit proposed in [7]. As shown in this figure, when the clock signal (CLK) is high and the MFA circuit is in evaluate phase, an energetic particle strike in the SA circuits, could alter the associated output to an incorrect state. The structure of other considered MFAs is similar to the one shown in Fig.3; and therefore, they are susceptive to SEUs as well. As expressed earlier, this paper proposes a rad-hard MFA that is capable of tolerating particle strikes with any amount of charge. Next section introduces our proposed rad-hard MFA and describes how it works as a full-adder. The functionality of the FA shown in Fig.3 can be easily understood after that explanation.

3- Proposed Rad-Hard MFA (RH-MFA)

Fig.5 shows our proposed rad-hard MFA (RH-MFA) circuit including two sub-circuits for SUM and output Carry (Co). Similar to other magnetic logic circuits [11-17], this circuit is composed of three components including a CMOS sense amplifier (SA) circuit, a CMOS logic tree (LT), and a nonvolatile MTJ component with a peripheral CMOS write circuit (for reconfiguration of the MTJs). As aforementioned, among the mentioned CMOS components, the sequential SA circuit is vulnerable to be affected by radiation effects [8, 12-14,17].

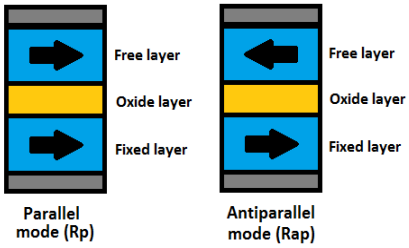

Fig.1. MTJ structure in two modes of parallel and antiparallel

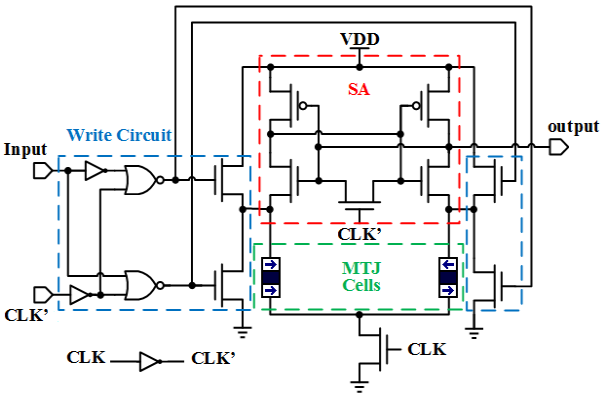

Fig.2. Unprotected magnetic latch: a complete circuit with the all CMOS and MTJ components

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2016.2644721, IEEE Transactions on Device and Materials Reliability

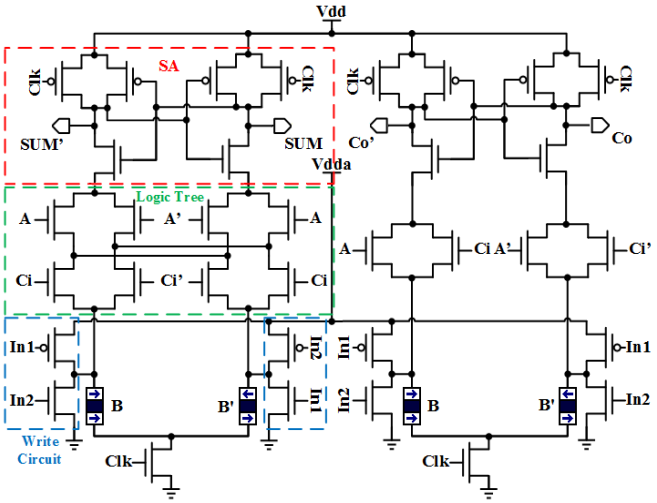

Fig.3. MFA circuit proposed in [7]

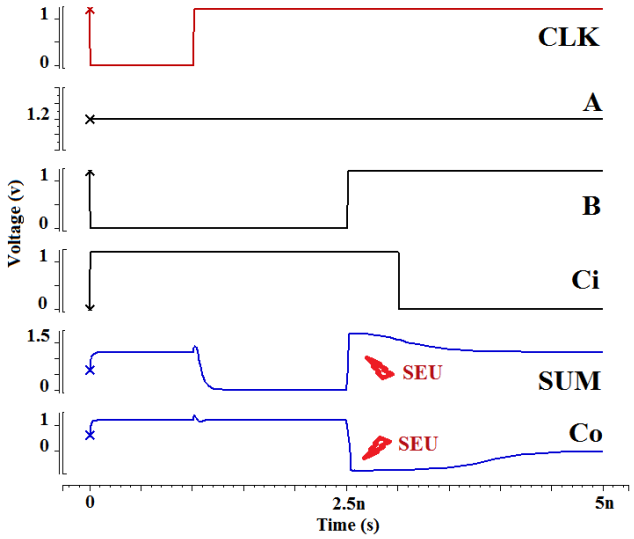

Fig.4. the results associated with SEU injection to MFA proposed in [7]

Instead of the 6-transistor susceptive SA circuit employed in Fig.3, we used a rad-hard SA circuit including 12 transistors to obtain SEU tolerance. Also, instead of two reconfigurable MTJs per each sub-circuit (totally 4 MTJs for a 1-bit FA), we used one configurable MTJ (the so-called free MTJ) along with a fixed one (the reference MTJ) for both the SUM and Co sub-circuits.

In other words, we decreased the number of configurable MTJs from 4 to only 1 in a 1-bit full-adder circuit to obtain a considerable energy efficiency.

The resistance of the configurable MTJ (the free MTJ) could be changed using the employed write circuit while the reference MTJ always has a fixed resistance. In order to obtain the highest TMR ratio, we set the resistance of the reference MTJ to $(R_{AP+} R_P)/2$ [18]. A TMR ratio of 600% for the MgO-MTJs is obtained in [10]. Therefore, such assumption of a free and a reference MTJ instead of two free MTJs is reliable enough. As noted before, the dominant factor of total power consumption in MTJ-based circuits is what that is needed for reconfiguring the MTJs. Therefore, fewer MTJ usage offered by our RH-MFA (from four to one), can result in a great decrease in power consumption.

The proposed RH-MFA, is a three-input (A, B, and Ci) and two-output (SUM and Co) circuit. To deal with leakage current, there is an MTJ in every path from the supply voltage (V_{dd}) to the ground (GND). Also, in order to lower the power consumption of the suggested MFA, a low-cost write circuit has been included that uses only 6 transistors instead of 16 transistors used in previous write circuits [6-7,15].

In the structure of proposed circuit shown in Fig.5, inputs A and Ci go to the related transistors and input B is saved in the free MTJ cell. Parallel mode of MTJ (with R_P) represents a logic value of '1' and antiparallel mode (with R_{AP}) represents '0' [19]. To result the logic function, the proposed SA circuit provides a reliable, power efficient and also high-speed read operation. Table 1 shows the truth table of outputs SUM and Co based on inputs A, B, and Ci.

Table 1: The truth table of outputs SUM and Co

A	B	Ci	SUM	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

As can be found from the truth table, Co is a majority function of the inputs (denoted by Eq. 2). When inputs A and Ci are both the same, Co does not depend on input B. For example, if both A and Ci are '1' (in the evaluation phase), the LT of right branch in the output Carry circuit will construct the pull-down path and causes Co′ to go down. When inputs A and Ci disagree, both branches of the LT circuit will being connected and based on the free MTJ configuration, the pull-down path will be constructed and the related output will be provided. As another example, when A and Ci are not the same and input B is '1', Co must be '1'. In this case, the free MTJ will demonstrate a path with lower resistance than the reference MTJ. Therefore, the applied resistance in the left branch becomes smaller than the one at the right side resulting to constructing the pull-down path in the left side. As a result, output Co′ goes '0' and Co stays at '1'. To understand how the sub-circuit of SUM works, we should consider Eq.3 for SUM.

$$Co = AB + AC_i + BC_i \quad (2)$$

$$SUM = A \oplus B \oplus C_i = ABC_i + AB'C_i' + A'BC_i' + A'B'C_i \quad (3)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2016.2644721, IEEE Transactions on Device and Materials Reliability

The functionality of the SUM-circuit can be understood easily by tracking the LT's path considering the configuration of the free MTJ. By the rise of the CLK signal, one of the paths will demonstrate a lower resistance regarding this configuration; so its corresponding node will be pulled down and the proper output will be provided. For example, consider the case which A and Ci are respectively '1' and '0' and a value of '1' is stored by the MTJ for input B. The parallel configuration of the MTJ will create a path with lower resistance in the left branch of LT, resulting the pull down of node SX6 and causing the output of '0' for the SUM's value. On the contrary, node SX5 will have no established path to ground and it will be pulled-up by V_{dd} that results in a high logic value for SUM′.

The normal functionality of proposed MFA is shown in Fig.6. It is clear that the function of MFA completely follows the truth table mentioned in table.1. When the CLK signal is at logic '0', nodes X1 to X4 and SX1 to SX4 will be pulled up by P1 to P8 transistors. In this case, the circuit is in pre-charge mode and we can reconfigure the free MTJ using the write circuit as desired. By the rise of the CLK signal, the SA circuits will go to the evaluation mode and proper outputs will be available at the outputs. Considering the schematic of the proposed MFA circuit, it can be understood that both the SA circuits are symmetrical; meaning that nodes X1 and X2 will have the same behavior with nodes X3 and X4. As nodes of the SA circuit related to the other sub-circuit are also the same, we only included nodes X1, X3, SX1, and SX3 in the simulation figures to have a more clarified figures.

As mentioned above, nodes X1 to X4 and SX1 to SX4 will be pulled up strongly by the supply source in the pre-charge mode. In the other case, which clock signal is at a logic value of '1', each node of SA circuits has a dual node with the same behavior. When an energetic particle strikes one of the nodes, it will deposit some charge at the struck region and cause a logic flip. However, due to circuit's behavior, this logic flip will cause a floated state at the node and the correct value will be restored by the other nodes. This case has been investigated in section-V and simulation figures have been included.

4- Incremented Rad-Hard MFA Circuits

A. A rad-hard and low power serial magnetic binary adder based on the proposed RH-MFA (SRH-MBA)

A serial binary adder is a digital circuit that performs binary addition in continuous clock signals. As shown in Fig.7, this circuit employs a full-adder as well as a flip-flop [20]. The full-adder has two direct inputs and a carry-in bit that is the previous calculated carry-out output. This circuit provides two output bits as the SUM and carry-out bits by adding inputs A and B (Fig.7), in a clock cycle.

The conventional serial binary adder (shown in Fig.7) suffers from radiation-induced SEUs in the employed flip-flop. This circuit also has a high power consumption due to its data storage method. We employed our proposed RH-MFA circuit to design a serial and rad-hard magnetic adder circuit (shown in Fig.8). Our proposed serial magnetic binary adder uses only two reconfigurable MTJs to save the resulted carry-out (Co) output as the next carry-in (Ci) input.

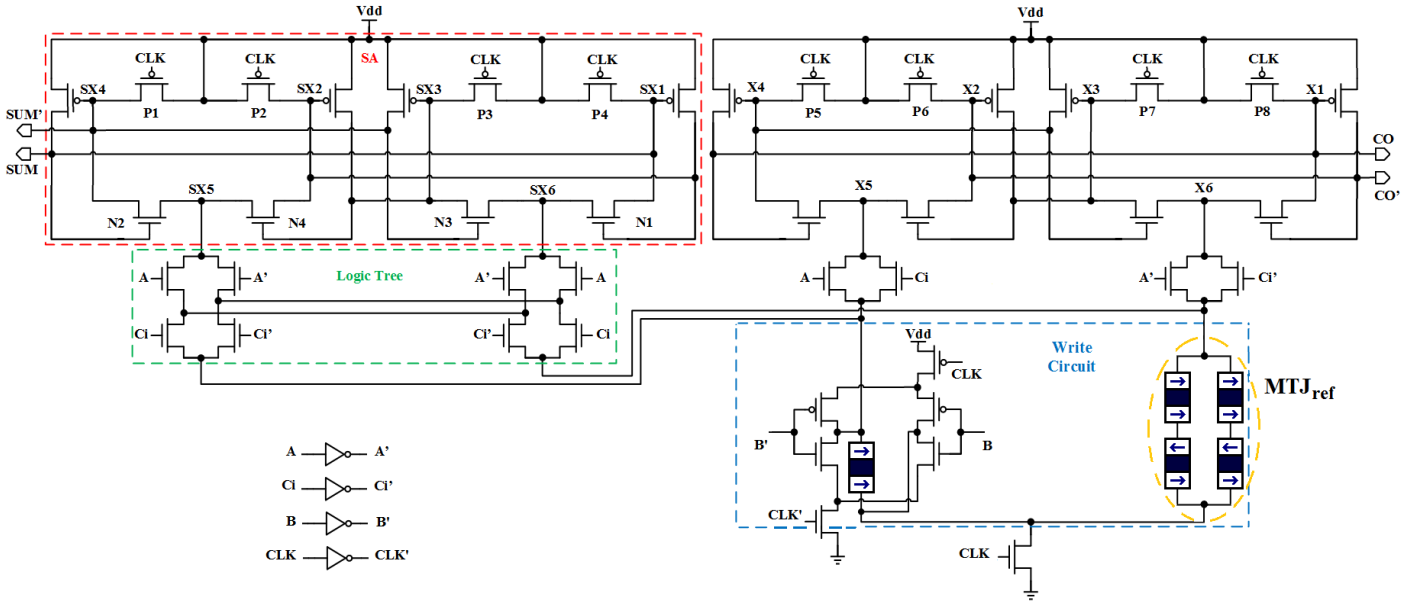

Fig.5. Proposed rad-hard MFA (RH-MFA) circuit

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2016.2644721, IEEE Transactions on Device and Materials Reliability

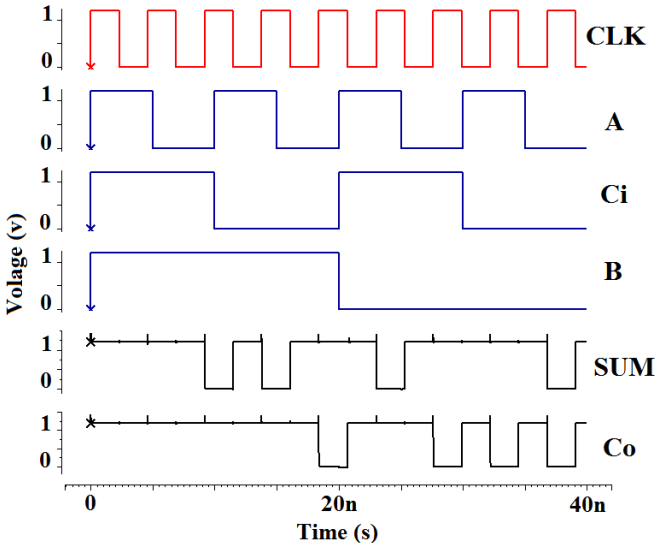

Fig.6. Normal functionality of the proposed RH-MFA

MTJs are inherently robust against particle strikes. Also, our sense amplifier circuit is radiation hardened. Therefore, the proposed serial magnetic binary adder is robust against SEUs. Also, due to the presence of MTJs in all the paths between the supply voltage and the ground, the issue of leakage current is not concerning. In this circuit, the saved value in each clock signal pulse as the carry-in (Ci), will be restored in by the SA circuit at the next clock rise. In fact, when the clock signal is high, one of the reconfigurable MTJs employed (M1 or M2) is being sensed by the SA circuits and the other one (M2 of M1) is being reconfigured by the write circuit (Fig.8). The MTJ connected to the SA circuits includes the previous Co (as the present Ci) that along with the present inputs A and B, result in the new Co and SUM. At this time, the write circuit reconfigures the other MTJ based on new Co to be used as Ci by the next clock cycle. When the clock signal goes low, both the SA and write circuits will go to an idle state and Co/Co' and SUM/SUM' will go to a high state by the pull-up transistors (P1 to P8 in Fig.5) to get ready for the next read/write operations. In circuit shown in Fig.8, transistor pairs of (P1, N1) to (P4, N4) act as multiplexers to swap MTJs M1 and M2 between the write and SA circuits. To select the MTJs and swap them between the write/SA circuits, a pulse signal of 2CLK is asserted. As declared in Fig.8, this signal has a period two times longer than that of the CLK signal. When 2CLK signal is low, M2 is connected to the write circuit to be configured based on the present Co state. Also, M1 is connected to the read (SA) circuits to be compared with the reference MTJ (denoted as M_{ref}). Fig.9 shows the normal operation of proposed rad-hard serial magnetic adder circuit. It should be noted that, the SUM/Co logic trees and SA circuits employed in this circuit (shown in Fig.8) are quite similar to those used in proposed RH-MFA circuit shown in Fig.5.

B. Proposed fully nonvolatile and radiation hardened MFA (NVRH-MFA)

As one of the most promising choices, hybrid design using MTJ and CMOS are being taken into consideration for the future IC designs thanks to their attractive futures such as nonvolatility, high endurance, high performance, CMOS integration compatibility and low power consumption [8]. Nonvolatile nature of the MTJ cells can be used to design full nonvolatile logic circuits. These circuits can be employed to design a nonvolatile microprocessor or any other digital integrated circuit. Also, for the power-gating architectures nonvolatile logics can resume the last state by power on [21]. In this section, a fully nonvolatile and also rad-hard MFA is proposed. To have nonvolatility, a spin transfer torque magnetic random access memory (STT-MRAM) circuit (shown in Fig.10) is suggested to save inputs A and Ci. This circuit is a low-cost and high-speed MTJ-based memory that is proposed and validated in [6]. As Fig.10 shows, data can be saved by the employed two MTJs. If the clock signal has a logic value of '1', then the path between the supply voltage and the ground will be established through transistors P4-N4 and the MTJ cells. In suggested circuit shown in Fig. 10, there are two modes of write (CLK=0) and read (CLK=1).

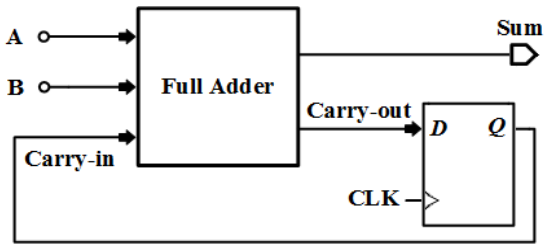

Fig.7. A conventional serial binary adder

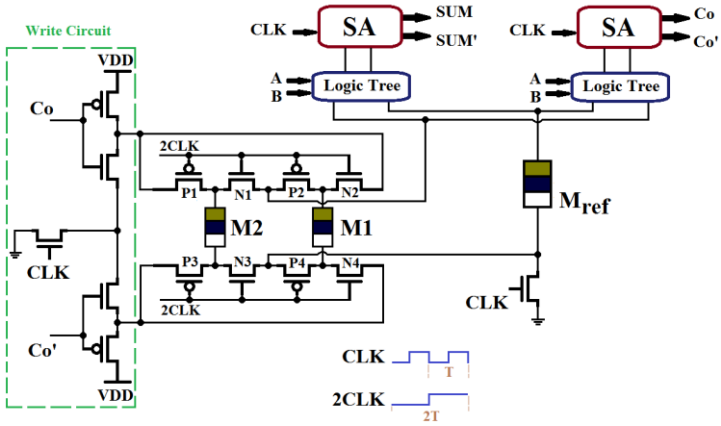

Fig.8. Proposed serial/rad-hard magnetic binary adder (SRH-MBA)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2016.2644721, IEEE Transactions on Device and Materials Reliability

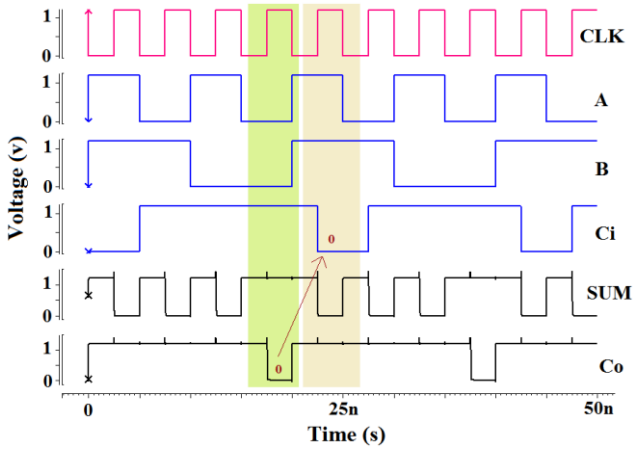

Fig.9. Normal operation of the proposed SRH-MBA circuit

In the write mode (CLK is low), when "Input" is '0', a current flows from V_{dd} to ground through transistor P2, the MTJs, and transistor N3. On the contrary, when "Input" is '1', the current flows through P3 and N2 in a reverse direction of the prior case. Therefore, based on "Input" two configurations for the MTJs are possible including a case that the upper MTJ is in antiparallel mode and the other in parallel and vice versa.

In the read mode (CLK is high), the voltage of node M can be given by one of the (4) or (5) based on the configuration of MTJs. Relation (4) is given for the case that the upper MTJ is in parallel mode and the other is in antiparallel.

$$V_M = V_{dd} \times \frac{R_{High}}{R_{High} + R_{Low}} \quad (4)$$

Considering the obtained TMR ratio of 600% [10], V_M will be equal to about 87.5% of V_{dd} in (4) to present a logic value of '1'.

When the upper MTJ is in antiparallel mode and the other is in parallel, the associated voltage value for node M is given by (5). In this case, with a TMR ratio of 600%, V_M will be equal to about 12.5% of the supply voltage (V_{dd}) to present a zero logic.

$$V_M = V_{dd} \times \frac{R_{Low}}{R_{Low} + R_{High}} \quad (5)$$

If we attach the output of suggested circuit to the logic trees of the proposed RH-MFA (as shown in Fig.11), the resulted design will be a fully nonvolatile and rad-hard MFA. This proposed circuit (the so-called NVRH-MFA) can be used in nonvolatile computing applications and power gating architectures [21].

5- Simulation results and analyses

A) Simulation setup

To investigate the radiation hardening of the proposed MFA circuit, some circuit-level simulations using the SPICE tool have been carried out. To simulate the circuits, a 45nm CMOS technology model [22] and an SPICE-compatible MTJ model [23] are employed. The supply voltage is set to 1.2V and the TMR ratio is assumed as 200% [6].

To inject SEU into the simulated circuits, we used the model proposed in [24] that is a double exponential current source specified by (6).

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_1 - \tau_2}(e^{-t/\tau_1} - e^{-t/\tau_2}) \quad (6)$$

Where, Q_{inj} is the total amount of charge deposited at the struck node. Also, τ_1 and τ_2 are material dependent time constants [24].

B) Investigation of SEU tolerance

As shown in Fig.12, all the logic flips occurred by the SEU injections have been recovered after a short period of time. This recovery is resulted due to a floating voltage of struck node that allows the associated dual node to restore the corrupted data. Also, the MTJs used in proposed circuits are inherently robust against radiation effect [12-14], in result, strike of energetic particles will not change their reconfiguration.

C) Comparative analyses

In general, fault tolerance is achieved at the expense of redundancies that result in energy, performance and area overhead [25]. In this section, we show that, the proposed rad-hard MFA circuits improving fault tolerance have reasonable design parameters. Table 2 compares the properties of proposed RH-MFA with the state-of-art counterparts. As the reported results reveal, our proposed MFA circuits offer a lower energy consumption over the other considered designs as they use fewer MTJs.

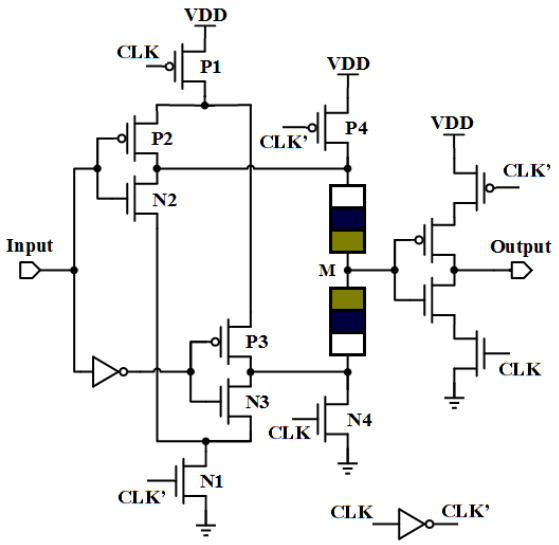

Fig.10. The suggested nonvolatile MTJ-based memory cell (similar to that is proposed in [6])

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2016.2644721, IEEE Transactions on Device and Materials Reliability

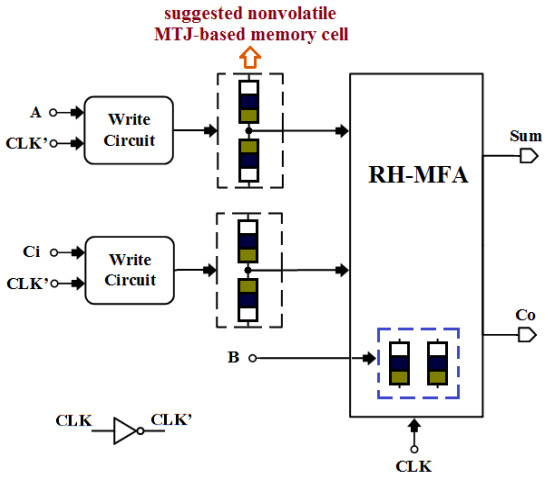

Fig.11. Proposed fully nonvolatile MFA

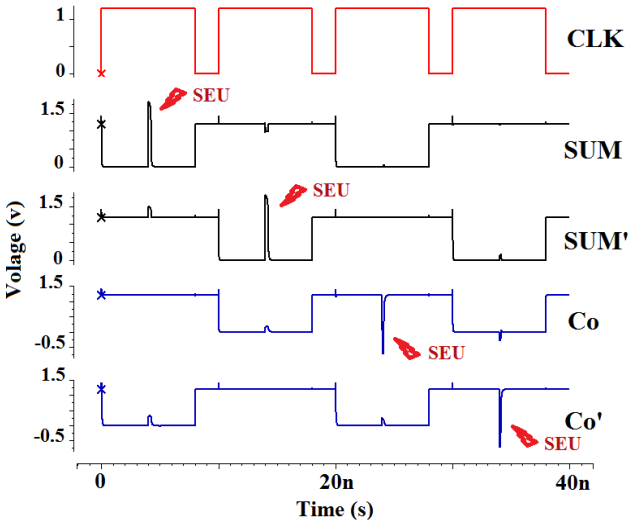

Fig.12. SEU injection to the proposed RH-MFA circuit

In Comparison with the MFA proposed in [7], our proposed RH-MFA offers lower energy and delay in write mode. It also offers a radiation tolerant sensing in evaluation (read) mode. However, it increases delay and energy consumption of sensing that is the expense of its SEU-tolerance. As Table.2 shows, the associated parameters of proposed SRH-MBA circuit is pretty similar to those of the proposed RH-MFA. In other words, comparing with the proposed design in [7], this circuit offers lower energy/delay for write operation. Besides, it increases the associated energy/delay of read operation while offering an SEU-tolerant sensing. The proposed full-nonvolatile rad-hard MFA (NVRH-MFA) should be compared with the full-nonvolatile MFA proposed in [6]. Similar to the prior case, this comparison reveals that, our proposed NVRH-MFA circuit offers a lower cost in write operation. Also, it has a radiation tolerant sensing in read operation at the expense of more cost in that. Therefore we can conclude that, our MFA circuits have improved the reliability of MTJ sensing with a reasonable increase in delay and energy. Besides, our circuit have decreased energy consumption in the pre-charge (write) mode employing fewer reconfigurable MTJs. As can be found from the results, the energy consumed for reconfiguring the MTJs are much more than what is needed for sensing the configuration. Therefore, our proposed MFA circuits have improved total energy consumption considerably. In conclusion, comparing with the considered previous MFAs, our designs incurred a little deration in performance while offered radiation immunity and energy saving.

6- Conclusion

This paper proposed an SEU-tolerant magnetic full-adder (RH-MFA). In comparison with the previous work, the proposed RH-MFA circuit offers a low energy consumption as well as radiation hardening. A serial magnetic adder as well as a full-nonvolatile MFA based on the proposed RH-MFA circuit are also suggested and evaluated. The proposed nonvolatile and rad-hard MFA circuit (NVRH-MFA) can be used for the power gating and reliable architectures. In conclusion, we can claim that the energy consumption and also robustness against radiation effects in magnetic full-adders are improved over the previous work.

Acknowledgments

This work was supported by the University of Shahid Beheshti under Grant # SAD/600/943.

Table 2: comparison table for design parameters of proposed RH-MFA with recent designs

MFA circuit	Hardware area		Fully Nonvolatile?	SEU tolerance?	Read time (ps)	Read energy (fJ)	Write time (ns)	Write energy (fJ)
	# of CMOS transistors	# of reconfigurable MTJs						
Design in [7]	38	4	No	No	122.9	6.67	1.16	202.4
Proposed RH-MFA	43	1	No	Yes	187.48	10.21	1.13	69.9
Proposed SRH-MBA	50	1*	No	Yes	196.12	10.92	1.14	70.2
Design in [6]	58	8	Yes	No	257.19	19.64	1.17	404.3
Proposed NVRH-MFA	75	5	Yes	Yes	220.11	22.85	1.15	274.7

* Although the proposed SRH-MBA circuit includes two reconfigurable MTJs (M1/M2), it has one reconfiguration in a clock cycle similar to the proposed RH-MFA and the MFA proposed in [7].

References

1- S. J. Pearton, F. Ren, Erin Patrick, M. E. Law, A. Y. Polyakov, "Review—Ionizing Radiation Damage Effects on GaN Devices Electronic and Photonic Devices and Systems," ECS J. Solid State Sci. Technol. 2016 5(2): Q35-Q60;

2- R. Rajaei, B. Asgari, M. Tabandeh, M. Fazeli, Design of Robust SRAM Cells Against Single Event Multiple Effects for Nanometer Technologies, IEEE Transactions on Device and Materials Reliability (TDMR) 2015.

3- R. Rajaei, M. Tabandeh, M. Fazeli, Low Cost Soft Error Hardened Latch Designs for Nano-scale CMOS Technology in presence of Process Variation, Microelectronic Reliability (MR), Elsevier, 2013.

4- S. A. Wolf, D. D. Awschalom, R. A. Buhrman, J. M. Daughton, S. von Molnár, M. L. Roukes, A. Y. Chtchelkanova, D. M. Treger, "Spintronics: a spin-based electronics vision for the future," Science 294, 1488–1495 (2001)

5- W. Zhao, E. Belhaire, C. Chappert, P. Mazoyer, "Spin Transfer Torque (STT)-MRAM based Run Time Reconfiguration FPGA circuit," ACM Transactions on Embedded Computing Systems, 2009.

6- E. Deng, Y. Wang, Z. Wang, J. O. Klein, B. Dieny, G. Prenat, W. Zhao, "Robust Magnetic Full-Adder with Voltage Sensing 2T/2MTJ Cell," IEEE/ACM International Conference Symposium on Nanoscale Architectures, 2015.

7- E. Deng, Y. Zhang, J. O. Klein, D. Ravelsona, C. Chappert, W. Zhao, "Low Power Magnetic Full-Adder based on Spin Transfer Torque MRAM," IEEE Transactions on Magnetics, 2013.

8- R. Rajaei, "Radiation Hardened Design of Non-volatile MRAM-based FPGA," IEEE Transactions on Magnetics, 2016.

9- W. Zhao, M. Moreau, E. Deng, Y. Zhang, J.-Michel Portal, J. O. Klein, M. Bocquet, H. Aziza, D. Deleruyelle, C. Muller, D. Querlioz, N. B. Romdhane, D. Ravelosona, Cl. Chappert, "Synchronous Non-Volatile Logic Gate Design Based on Resistive Switching Memories," IEEE Trans. Circuits Syst. I, Reg. Papers, Vol. 61, No. 2, Feb 2014.

10- S. Ikeda, J. Hayakawa, Y. Ashizawa, Y. Lee, K. Miura, H. Hasegawa, M. Tsunoda, F. Matsukura, and H. Ohno, "Tunnel magnetoresistance of 604% at 300 k by suppression of ta diffusion in cofeb/mgo/cofeb pseudo-spin-valves annealed at high temperature," Applied Physics Letters 93, 082508–082508 (2008).

11- W. Zhao, E. Belhaire, Q. Mistral, E. Nicolle, T. Devolder, C. Chappert, "Integration of Spin-RAM technology in FPGA circuits", *Proc. Of 8th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Shanghai, China, 2006.

12- Y. Lakys, W. Zhao, J. Klein, C. Chappert, "Hardening techniques for MRAM-Based non-volatile latches and logic," IEEE Transaction on Nuclear Science, *vol. 59, issue 4, pp.1136-1141,* 2012.

13- W. Kang, W. Zhao, E. Deng, Y. Cheng, J. Klein, D. Ravelosona, Y. Zhang, C. Chappert, "Radiation Hardened hybrid spintronics/CMOS nonvolatile unit using magnetic tunnel junctions," Journal of Physics D: Applied Physics , 2014.

14- R. Rajaei, M. Fazeli, M. Tabandeh, Soft Error-Tolerant Design of MRAM-based Non-Volatile Latches for Sequential Logics, IEEE Transactions on Magnetics, 2014.

15- W. Zhao, E. Belhaire, V. Javerliac, C. Chappert, B. Dieny, "A non-volatile Flip-Flop in Magnetic FPGA chip", *Proc. Of IEEE International Conference on Design & Test of Integrated Systems (IEEE-DTIS), Tunis, Tunisia, 2006.pp.323-327*

16- S. Yamamoto, Y. Shuto, S. Sugahara, "Nonvolatile flip-flop using pseudo-spin-transistor architecture and its power-gating applications," 2012 International Semiconductor Conference Dresden-Grenoble, 2012.

17- R. Rajaei, S. Bakhtavari, F. Eslaminasab, Radiation Hardening by Design for Nonvolatile Magnetic Flip-Flops, The 1st International Conference on New Research Achievements in Electrical and Computer Engineering, Tehran, Iran, 2016.

18- D. Suzuki, M. Natsui, T. Endoh, H. Ohno, and T. Hanyu, "Six-input lookup table circuit with 62% fewer transistors using nonvolatile logic-in-memory architecture with series/parallel-connected magnetic tunnel junctions," J. Appl. Phys., vol. 111, no. 7, p. 07E318 (2012).

19- F. Ren, D. Markovic, "True Energy-Performance Analysis of the MTJ-Based Logic-in-Memory Architecture (1-Bit Full Adder)," IEEE Transactions on Electron Devices, 2010.

20- M. M. Mano, Michael D. Ciletti, "Digital Design", 4th edition, Hardcover, 2006.

21- K. Kwon, S. H. Choday, Y. Kim, K. Roy, "SHE-NVFF: Spin Hall Effect-Based Nonvolatile Flip-Flop for Power Gating Architecture," IEEE Electron Device Letters 35(4):488-490 · April 2014.

22- Predictive Technology Model for Spice Tool. [Online]. Available: http://ptm.asu.edu/

23- J. Kim, A. Chen, B. Behin-Aein, S. Kumar, J.P. Wang, and C.H. Kim, "A Technology-Agnostic MTJ SPICE Model with User-Defined Dimensions for STT-MRAM Scalability Studies", Custom Integrated Circuits Conference (CICC), Sep. 2015.

24- H. Cha and J. H. Patel, "A Logic-Level Model for Particle Hits in CMOS Circuits," in Proc. 12th Int. Conf. ICCD, pp 538-542, 1993.

25- R. Rajaei, M. Tabandeh, M. Fazeli, Single Event Multiple Upset (SEMU) Tolerant Latch Designs in Presence of Process and Temperature Variations, Journal of Circuits, Systems and Computers (JCSC), World Scientific, 2014.

Ramin Rajaei received the M.Sc. and Ph.D. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2009 and 2014 respectively. During the PhD program, he was a member of National Elites Foundation of Iran.
He has been an Assistant Professor with the Department of Electrical Engineering, Shahid Beheshti University, Tehran, Iran, since 2015. His current research interests include reliability and power issues in ASIC/FPGA designs based on CMOS and also emerging technologies.

Sina Bakhtavari Mamaghani received the high school diploma and pre-university certification from Shahid Beheshti High school, a NODET (national organization for development of exceptional talents) school of Urmia, Iran. In 2014, he joined the Department of Electrical Engineering at Shahid Beheshti University, Tehran, Iran, where he currently is working toward the B.Sc. degree. His research interests include digital integrated circuits reliability and efficiency. Under supervision of Dr. Rajaei, he received the Best Paper Award at the 1st International Conference on new Research Achievements in Electrical and Computer Engineering in 2016.