A 128-Tap Highly Tunable CMOS IF Finite Impulse Response Filter for Pulsed Radar Applications

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***Abstract*— A configurable-bandwidth (BW) filter is presented in this paper for pulsed radar applications. To eliminate dispersion effects in the received waveform, a finite impulse response (FIR) topology is proposed, which has a measured standard deviation of an in-band group delay of 11 ns that is primarily dominated by the inherent, fully predictable delay introduced by the sample-and-hold. The filter operates at an IF of 20 MHz, and is tunable in BW from 1.5 to 15 MHz, which makes it optimal to be used with varying pulse widths in the radar. Employing a total of 128 taps, the FIR filter provides greater than 50-dB sharp attenuation in the stopband in order to minimize all out-of-band noise in the low signal-to-noise received radar signal. Fabricated in a 0.18-μm silicon on insulator CMOS process, the proposed filter consumes approximately 3.5 mW/tap with a 1.8-V supply. A 20-MHz two-tone measurement with 200-kHz tone separation shows IIP3 greater than 8.5 dBm.**

***Index Terms*— Bandpass filters, finite impulse response (FIR) filters, matched filters, pulse-doppler radar, radar, widely programmable filters.**

I. Introduction

DISCRETE-TIME analog-domain finite impulse response (FIR) filters are used in a wide range of applications, such as wireless local area network and cellular receivers [1]–[10], frequency synthesizers [11], frequency downconversion [12]–[14], software defined radio [15]–[17], line equalizers [18]–[22], and various other usages [23]–[31]. However, FIR topologies have not been used in radar systems to filter received radar pulses, where they could potentially be even more useful. In a pulsed-Doppler radar transceiver, RF pulses are transmitted and the Doppler-shifted echo signal is returned and processed by the receiver [32]–[36].

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An example of a pulsed-Doppler radar system (see Fig. 1) measures the range and velocity of a target by detecting the transmit time and Doppler shift of a reflected RF-modulated pulse [32]. This transmitter consists of a pair of signal sources—a reference oscillator operating at f_{IF} and a voltage-controlled oscillator (VCO) operating at the RF frequency f_{VCO}. The reference signal is upconverted to $f_{\mathrm{VCO}}-f_{\mathrm{IF}}$ and then pulse modulated at a pulse repetition frequency (PRF) f_{PRF}. A binary pseudorandom phase code is employed to eliminate range ambiguities, while also reducing receiver sensitivity to any in-band interferers that may be present. The pseudorandom pulsed RF signal is radiated from the antenna, to the target, and then reflected back to the antenna with some delay proportionate to the distance between the antenna and the target. The return signal also undergoes a Doppler shift f_D dependent on the target's velocity. The received signal at $f_{\mathrm{VCO}}-f_{\mathrm{IF}}-f_D$ is amplified, bandpass filtered, and then downconverted by an image-reject mixer to $f_{\mathrm{IF}}+f_D$. This IF signal is bandpass filtered through a radar matched filter and then sampled once per pulse by a 1-b analog-to-digital converter (ADC) clocked at $f_S = f_{\mathrm{PRF}}$ [32]–[34]. The sampled signal is then processed by a digital signal processor (DSP) for analysis to determine the range and velocity of the target.

In radar systems, the received signals are typically very weak, often much weaker than the surrounding noise levels resulting in poor signal-to-noise (SNR) ratios. In designing the matched filter, it would be beneficial to reduce the bandwidth (BW) as much as possible in order to improve the SNR; however, filter BWs that are too small would not be able to pass the received pulse without distortion of the pulse envelope in the time domain. Therefore, the matched filter must be designed with a BW large enough to pass the received pulse without causing extreme time-domain distortion, while being small enough to maximize receiver SNR.

In current applications, the matched filter has typically been implemented with surface acoustic wave and bulk-acoustic-wave filters. The disadvantage of these filters is that they are bulky, untunable, temperature sensitive, and must be off chip which is expensive compared to on-chip solutions.

Most previously reported FIR filters typically fall into one of two categories. References [3], [5], [9]–[12], [18]–[20], and [26] all use switched-capacitor designs that typically need one amplifier per tap, while the newer trend in research tends toward switched-current techniques [2], [4], [6]–[8], [13], [15], [17], [21]–[25], [27]–[31] that involves routing current through

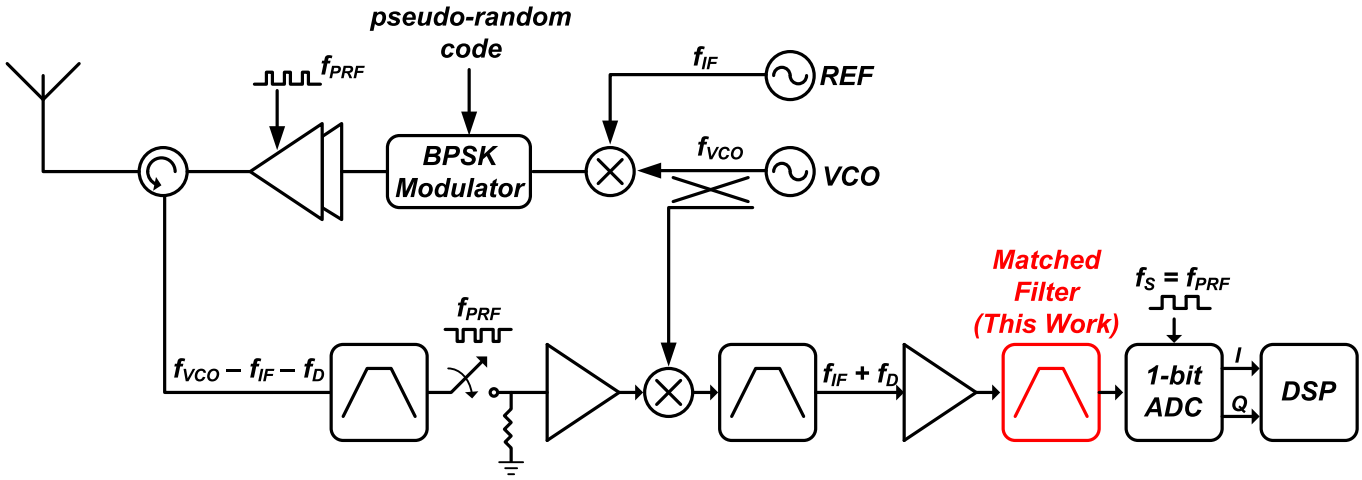

Fig. 1. Block diagram of a pulsed-Doppler radar system with monobit subsampling. This paper presents the design of the matched filter.

switches to charge and discharge capacitors to provide filter function. Of these, references [23], [24] have reported tunable designs; however, these are low-pass filters that can be adjusted in BW by varying the clock rate. If the transfer functions were modified to a bandpass shape, adjusting the clock rate would not only change the filter BW but also have the unfortunate effect of varying the filter's center frequency.

Designed in a 0.18-μm silicon on insulator (SOI) CMOS process [37], this paper presents an FIR bandpass matched filter that has a 1.5–15-MHz tunable BW centered at 20 MHz. The proposed FIR filter employs 128 taps realized by transconductors, switches, capacitors, and 34 nonoverlapping clock phases. The transconductors are highly tunable, which allows them to realize various filter BWs without altering the filter clock rate of 75 MHz. The entire FIR filter architecture dissipates approximately 450 mW and achieves attenuation greater than 50 dB at 5 MHz beyond the −3-dB frequency with a center frequency of 20 MHz. Group delay variations are limited within approximately 10 ns.

This paper is organized as follows. Section II describes the system-level operation of the proposed filter, circuit design is discussed in Section III, and Section IV presents the measurement results with conclusions following in Section V.

II. FIR Filter System-Level Design

To meet the requirements of the radar receiver, the bandpass filter needed to be tunable in BW, while maintaining constant group delay. This is difficult to achieve with conventional analog filters, so a discrete-time FIR topology was chosen. FIR filters are process, voltage, and temperature (PVT) variation tolerant and can usually be scaled in frequency by scaling the clock frequency. FIR filters can usually be implemented at a much higher order than would be conceivable with G_m-C, active-RC, and switched-capacitor techniques. The discrete-time FIR filter can have a constant group delay, whose value depends only on the clock rate and the number of taps. FIR filters can be described as

$$H(z) = \sum_{n=0}^{N} \alpha_n z^{-n} \tag{1}$$

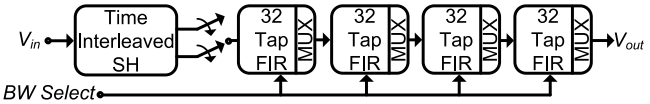

Fig. 2. Proposed 128-tap programmable FIR bandpass filter block diagram including time-interleaved S/H followed by four 32-tap FIR filters with controllable BW.

where N is the number of taps. If the coefficients of (1) are symmetric, meaning

$$\alpha_n = \alpha_{N-n}, \quad 0 \le n \le N \tag{2}$$

then the filter will have constant group delay across all options [38]. For the pulsed-Doppler radar filter, constant group delay will allow the received signal to pass the desired IF pulse without causing time-domain distortion in the pulse shape.

The MATLAB digital filter toolbox was used to obtain the required order and coefficients needed for each desired BW. The selected IF was 20 MHz with an overall clock rate of 75 MHz. The BW was tunable from approximately 1.5 to 15 MHz. In order to obtain the required attenuation of −50 dB at 5 MHz beyond the passband, four identical 32-tap FIR filters were cascaded as illustrated in Fig. 2. Since the operation of the FIR filter in this application is discrete time in nature, the input was first sampled with a sample-and-hold (S/H) circuit. As will be seen during the discussion of the filter architecture, the input to the FIR filter must remain constant during each clock cycle; thus a time-interleaved S/H topology was used to provide a constant input throughout the entire clock cycle.

Fig. 3 shows the ideal overall frequency response of the four cascaded stages and plots BWs of 1.5, 7.5, and 15 MHz. MATLAB simulations showed that a random mismatch of 20% in the filter coefficients will result in less than a 2-ns variation in group delay over the filter's passband.

To explain the operation of the architecture, let us consider the circuit shown in Fig. 4(a), which includes the set of nonoverlapping clock phases illustrated in Fig. 4(b).

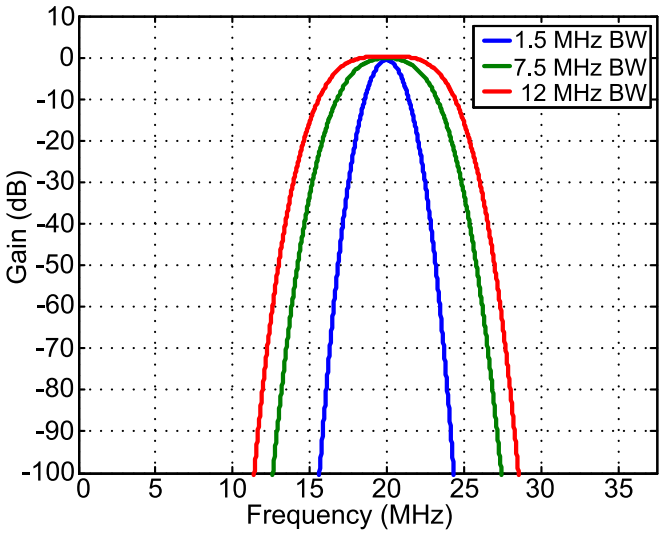

Fig. 3. Ideal magnitude response of the BW programmable 128-tap FIR filter. A 20% random mismatch was included in the filter coefficients. 1.5-, 7.5-, and 15-MHz BWs are shown.

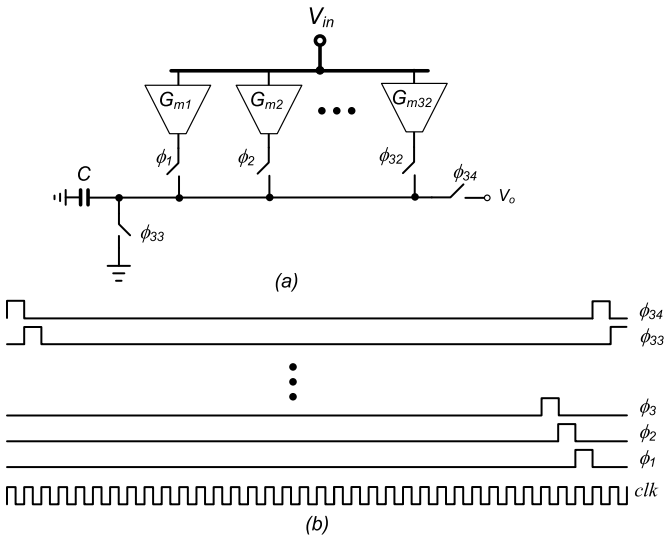

Fig. 4. Single-tap implementation illustrating (a) system level including 32 tunable transconductor cells, charge accumulation capacitor, and switches with (b) required 34 nonoverlapping clock phases.

The input voltage, which is constant during each clock phase, is converted into a set of currents which, depending on the current clock phase, charge the capacitor. The total charge injected onto the capacitor after 32 consecutive cycles and measured at the end of the process during clock phase ϕ_{34} is

$$Q_{C1}[\phi_{34}] = \sum_{i=1}^{32} g_{\mathrm{mi}} v_{\mathrm{in}}[\phi_i] T_{\mathrm{ck}} \tag{3}$$

where T_{ck} is the sample period. Since the charge is accumulated on a capacitor, the voltage at the evaluation phase is

$$V_o[\phi_{34}] = \frac{T_{\mathrm{ck}}}{C} \sum_{i=1}^{32} g_{\mathrm{mi}} v_{\mathrm{in}}[\phi_i]. \tag{4}$$

Employing the z-transform of the discrete-time equation leads to

$$\begin{aligned} V_O[z]|_{\phi_{34}} &= \left(\frac{T_{\mathrm{ck}}}{C}\right)\left(\sum_{i=1}^{32} g_{\mathrm{mi}} z^{-i}\right) V_{\mathrm{in}}[z] \\ &= \left(\frac{T_{\mathrm{ck}}}{C} g_{m1} V_{\mathrm{in}}[z]\right)\left(\sum_{i=1}^{32} \alpha_i z^{-i}\right) \end{aligned} \tag{5}$$

where the coefficients $\alpha_i = 1$ and all other coefficients $\alpha_{2-32} = g_{m2-32}/g_{m1}$. It is clear that (5) resembles a typical discrete-time filter transfer function thus enabling an FIR topology, where the filter coefficients are implemented by ratios of transconductances making the overall filter shape less sensitive to PVT variations; the in-band gain, however, is sensitive to PVT variations, but a simple servo mechanism can be added to make g_{m1}/C inversely proportional to T_{ck} [39].

Although this architecture is interesting, the effective sampling rate is only $T_{\mathrm{ck}}/34$, which is too slow for the intended application. The circuit in Fig. 4(a) with 32 taps is expanded to the proposed FIR topology illustrated in Fig. 5. This filter adds additional capacitors and a multiplexer (MUX) to allow the output signal to be taken from one capacitor each clock cycle.

One concern of this expanded architecture is the effect of capacitor mismatch. This effect can be observed by the effect of a pseudo-FIR filter with the transfer function of

$$H_{\mathrm{mismatch}}(z) = \sum_{n=0}^{N} \Delta\alpha_n z^{-n} \tag{6}$$

working in parallel with the primary FIR filter, where the coefficients $\Delta\alpha_n$ represent the capacitor mismatch. This filter does not present the desired linear phase properties and will produce limitations, mainly on the attenuation of the frequency nulls and also introduce phase variations. The overall filter transfer function can be expressed as

$$H(z) = \sum_{n=0}^{N} \alpha_n z^{-n} + \sum_{n=0}^{N} \Delta\alpha_n z^{-n}. \tag{7}$$

Capacitor and transconductor mismatch should be much less than 20% with good layout techniques. MATLAB simulations show that a 20% mismatch in coefficients does not have much effect on the shape of the passband of the filter. Only the stopband is affected, which still remains at a large amount of attenuation. The true stopband of the filter will be noise limited.

III. FIR Filter Design

A. Sample-and-Hold Design

The input to the FIR filter needs to be constant during each clock period, so that the charge injected onto the capacitor is proportionate to the sampled input voltage. An S/H circuit, which uses half the clock period to track the input signal, cannot be used. Fig. 6 shows the proposed S/H circuit (single-ended representation for simplicity), which is a time-interleaved approach. During one clock period, one of the two S/H circuits will track the input, while the other holds

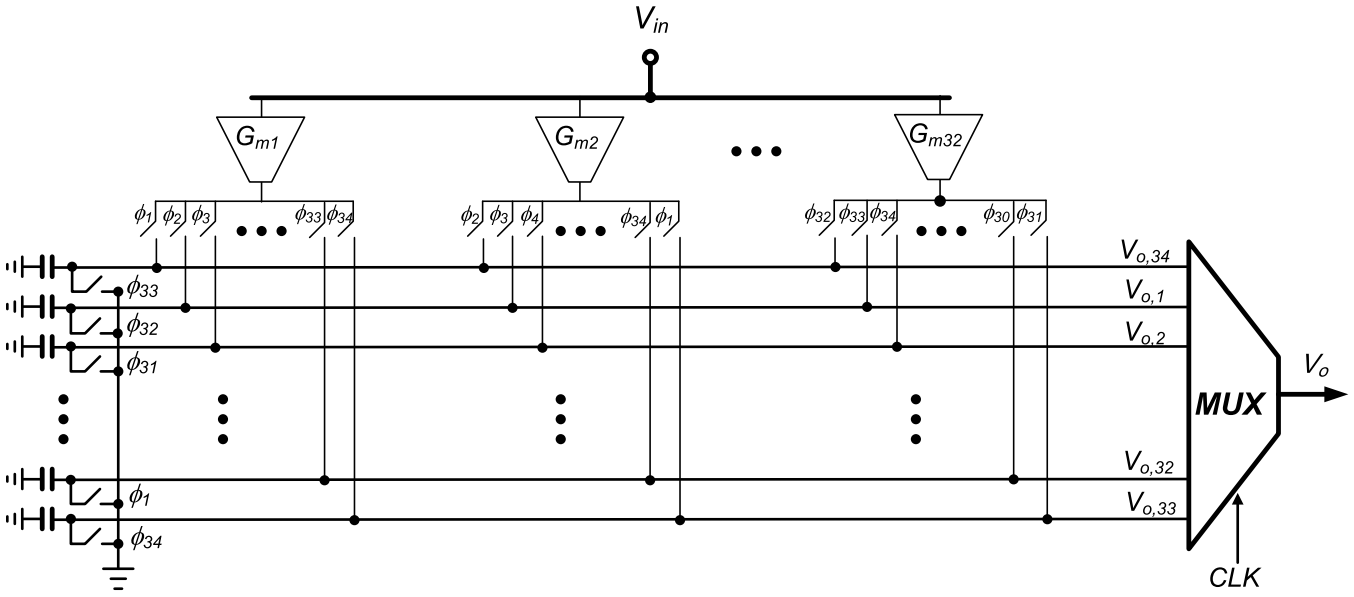

Fig. 5. Thirty-two-tap FIR filter architecture system level including 32 tunable transconductor cells, 34 capacitors, switches, and a MUX. The clock phases used are illustrated in Fig. 4(b).

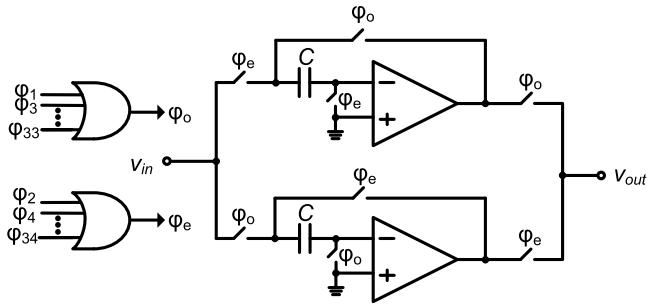

Fig. 6. S/H architecture. The clock phases from Fig. 4(b) are processed through two 17-input OR gates to create the even and odd phases that control the switches in the S/H.

a constant value. These operations will then switch for the next clock cycle, and so on. The S/H circuits each require two nonoverlapping clock phases: one clock will turn the switches ON to sample the input voltage onto the capacitor, while the second clock is used to put the capacitor in feedback around the amplifier during the hold phase.

Ideally, the output of the S/H would be constant during the entire hold phase, which would allow the transconductor cells and capacitors that follow to do the desired integration error free; however, this is not the case due to finite settling time of the amplifier. If a single pole amplifier is employed, the output of the S/H can be approximated to be

$$V_{O,\mathrm{SH}}(t) = V_{O,\mathrm{ideal}}(1 - e^{-t \times \mathrm{GBW}}) \tag{8}$$

where GBW is the gain-BW product of the amplifier loop gain (including loading and feedback factor) and $V_{O,\mathrm{ideal}}$ is the output voltage after full settling. The S/H output voltage drives the filter sections, and each FIR operational transconductance amplifier (OTA) output current is then integrated; thus, the final voltage increment on one of the capacitors of the filter of Fig. 5 during one clock cycle is given by (9). In an ideal case with infinite GBW, the voltage increment on the capacitor is

$$\begin{aligned} V_C(T_{\mathrm{ck}}) &= \frac{1}{C}\int_0^{T_{\mathrm{ck}}} g_{m,i} V_{O,\mathrm{ideal}}(1 - e^{-T_{\mathrm{ck}} \times \mathrm{GBW}})\mathrm{dt} \\ &= \frac{1}{C} g_{m,i} V_{O,\mathrm{ideal}} T_{\mathrm{ck}} \left(1 - \frac{1 - e^{-T_{\mathrm{ck}} \times \mathrm{GBW}}}{\mathrm{GBW} \times T_{\mathrm{ck}}}\right) \end{aligned} \tag{9}$$

$$V_{C,\mathrm{ideal}} = \frac{1}{C} g_{m,i} V_{O,\mathrm{ideal}} T_{\mathrm{ck}}. \tag{10}$$

Subtracting (9) from (10) gives the coefficient of error which is approximated as $1/(\mathrm{GBW} \times T_{\mathrm{ck}}$ with GBW in radians per second. For a sample rate of 75 MHz and an amplifier GBW of 600 MHz, the error accumulated in a clock period is 2%.

Another source of integration error in the FIR transfer function is due to the finite gain of the S/H amplifiers. Gain error is inversely proportional to the amplifier's gain, which was more than 60 dB, which will result in an error of less than 0.1%. This error is much less than the error introduced due to the amplifier's finite BW so is of little concern in the presented system.

A more concerning effect of the limited amplifier gain is its effect on unwanted spurs that occur during the time-interleaved operation. Since the filter's clock rate is 75 MHz (Nyquist frequency is 37.5 MHz), the signal BW for the widest 15-MHz BW shows that in-band signal is limited to 27.5 MHz, which satisfies the Nyquist criteria. However, each S/H section operates at 37.5 MHz, resulting in alias components falling in-band. Mismatch between the two branches will not cancel these components, and remaining alias in-band components will be present at the S/H output. The S/H errors are a function of the gain error function, which again are limited by the greater than 60-dB gain in the amplifier as well as its broadband nature (unity gain frequency in the range of 600 MHz), and therefore, not a major concern in the proposed design.

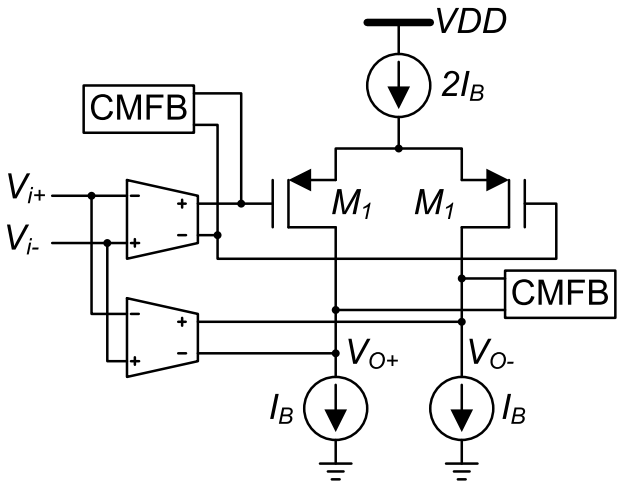

Fig. 7. S/H amplifier with CMFB.

Succeeding the S/H is the set of 32 transconductors for the FIR filter, which has a total input capacitance of 3.8 pF. The amplifier topology used to meet the GBW requirements, while driving this large capacitive load is a two-stage operational amplifier with a low-power, high-gain folded-cascode configuration in the first stage, and a high-power feed-forward stage for amplifier stability [40]. A simplified schematic of the amplifier is illustrated in Fig. 7. The common-mode feedback (CMFB) schemes are realized by employing the approach reported in [41].

B. Tunable G_m

In the proposed filter topology, the BW of the filter needs to be tunable, which is achieved by varying the filter coefficients α_n from (1). In this design, the tuning of the coefficients α_n is done by varying the transconductors from Fig. 5 using the bank of transistors M_{T1}–M_{T5} to achieve the correct filter coefficients according to (5). Table I lists the transconductance values needed to meet the set of BWs required by the system. Ranging from 95 to less than 0.1 μA/V, each transconductor cell must be tunable in both magnitude and polarity across a broad range of values that do not follow any sort of common pattern between varying filter BW selections. For each filter setting, there are only 16 different transconductance values needed, since the filter is symmetric. All transconductance values less than 0.1 μA/V were set to zero; MATLAB simulations show that doing this has little effect on the shape of the filter in the passband—stopband attenuation decreases from 250 for the ideal case to 90 dB when the smallest transconductors are set to zero and a 20% random mismatch in the remaining filter coefficients, which still meets the required specifications. In order to zero the small transconductors, the bias current sources are disabled for the transconductors of interest.

Since the required transconductance values vary by several orders of magnitude, it is inefficient to design a single device that can meet every requirement. In this design, five transconductors were designed, which have the following transconductance tuning ranges: 0.2–2 μA/V, 0.7–6 μA/V, 1–11 μA/V, 4–20 μA/V, and 20–100 μA/V. These tuning

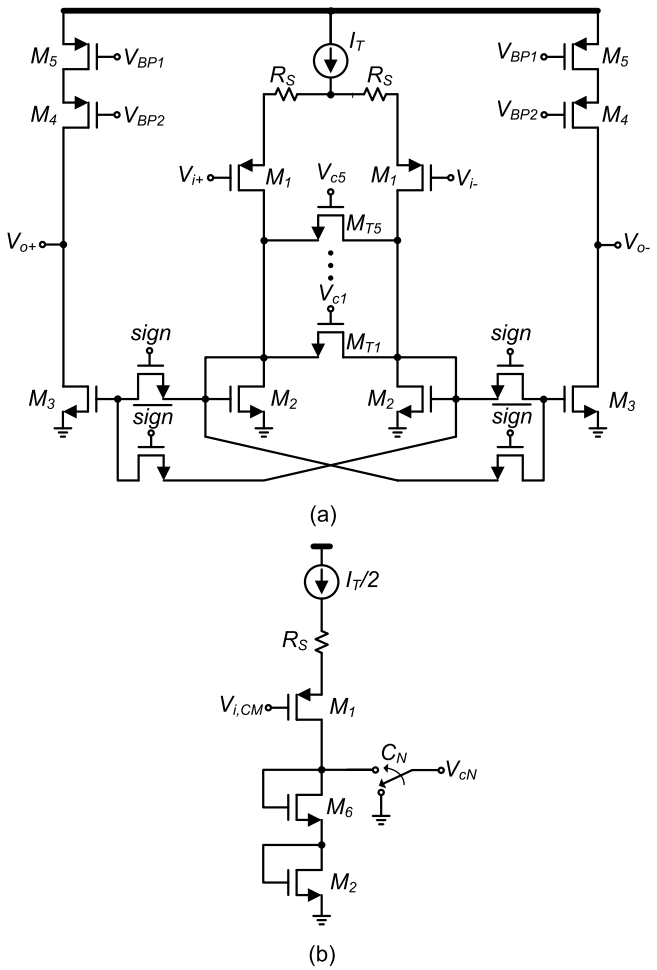

Fig. 8. (a) Tunable transconductance topology with polarity control. (b) Replica circuit for tuning voltage generation.

range values allow for a single transconductor to be used for any one tap; i.e., the 20–100 μA/Vtransconductor can be used for tap 16, since this fully covers its required range. Likewise, the 1–11-μA/V transconductor can be used for tap 15 and 17. Multiple transconductors in parallel are not needed.

The schematic of the proposed widely tunable transconductor is shown in Fig. 8(a). The transconductor consists of a basic source degenerated differential pair with a current mirror load. The transistors M_{T1}–M_{T6} are placed across the drain of the transistors in the differential pair and, along with the replica circuit shown in Fig. 8(b), are used to tune the transconductance by attenuating the differential current entering into the current mirror load. The tuning transistors operate in the triode region when activated and present a resistance of R_{tune} that is controlled by the gate voltage equal to $2V_{\text{gs}2}$. Due to the overall array of impedances, the total low-frequency current being mirrored from M_2 to M_3 is then computed as

$$i_{\text{out}} = V_{\text{in}} \times \frac{g_{m1}}{1 + g_{m1}R_S} \times \frac{\frac{R_{\text{tune}}}{2}}{\frac{R_{\text{tune}}}{2} + \frac{1}{g_{m2}}}. \tag{11}$$

Due to the replica circuit of Fig. 8(b), the overdrive voltage $V_{\text{GS}} - V_T$ of M_2 and M_T is similar, which gives an overall

TABLE I
REQUIRED G_m VALUES FOR THE SET OF TUNABLE TRANSCONDUCTORS IN μA/V

Tap Number	1.5 MHz	2 MHz	3 MHz	4 MHz	5 MHz	6 MHz	7.5 MHz	10 MHz	12.5 MHz	15 MHz
1, 31	0.0	0.0	0.0	0.0	0.0	0.3	0.4	0.2	0.4	0.2
2, 30	0.0	0.0	0.0	0.0	0.0	0.0	-0.1	0.0	-0.1	0.0
3, 29	-2.7	0.0	0.0	0.0	0.7	0.1	-0.7	0.8	-0.4	1.0
4, 28	0.0	0.0	0.0	0.0	-0.5	-0.3	0.1	-0.5	-0.2	-0.4
5, 27	4.5	2.1	0.0	0.0	-2.1	-1.8	-0.6	-1.6	-1.9	-0.4
6, 26	-3.2	-1.8	0.0	0.0	1.4	1.6	1.2	0.4	1.5	-1.0
7, 25	-6.5	-4.4	0.0	0.0	2.3	3.3	3.6	-1.4	1.7	-3.6
8, 24	6.6	5.2	-2.5	0.0	-1.0	-2.5	-3.9	3.6	1.0	2.7
9, 23	7.9	7.1	-4.8	-3.0	1.0	-1.0	-3.5	5.6	4.8	-0.9
10, 22	-11.2	-11.0	9.4	7.6	-5.4	-2.8	1.2	-6.6	-9.3	8.1
11, 21	-7.9	-8.4	8.3	7.8	-6.9	-5.6	-3.3	-1.0	-4.7	7.5
12, 20	16.2	18.2	-20.2	-20.8	20.5	19.4	16.7	-10.2	-2.6	-7.2
13, 19	6.0	7.1	-8.5	-9.2	9.7	9.9	10.0	-9.2	-7.7	4.9
14, 18	-20.1	-24.6	31.0	25.0	-38.3	-41.1	-44.8	48.5	50.5	-49.7
15, 17	-2.2	-2.8	3.6	4.2	-4.7	-5.1	-5.8	6.8	7.7	-8.6
16	21.5	27.1	-35.6	-41.3	46.5	51.4	59.1	-70.5	-81.9	94.9

low-frequency transconductance that can be approximated as

$$G_m = \frac{g_{m1}}{1 + g_{m1} R_S} \times \frac{1}{1 + 2 \times \frac{(W/L)_T}{(W/L)_2}}. \tag{12}$$

The input stage of all transconductors is similar and is optimized for noise and linearity; g_m tunability is achieved through the bank of transistors M_{Ti} that operate in the triode region. The transconductance can thus be tuned by adjusting the ratio of two transistor dimensions, which is reliable with PVT variations. The tuning is carried out through a bank of transistors that allows the adjustment of $(W/L)_T$ without affecting the OTA operating point. However, g_m itself is susceptible to PVT variations, which can introduce a gain error in the FIR filter according to (5). A tuning scheme can be used, if better accuracy is needed in the FIR filter gain [39] but was not included because accurate passband gain was not a critical design parameter for the radar matched filter.

The input referred thermal noise of the transconductor cells is a function of the OTA transconductance values and can be calculated as

$$v_{n,\text{in}}^2 = 8kT \left(\frac{1 + g_{m1} R_S}{g_{m1}} \right)^2 \times \left[\frac{\gamma}{A_{\text{cd}}^2} (g_{m3} + g_{m5}) + \gamma\, g_{m2} + \frac{2}{r_{ds,T}} + \left(R_S g_{m1}^2 + \gamma\, g_{m1} \right) \left(\frac{1}{1 + g_{m1} R_S} \right)^2 \right] \tag{13}$$

where γ is the noise fitting factor and is typically between 2/3 and 1; meanwhile, the A_{cd} factor represents the current division gain between the diode connected transistor M_2 and the tuning transistor M_T, which is expressed as

$$A_{\text{cd}} = \frac{g_{m2} r_{\text{ds},T}}{2 + g_{m2} r_{ds,T}}. \tag{14}$$

This results in a noise power density ranging from -149 dBm/Hz when all of the tuning transistors are OFF (maximum transconductance gain) to about -121 dBm/Hz when they are all switched ON (minimum transconductance gain), which is the worst case since the current division factor is maximum under this condition. According to Table I, the two most dominant transconductors of Fig. 5, g_{m14} and g_{m16}, will both have their highest input referred noise level when the filter BW is at its minimum; therefore, total integrated noise will stay fairly constant across BW selections; this result agrees with the fact that noise is usually dominated by kT/C, and in this filter realization, the load capacitor remains constant.

TABLE II
DEVICE SIZES FOR THE 20–100-μA/V TRANSCONDUCTANCE CELL. THE SMALLER TRANSCONDUCTOR CELLS ARE SCALED DOWN VERSIONS OF THIS TRANSCONDUCTOR

Component	Size
M_1	16 / 1
M_2	3 / 1
M_3	3 / 1
M_4	10 / 0.4
M_5	10 / 0.4
M_6	3 / 1
M_T	0.22/0.8 to 3.52/0.8
R_s	4 kΩ
C_s	650 fF

TABLE III
PERFORMANCE METRICS OF THE 20–100-μA/V TRANSCONDUCTANCE CELL

Specification	Values
G_m Range	20 – 100 µA/V
IIP3	>16 dBm
Power Noise Density	< -132 dBm/Hz
Power Consumption	316 µW

Table II lists the sizes of the transistors, capacitors, and resistors for the 20–100-μA/V transconductor cell. The other four tunable transconductors are scaled down versions of this cell. Achievable transconductance values for the 20–100-μA/V transconductor cell are shown in Fig. 9. Five control bits were used to achieve the required values needed to generate the FIR filter coefficients. An additional sixth control bit was used to provide polarity control to switch the transconductor's singe between positive and negative. Table III summarizes the performance metrics of the 20–100-μA/V transconductors.

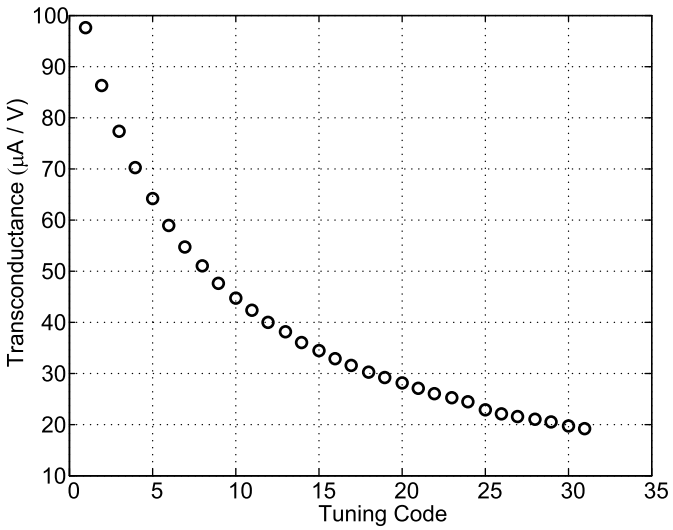

Fig. 9. Tunability of the 20–100-μA/V transconductor. Five control bits were used to access values across the desired range.

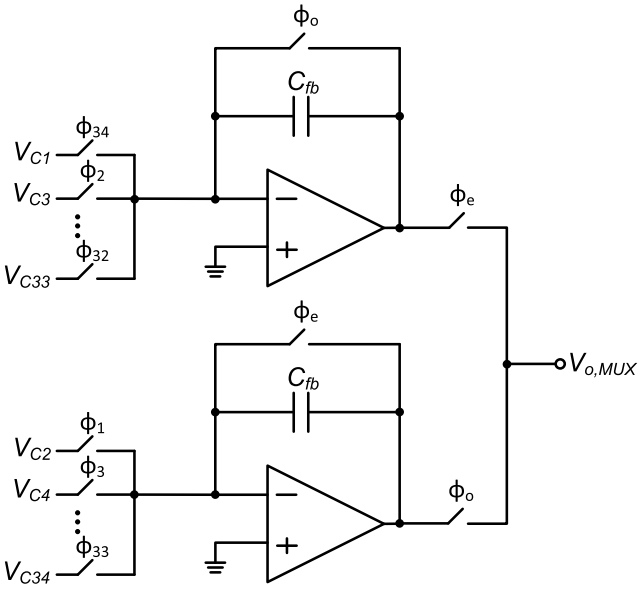

Fig. 10. Time-interleaved MUX topology.

The other four tunable transconductors have similar performance.

C. Active MUX

The simplified single-ended schematic of the MUX is illustrated in Fig. 10, which is a time-interleaved topology similar to that used for the S/H. During the even numbered clock phases, the charge from the desired capacitor is injected onto the capacitor $C_{\rm fb}$ which, in conjunction with the amplifier, holds the output voltage until the next cycle; meanwhile, in the second amplifier, the voltage across the feedback capacitor is being reset to zero to prepare it for its upcoming hold phase.

The amplifier needs to drive the following stage, which consists of the set of tunable transconductors in the same way that the S/H must drive the first stage's transconductors. This makes the requirements for the amplifier of the MUX to be the same as that of the S/H; the same amplifier topology is used here. The GBW of the amplifier is around 600 MHz when driving a 5-pF load with each amplifier consuming 47 mW due to timing constraints and large capacitors involved in its operation.

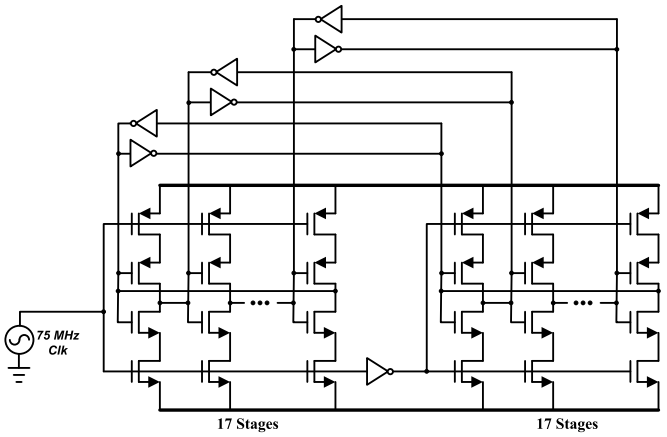

Fig. 11. Seventeen-stage injection-locked ring oscillator used for the generation of the 34 nonoverlapping clock phases.

D. Thirty-Four-Phase Nonoverlapping Clock Generator

Of key importance in the operation of the FIR filter is the 34-phase nonoverlapping clock generator. For the proposed solution, a differential ring oscillator is locked with the reference clock to synchronously oscillate at a frequency equal to 75/34 MHz as illustrated in Fig. 11 [42]. Although only 17 inverters are used, the frequency is divided by 34 since each one of the positive and negative transitions of the ring oscillator requires 17 clock cycles of the master clock to propagate through the inverter chain demanding a total of 34 clock cycles to complete a full cycle. The injection locking technique dictates when the transitions of the ring oscillator will occur; thus, the jitter performance of the ring oscillator output is correlated with that of the master clock.

The nonoverlapping behavior is obtained by adding delay elements at CkB outputs of each inverter stage as shown in Fig. 12. These delayed inverted clock signals combined with the original noninverted clock signals allow the required nonoverlapping clock signals to be obtained. For example, clock phase ϕ_1 is obtained by ANDing the clock phases Ck1B and Ck2 as depicted in Fig. 13. Similarly, clock phase ϕ_2 is obtained by ANDing Ck2B and Ck3. The nonoverlapping time is defined by the delay of the digital buffers used.

E. Switch Design

All switches used are single n-type metal oxide semiconductor transistors. The common-mode voltage throughout the system was set to 600 mV. With a 1.8-V supply, this allows sufficient overdrive voltage on the switches remedying the need for a full transmission gate. The dimensions of the switches are 1.0/0.18 μm, which produce 1 kΩ of switch

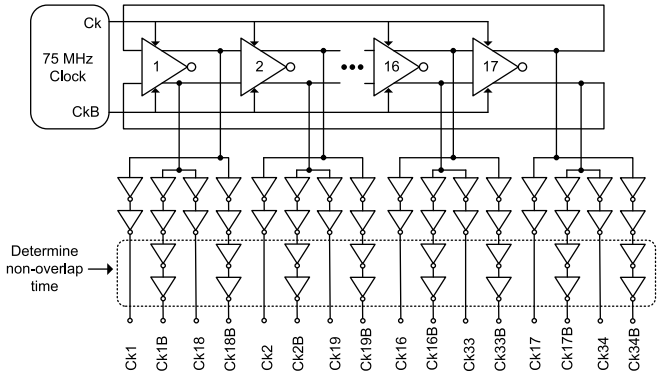

Fig. 12. Clock signals used in the generation of the 34 nonoverlapping clock phases.

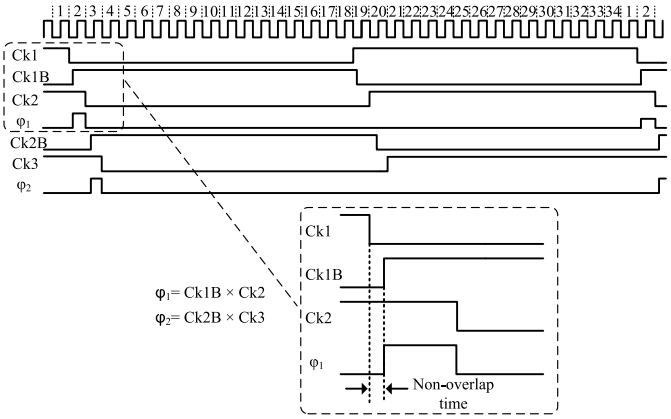

Fig. 13. Generation of the nonoverlapping clock phases.

resistance in simulations for a typical corner. The small switch size minimizes the effect of any clock feedthrough or charge injection issues. Since OTA output is current, the FIR architecture is tolerant to the resistance of the switches connected in series between OTA outputs and integrating capacitors.

IV. Measurement Results

The filter was fabricated in the Jazz 0.18-μm CMOS SOI process and designed to have an IF frequency of 20 MHz with a BW adjustable from 1.5 to 15 MHz. Fig. 14 shows the photograph of the fabricated filter. The full die area is 2×3 mm^2 with the main filter area being approximately 1.6×2.1 mm^2. The four FIR filter stages consume the majority of the area. The nonoverlapping clock generation is centrally located to minimize delay differences in the individual clock phases as they are distributed to the switches in the filter stages.

The filter consumes approximately 250 mA from a 1.8-V supply for a total power consumption of 450 mW. Each tunable OTA consumes approximately 195 μW. The majority of the power consumption is from the amplifiers used in the MUX, which each consume 47 mW due to their need to drive a 3.5-pF load, while maintaining fast settling time performance. In this design, the final FIR stage had to drive the pads and active probes that have comparable input impedance to the transconductors; however, in the radar system, a 1-b

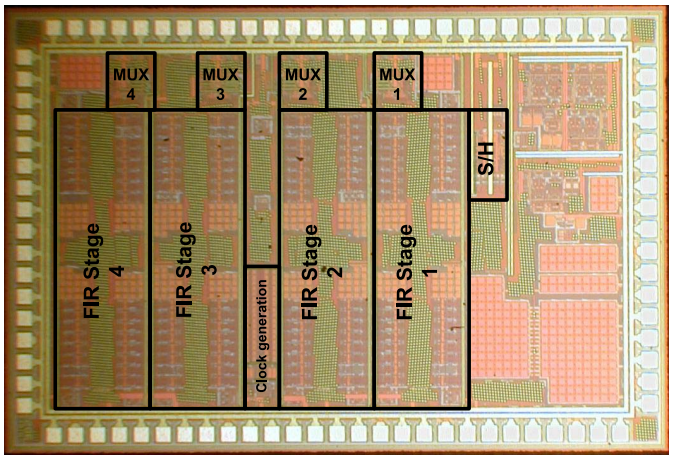

Fig. 14. Photograph of the 2 mm $\times$ 3 mm die with 1.6 mm $\times$ 2.1 mm active area used for the FIR filter.

ADC follows the FIR filter so the load capacitance will be greatly reduced to less than 100 fF [32]–[34]. The final stage could therefore be scaled down to use less than 1 mW, each representing a savings of 92 mW, or a 20% reduction in power.

To measure the frequency response of the FIR filter, a network analyzer was used with an input power of -10 dBm. The magnitude response of the FIR filter is illustrated in Fig. 15(a); BW selections of 1.5, 7.5, and 15 MHz are shown. The center frequency is near 20 MHz, and there is a near rectangular sharp roll-off in the stopband to help suppress all of the received radar pulse's thermal noise and blockers that are not in the BW of the filter. Nearly 50-dB attenuation is achieved in the stopband. The droop in gain evident in the wider BW cases is due to *sinc* distortion from the low-pass sampling operation [14]. This effect is most prevalent during the wider BW cases due to the fact that the upper corner frequency is near the Nyquist frequency of 37.5 MHz, where a zero is located. If needed, one method to minimize this effect would be to use a higher sampling rate which would push the null at the Nyquist frequency further from the passband. Alternatively, since this is a known systematic effect, it could be compensated in the digital domain by DSP since an ADC follows this matched filter; the result of this operation is illustrated in Fig. 15(b). For the designed radar application, *sinc* (magnitude) distortion is not detrimental since the critical information is in the time delay of the received signal and not in its amplitude.

For testing the linearity of the highly selective bandpass filter, a two-tone test was done with input frequency tones of 19.9 and 20.1 MHz. Fig. 16 shows a plot of the IIP3 for each BW selection. The worst case IIP3 is 8.5 dBm with the maximum reaching approximately 11.7 dBm.

To measure the noise performance of the filter, a 50-Ω load was attached to the input of the filter. The noise spectrum at the filter output plus buffers was measured for each BW. The output noise spectral density was integrated to find the total noise that appears at the output as illustrated in Fig. 17. These values fit well with the estimated noise level discussed in Section III-B.

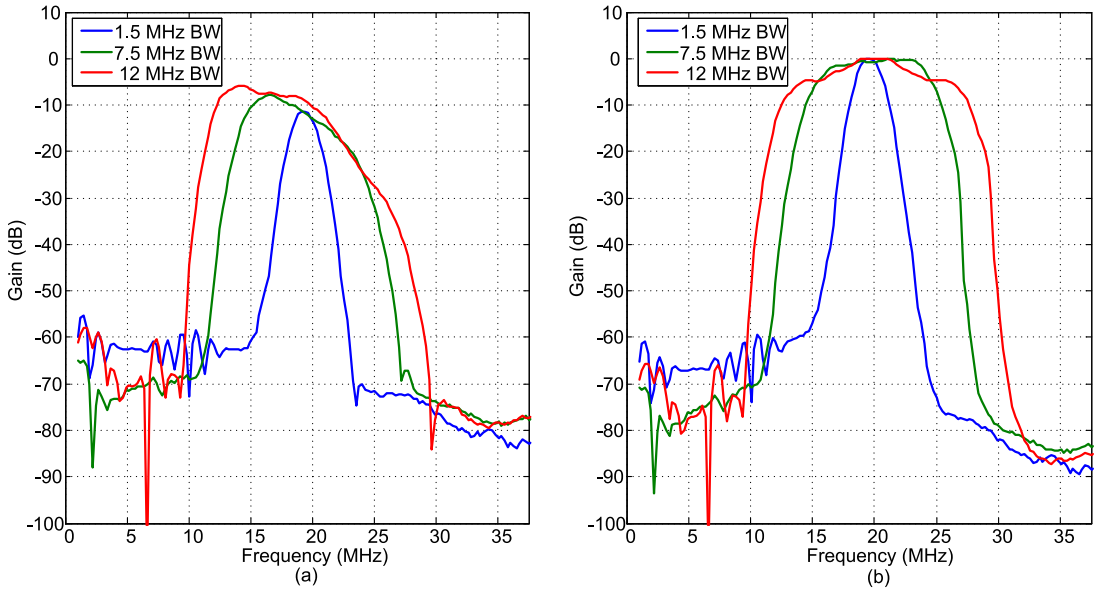

Fig. 15. (a) Measured magnitude response of FIR filter. BWs of 1.5, 7.5, and 15 MHz are shown. (b) Measured magnitude response after being compensated for the sinc distortion that appears in (a).

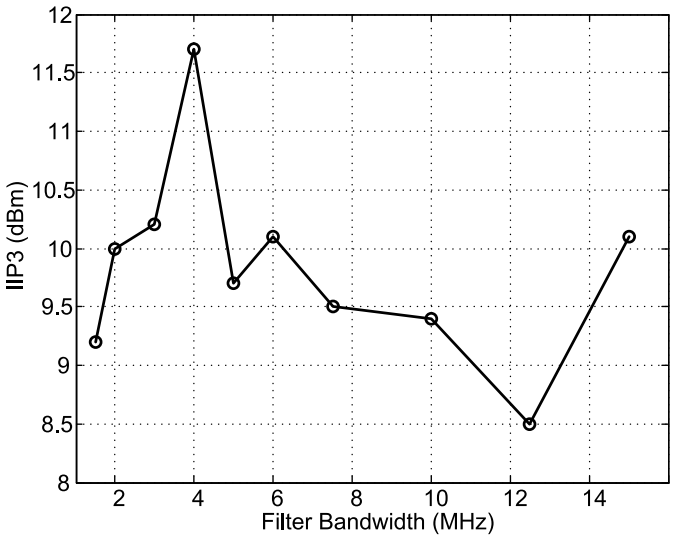

Fig. 16. Measured IIP3 across all filter BWs.

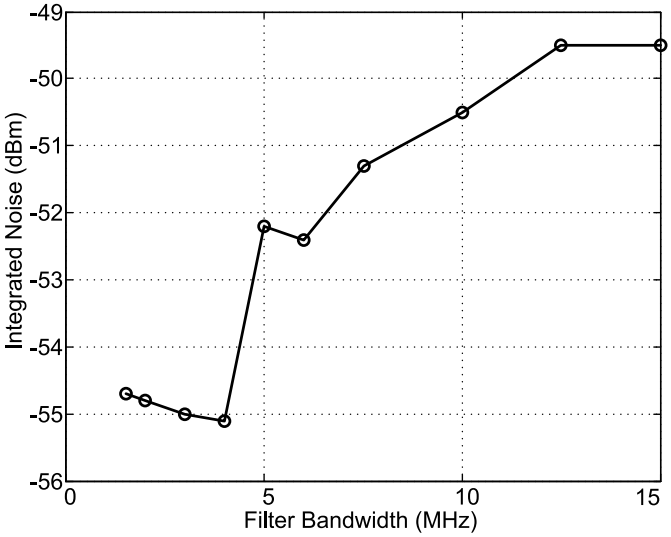

Fig. 17. Measured total in-band integrated output noise power for each filter BW selection.

One of the main requirements of this filter was to have a linear phase response so that the pulsed waveform could pass through the filter without large amounts of dispersion in the time domain. The phase of the FIR filter was measured as depicted in Fig. 18; as expected, it looks very linear within two times filter BW, e.g., 1.5-MHz BW and frequency span is 3 MHz. However, due to the sampling operation at the input of the filter, it is difficult to get meaningful group delay information from a network analyzer because the S/H delay can vary by the sample period by just varying the initial phase of the input. Because of this constraint, modulated pulses of varying frequency across the filter's passband that emulate radar signals were input into the filter and the output was measured, as displayed in Fig. 19 for two cases. The envelope of the input and outputs were obtained and used to calculate the overall delay. Fig. 20 shows the pulse delay averaged across the BW of each filter BW selection. Also shown is the standard deviation. Included in these results is also the variation introduced by the S/H circuitry which is in the range of $\pm T_S/2 = 6.67$ ns so the true variation in group delay in each BW of the filter itself will be less than what is shown. To minimize this issue, it is recommended to increase the oversampling ratio (e.g., >6) that evidently results in a tradeoff since power consumption increases. These results include the phase errors introduced by the buffers.

Table IV summarizes the results and compares them with previously published FIR filters; unfortunately, previous filters were not designed for radar applications and the number of taps is small compared to this paper. Also, most published

TABLE IV

SUMMARY AND COMPARISON OF PREVIOUS PUBLICATIONS. ATTENUATION AT 5 MHz FROM BW FOR [11] AND [23] ARE ESTIMATED FROM MAGNITUDE RESPONSE PLOTS IN THEIR MEASUREMENT RESULTS

Reference	Technology	Filter Type	Bandwidth (MHz)	Attenuation at 5 MHz from BW (dB)	IIP3 (dBm)	Number of Taps	Power per tap (mW)	Power (mW)
[5]	130 nm CMOS	Low-Pass	<5	-10	12	12	0.2	6
[11]	350 nm CMOS	Band-Pass	2	<-10	NR	15	9	136
[23]	65 nm CMOS	Low-Pass	5–26	<-30	-19	12	0.7	8.4
[43]**	45 nm CMOS	Low-Pass	600	<-20	11	16	4	64
This work	180 nm SOI CMOS	Band-Pass	1.5–15	-60	Worst case 8.5	128	2.6*	358*

* Power consumption excluding the power of the buffers.
** -3 dB bandwidth, attenuation at 5 MHz offset, and IIP3 were extracted from original paper.

Fig. 18. Measured in-band phase response of the filter for the case of 1.5-MHz BW.

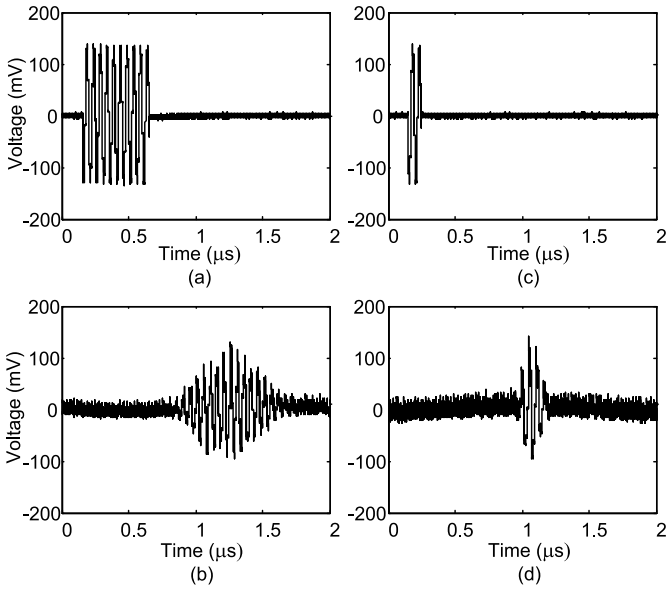

Fig. 19. Measured pulse response of filter. (a) 500-ns input pulse with filter BW set to 2 MHz. (b) Output pulse showing no time dispersion distortion. (c) 100-ns input pulse with a duration of 100 ns with filter BW set to 10 MHz. (d) Output pulse showing no time dispersion distortion.

works are low pass. The reported work that is bandpass is not tunable in BW, only center frequency by varying the clock rate; thus, a direct comparison between this paper and the previously published results is difficult. Although not shown in this paper, the switching capacitor nature of this architecture allows tuning filter's center frequency by employing the clock. Reference [11] presented a bandpass filter centered at 57 MHz with a fixed BW. By varying the sample rate, its center frequency shifted; however, its BW stayed fairly constant in the 1–2-MHz range. Reference [23] implemented a low-pass filter with a tunable BW that could potentially be used in a direct conversion radar receiver but exhibits very limited IIP3. To the best of the authors' knowledge, the filter presented in this paper is the only widely tunable BW bandpass FIR filter; center frequency programming with clock frequency is an additional benefit due to its switched nature. Annaid *et al.* [43] reported a 600-MHz low-pass 16-tap FIR filter; stopband attenuation is limited and power consumption is significant although is fabricated in an advanced 45-nm technology. While using more power than other approaches, this drawback is not a concern for a radar system that has power amplifiers operating at greater than 10 W. This new

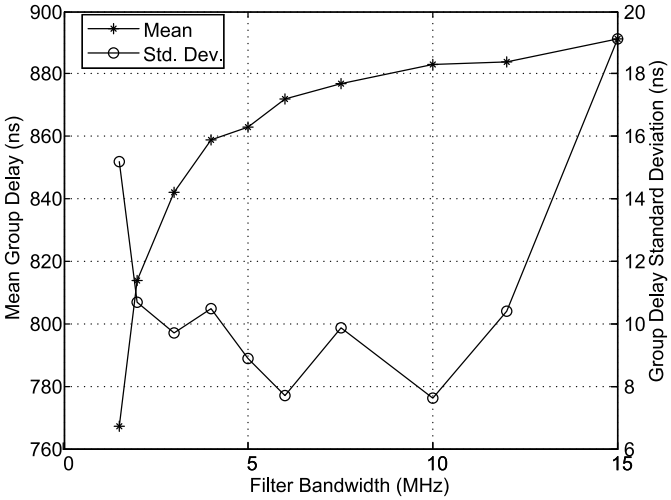

Fig. 20. Mean pulse delay averaged over the filter BW with the standard deviation illustrated as well. These results include the variations introduced due to the SH.

architecture allows complete control over the filter's transfer function at the expense of having one transconductor per coefficient. Although fabricated in 0.18-μm technology, this solution consumes only 3.5–2.6 mW per tap when the output

buffer's power is not included. This solution offers unmatched attenuation factors in the stopband.

V. Conclusion

This paper introduces a programmable linear phase 128-tap FIR bandpass filter in a 0.18-μm Jazz SOI process. The filter has a 20-MHz IF and is tunable in BW from 1.5 to 15 MHz. Due to the nature of linear phase FIR filters, minimal group delay variations are generated, which is optimal for pulsed-Doppler radar systems. The filter has a mean IIP3 of 9.8 dBm. The total integrated noise is a worst case of -49 dBm. The FIR filter architecture employs the cascade of four 32-tap sections coupled by four active MUX sections leading to an FIR filter with 128 taps. The filter is highly programmable in BW thanks to the use of bias constant OTA with a widely adjustable transconductance. The OTA current is coherently integrated in a set of capacitors that are sequentially read through the active MUXs, employing a phase synthesizer that generates 34 nonoverlapping clock phases. The architecture is suitable for high-frequency operation, and it is amenable for advanced technologies since it is based on current mode techniques.

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Dr. Rodenbeck was a recipient of the 2016 Texas A&M University Outstanding Early Career Professional Achievement Award from among more than 100 000 engineering alumni, the IEEE MTT-S Outstanding Young Engineer Award in 2015, the prestigious 2012 NNSA Award of Excellence, a Sandia Innovator Award in 2013, and an internal citation for "Excellence in Radar Technology Leadership" in 2011. He was the Principal Investigator for an R&D program. He is an Associate Editor of the *Encyclopedia of Electrical and Electronics Engineering* (New York, NY, USA: Wiley), responsible for the Microwave Theory and Techniques subject area.