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Multiloop Control for Fast Transient DC–DC Converter

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***Abstract*— A novel ac coupled feedback (ACCF) is proposed to alternatively realize fast transient response while inherently controlling the start-up in-rush current of a dc–dc switching converter. The proposed ACCF is modified from a conventional capacitor multiplier and connected between the outputs of the converter and the transconductance. With this supplemental feedback, the transient response has been significantly improved due to the gain-boosting effect around the compensator's mid-band. Moreover, the ACCF circuit assists to manage the ramping speed of the output voltage during power-up, thereby eliminating the bulky soft-start circuit. The new controller is very simple to implement and occupies a tiny footprint on-chip. A buck converter with the proposed scheme has been fabricated using the 0.18-μm standard CMOS process with an active silicon area of 0.573 mm^2. Measurement results show that the output voltage rises linearly for a soft-start period of 1.05 ms according to the designed slope. Excellent load transient responses are achieved under different load current steps; the output voltage overshoot/undershoot of 60 mV settles down within 10 μs for a load variation from 50 μA to 1 A in 1 μs. Moreover, the proposed converter maintains both excellent load and line regulations of 0.018 mV/mA and 0.0056 mV/mV, respectively.**

***Index Terms*— Current mode, dc-dc converter, fast transient, output voltage overshoot/undershoot, pulsewidth modulation, recovery time, soft-start.**

I. Introduction

THE demand for fast load transient performance has grown significantly, affecting the power supplies of modern high-speed processors—especially processors targeting to achieve a fast transition from the low-power idle mode to the high-speed active mode [1]. There is a massive load current change when the system switches from an idle mode to an active mode. Ideally, the regulator should maintain a voltage level that is almost constant, which means that there should be a negligible output voltage overshoot/undershoot and rapid response time. To accomplish these stringent requirements, various research works on fast transient dc–dc converters have been proposed. Among these methods, the increase of system bandwidth has been the most general solution for the majority of the analog circuits designed according to the linear control theory. In the design of a switching-mode dc–dc converter, the wide system bandwidth can be achieved by adopting the current-mode control method [2]–[7]. On top of that, an adaptive pole–zero position circuit has been proposed to instantly move the pole and zero pair of the compensation network to higher frequencies, in order to temporarily extend the bandwidth of the system during the transient event [2], [3]. The pole and zero are moved back immediately after the transient event to stabilize the system. However, a careful design targeting system stability during the whole process needs to be taken into consideration once the bandwidth is tentatively changed. Another commonly used method to improve the transient response is to increase of the slew rate of the error amplifier [8]–[11]. Different current-boosting modules are used to increase the source/sink current at the output of the error amplifier during the transient period. The required boosting current must be large enough to realize an obvious improvement on the transient response, and at the same time, it needs to avoid the over-response oscillation caused by the excessive boosting current. Moreover, current-boosting modules introduce more power consumption, which degrades the overall efficiency. Besides that, the use of nonlinear control is an alternative to realize fast transient response. For example, hysteresis control can offer immediate feedback during load variations. However, this method has a drawback—the high electromagnetic interference (EMI) noise due to its variable switching frequencies [12], [13]. Circuits can be added to lock the switching frequency and thus abate the EMI noise, but such additions bring more complexities into the circuit design [14]–[16].

In this paper, a multiloop control dc–dc converter is proposed, with an additional ac coupled feedback (ACCF) connecting between the outputs of the regulator and the transconductance as shown in Fig. 1. (The conventional current-mode buck dc–dc converter is highlighted with the blue dashed line.) Differing from the conventional type-III compensation network which contains three poles and two zeros to boost the phase to ensure stability, the proposed method generates the same number of poles and zeros to boost the mid-band gain to significantly enhance the response strength of the compensator, thus increasing the transient response. At the same time, the proposed scheme also helps to manage the output voltage ramping speed during the converter power-up. In other words, a soft-start function is inherently realized. The proposed novel ACCF is easy to implement, and yet demonstrates great performance in the experimental results.

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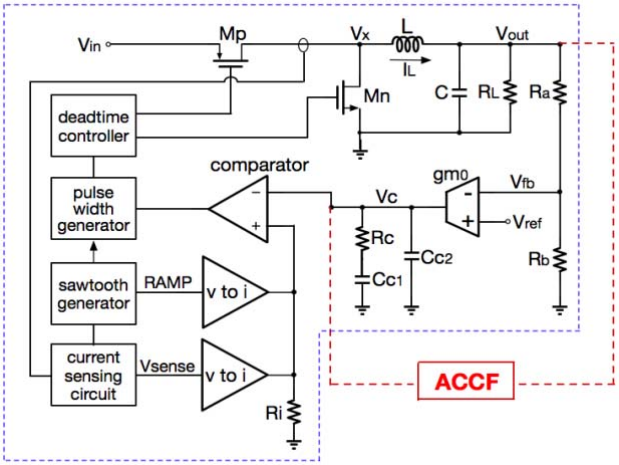

Fig. 1. Conventional current-mode buck converter with the proposed ACCF loop.

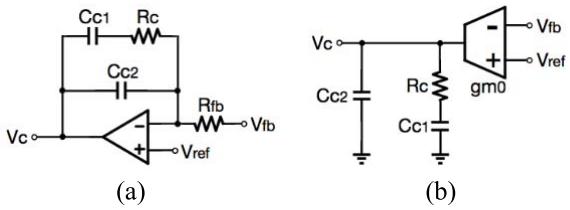

Fig. 2. Type-II compensation designs. (a) OpAmp–*RC* topology. (b) G_m–C topology.

The overall structure and operation principle of the proposed multiloop dc–dc buck converter will be briefly illustrated in Section II. Section III will describe the details of the circuit implementations of the proposed ACCF network and the several essential functional blocks. The experimental results of the dc–dc converter prototype will be presented and discussed in Section IV. Lastly, Section V will draw the conclusion based on the findings.

II. Operation Principle

Theoretically, the transient performance depends mainly on two factors—the response speed and the response strength. The former can be interpreted as the delay time from the load transient event to the change on the control signal, and the latter refers to the amount of the amplitude changes on the control signal. Taking the widely used type-II compensation design as an example here, the structure of the type-II compensation designs can be realized by either the operational amplifier–resistor–capacitor (OpAmp–*RC*) topology [as shown in Fig. 2(a)] or the transconductance–capacitor (G_m–C) topology [as shown in Fig. 2(b)]. During the load step, the variation in the output voltage results in a change in the feedback signal V_{fb}. The control signal V_c can only respond gradually, due to the compensator's integrating effect. Its response speed depends on the bandwidth of the compensator. Assuming an error voltage V_{err} turns up on the feedback, the amount of change of the control signal ($|\Delta V_c|$) from its steady-state level can be expressed in the following equations for the

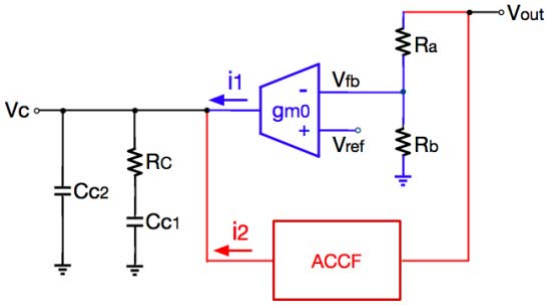

Fig. 3. Proposed compensation network.

OpAmp–*RC* and G_m–C topologies, respectively [1]:

$$\text{OpAmp}--RC: \quad |\Delta V_c| = \frac{R_c}{R_{\text{fb}}} V_{\text{err}} \tag{1}$$

$$G_m--C: \quad |\Delta V_c| = g_{m0} R_c V_{\text{err}} \tag{2}$$

where V_{err} stands for the error voltage that turns up on the feedback, g_{m0} is the transconductance of the g_{m0} cell, and R_{fb} and R_c are the resistors connected to the inverting input terminal of the OpAmp and the compensation resistor, respectively.

Obviously, a higher $|\Delta V_c|$ can cause larger adjustments on the duty signal, and therefore, it promotes the quicker recovery of the output. This explains how the response strength positively affects the load transient performance.

This paper utilizes a current-mode controller to improve the response speed aspect by increasing the system bandwidth in order to enhance the load transient response. On top of that, a novel ACCF is paralleled around the compensator to boost the response strength at the mid-band (as shown in Fig. 3), which is lacking in the conventional designs. The output impedances of both g_{m0} cell and ACCF are assumed to be infinity (which will be discussed in Section III). The transfer function of the conventional type-II compensation network can be expressed in (3) which includes two poles and one zero (located at p_1, p_2, and z_1, respectively). With the additional ACCF, three poles and two zeros will be generated (located at p_1', p_2', p_3', z_1', and z_2', respectively), and the newly generated poles and zeros will boost the compensation mid-band gain as derived in (4). The respective Bode plot can be found in Fig. 4 accordingly

$$\text{Without ACCF:} \quad \frac{v_c(s)}{v_{\text{out}}(s)} = \frac{\alpha(s - z_1)}{(s - p_1)(s - p_2)}$$
$$z_1 = \frac{1}{2\pi R_{c1} C_{c1}}$$
$$p_1 = 0$$
$$p_2 = \frac{1}{2\pi R_{c1} C_{c2}} \tag{3}$$

$$\text{With ACCF:} \quad \frac{v_c(s)}{v_{\text{out}}(s)} = \frac{\alpha'(s - z_1')(s - z_2')}{(s - p_1')(s - p_2')(s - p_3')} \tag{4}$$

where

$$v_c(s) = (i_1 + i_2) \frac{1 + R_c C_{c1} s}{s(C_{c1} + C_{c2}) \left(R_c \frac{C_{c1} C_{c2}}{C_{c1} + C_{c2}} s + 1 \right)}$$

$$i_1 = -g_{m0} \frac{R_b}{R_a + R_b} V_{\text{out}}$$

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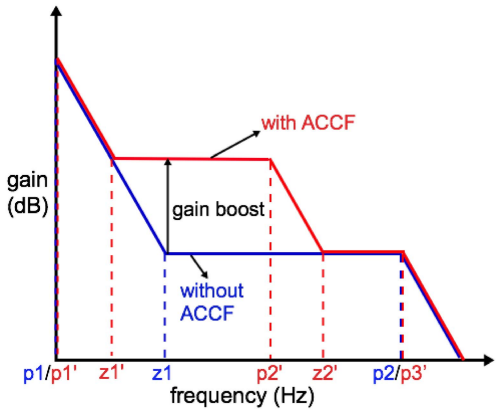

Fig. 4. Illustration of the Bode magnitude plot of the buck converter with ACCF versus without ACCF.

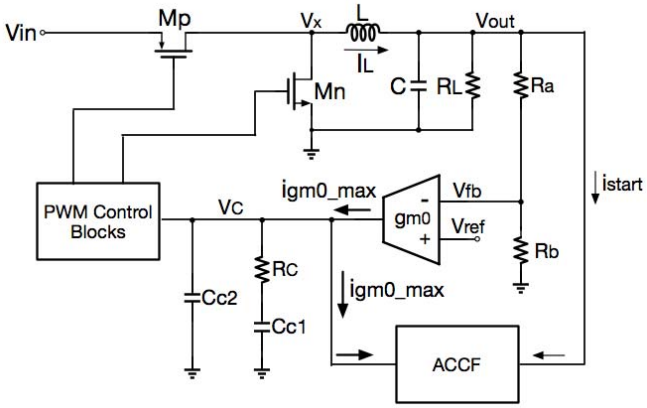

Fig. 5. Start-up response of the proposed controller.

where i_1 and i_2 are the output current from the g_{m0} cell and ACCF, respectively, α and α' are constant coefficients, R_a and R_b are the voltage divider series resistors connected at the output of the dc–dc converter, and C_{c1}, C_{c2}, and R_c are the compensation capacitors and resistor, as shown in Fig. 3.

Furthermore, the ACCF circuit also defines the output voltage rising slope during the converter power-up. The working principle of the soft-start function is illustrated in Fig. 5. During start-up, V_{out} is much lower than V_{ref}, so that the g_{m0} cell will be saturated with an extremely high output voltage V_c, which will program an unfavorable runaway inductor current. With the help of the ACCF circuit, in this case, the fast-rising voltage appearing at V_{out} caused by the in-rush start-up current is coupled through the ACCF and induces the ac current from V_c into the ACCF itself. As a result, V_c is pulled down to define the slow increase in the inductor current and output voltage. This particular inherent function of the proposed ACCF eliminates the need for a dedicated soft-start circuit in the conventional designs [17]–[20].

III. Circuit Implementation

A. Active Compensation Capacitor

Active capacitor has been proposed and used in the amplifier to amplify capacitance in [21]. In this paper, the large passive compensation on-chip capacitor C_{c1} is replaced by the equivalent active capacitor in the proposed buck converter to

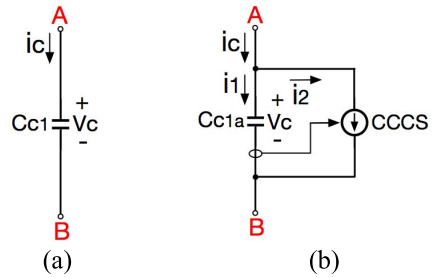

Fig. 6. Schematics of the equivalent capacitors. (a) Passive capacitor. (b) Active capacitor.

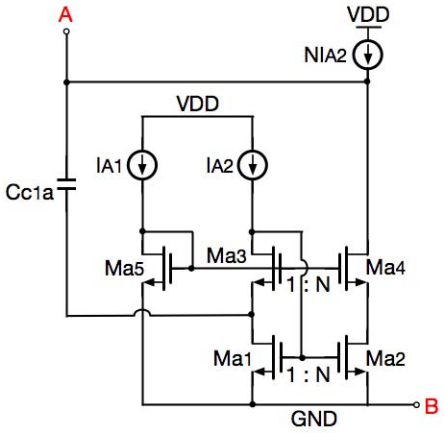

Fig. 7. Circuit implementation of the active capacitor.

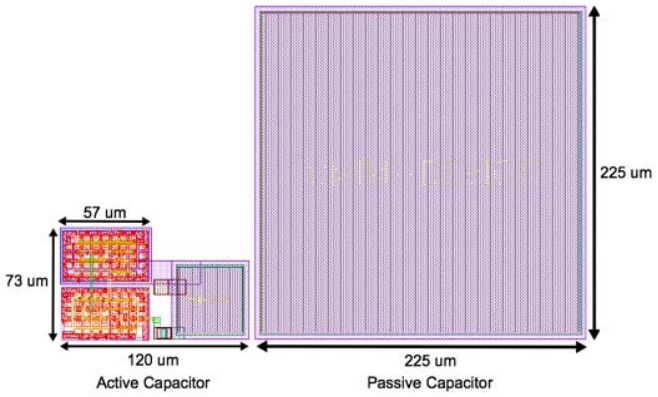

Fig. 8. Footprint of the active and passive capacitors ($N = 19$).

reduce the footprint, as shown in Fig. 6. The schematic of the active capacitor will be also modified and used in realizing the ACCF, which will be discussed later. Equations (5)–(7) explain the derivation of the equivalent active capacitor from the passive capacitor mathematically. The equivalent circuit of (7) is modeled in Fig. 6(b) as an active capacitor. The current mirror is used as the current control current source to amplify the ac current in this work. Fig. 7 shows the circuit implementation of the active capacitor by using the current mirror. A $(N + 1)$ times smaller passive capacitor is utilized in parallel with the current mirror, which has an amplification factor of N ($N = 19$ in this paper), to realize the same capacitance as C_{c1}($C_{c1} = 80$ pF in this paper). Fig. 8 shows an approximately seven-time-reduction in the silicon area with the use of the equivalent active capacitor. The higher the value of N, the smaller is the footprint of the active capacitor.

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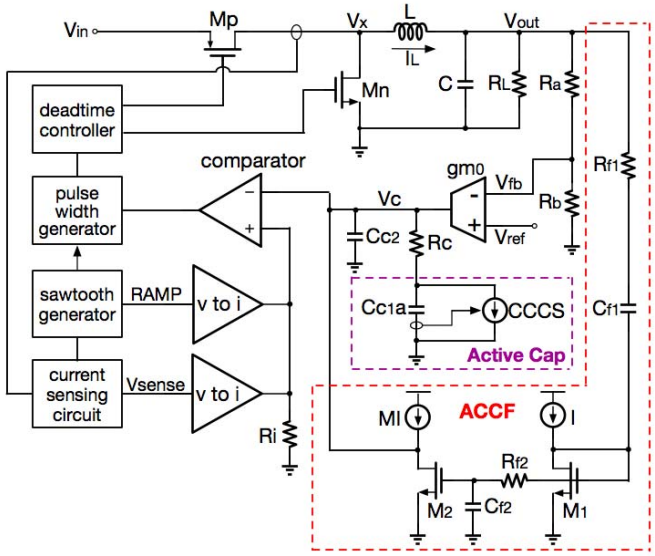

Fig. 9. Proposed current-mode buck converter.

Nevertheless, the higher N with higher quiescent current will increase the static power consumptions. As a result, N needs to be designed at an optimized value

$$\text{Passive capacitor } i_c = C_{c1}\frac{dV_c}{dt}. \tag{5}$$

Assume

$$C_{c1} = (N+1)\,C_{c1a} \tag{6}$$

$$i_c = (N+1)\,C_{c1a}\frac{dV_c}{dt} \tag{7}$$

where

$$NC_{c1a}\frac{dV_c}{dt} = i_2, \quad C_{c1a}\frac{dV_c}{dt} = i_1.$$

B. Multiloop Control for Transient Enhancement and Soft-Start

The main structure of the ACCF circuit is modified from the active capacitor circuit [21], [22], where an ordinary on-chip capacitor C_{f1} is ac coupled from V_{out}, amplified by the current mirror (transistor M_2-to-M_1 with the ratio M:1, M $>$ 1), and connected back to the main control loop at the g_{m0} cell output node, as shown in Fig. 9. The circuit implementation of the g_{m0} cell is shown in Fig. 10. Resistor R_{g_m} is inserted in between the source terminals of M_{P1} and M_{P2} to sense the voltage differences (ΔV) between the input terminals (V+ and V−) of the two super-source-followers; hence, g_{m0} of the cell will be inversely proportional to the value of R_{g_m}. The output current is generated by the two pairs of current mirrors formed by M_{P3}, M_{P4}, M_{N3}, and M_{N4} at the output stage, and it will charge the compensation network at the output of the g_{m0} cell. The mid-band gain ($A_{\text{mid-band}}$) of the g_{m0} cell is, therefore, proportional to R_c while inversely proportional to R_{g_m}, as expressed in (8). Eventually, the process, voltage and temperature variations of the two resistors are effectively canceled. Nevertheless, R_c should be placed close to R_{g_m} in the layout for a better matching purpose

$$A_{\text{mid-band}} \propto \frac{R_c}{R_{g_m}} \tag{8}$$

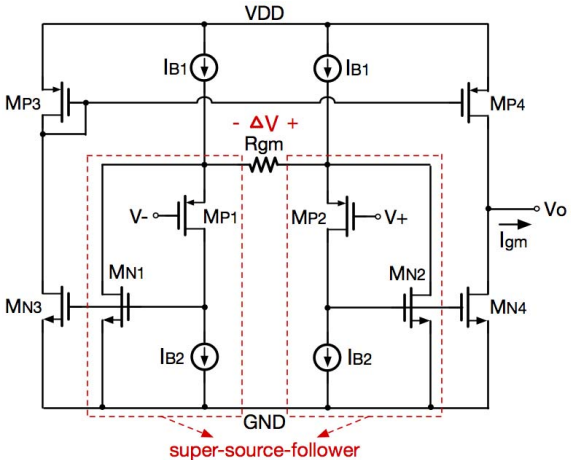

Fig. 10. Schematic of the g_{m0} cell.

where R_c is the resistor in the compensation network at the output of the g_{m0} cell, and R_{g_m} is the resistor in between the sources of M_{P1} and M_{P2}.

The circuit implementation of the proposed ACCF realizes fast transient response as well as soft-start, which are analyzed in three aspects in the following.

1) Soft-Start Analysis: With the help of the ACCF, the fast-rising voltage appearing at V_{out} caused by the start-up in-rush current will be coupled through C_{f1}. Then, an ac current will be induced into the transistor M_1. The M_2-to-M_1 current mirror is able to amplify the induced current and pull it from V_c; therefore, V_c is adjusted to a lower level. Consequently, V_c, inductor current, and V_{out} are well managed by the current control loop. The controllable soft-start slope is expressed in the following equation:

$$V_{\text{out}}\text{Soft-start Slope} = \frac{I_{\text{gm0\_max}}}{MC_{f1}} \tag{9}$$

where $I_{\text{gm0\_max}}$ is the maximum output current of the g_{m0} cell, M is the current ratio of transistor M_2-to-M_1, and C_{f1} is the capacitor in the proposed ACCF.

2) Steady-State Analysis: The ACCF path is virtually disconnected from V_{out} during the steady state. The low pass filter $R_{f2}C_{f2}$ is added to prevent the V_{out} ripples from passing through the ACCF path and disturbing V_c. It is designed to cut off around the converter's switching frequency. Although there is no current flowing between the g_{m0} cell and the ACCF circuit, the output impedance of the g_{m0} cell is reduced due to the ACCF output stage. The advanced current mirror with high output impedance should be considered on condition that a large dc loop gain is preferred [23], [24].

3) Transient Analysis: As discussed previously, the load transient performance is improved on account of the gain boosting effect around the compensator's mid-band. This can be understood analytically by deriving the transfer function from the small-signal equivalent circuit, as shown in Fig. 11(a). The transconductance of the transistors M_1 and M_2 are labeled as g_{m1} and g_{m2} ($g_{m2} = Mg_{m1}$), and R_O represents the combined output impedances of the g_{m0} cell and the ACCF. The original single-loop compensation capacitor C_{c1} still determines the dominant pole in this multiloop network. As the

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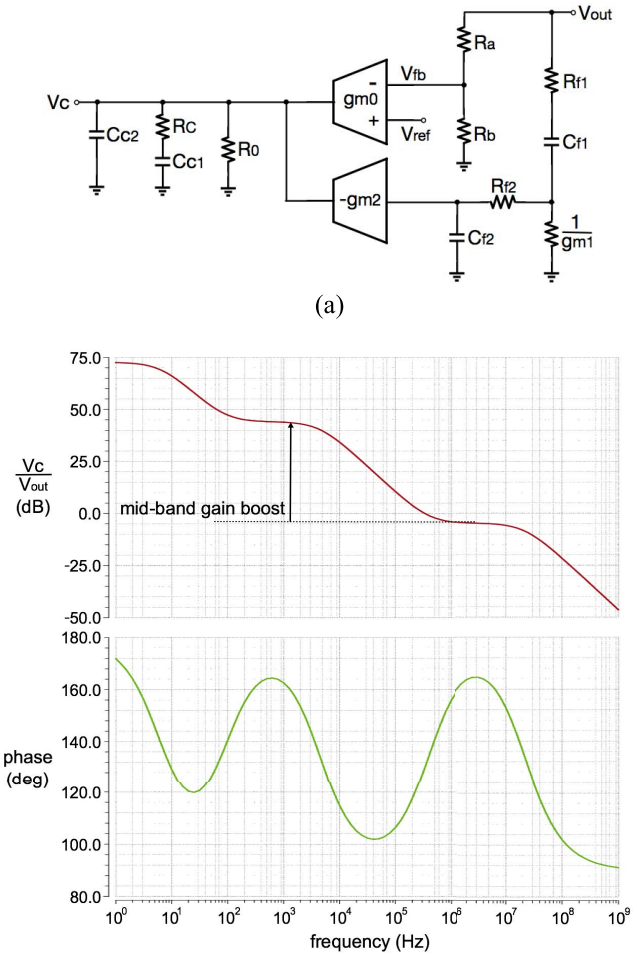

Fig. 11. Proposed compensation network. (a) Small-signal equivalent circuit. (b) AC Bode plot.

frequency increases, capacitor C_{f1} feeds the V_{out} information into the ACCF circuit, which brings about a gain boosting over the mid-band. The transfer function is expressed in (10), which matches the simulation waveforms as shown in Fig. 11(b). It seems that only a small frequency range is covered by the gain boosting effect over the mid-band (due to the logarithmic scale). Nonetheless, it is the most crucial band that supports the load transient

$$\frac{V_C}{V_{\text{out}}} = -\frac{g_{m0}R_0R_b(C_{c1}R_Cs+1)(hs^2+ks+1)}{(R_a+R_b)(as^2+bs+1)(ps^2+qs+1)} \quad (10)$$

where

$$a = C_{c1}C_{c2}R_0R_C$$

$$b = C_{c1}R_0 + C_{c2}R_0 + C_{c1}R_C$$

$$h = p = \frac{C_{f1}C_{f2}(R_{f1}+R_{f2}+R_{f1}R_{f2}g_{m1})}{g_{m1}}$$

$$k = \frac{(R_a+R_b)C_{f1}M}{R_bg_{m0}} + \frac{C_{f1}+C_{f2}}{g_{m1}} + C_{f1}R_{f1} + C_{f2}R_{f2}$$

$$q = \frac{C_{f1}+C_{f2}+C_{f1}R_{f1}g_{m1}+C_{f2}R_{f2}g_{m1}}{g_{m1}}.$$

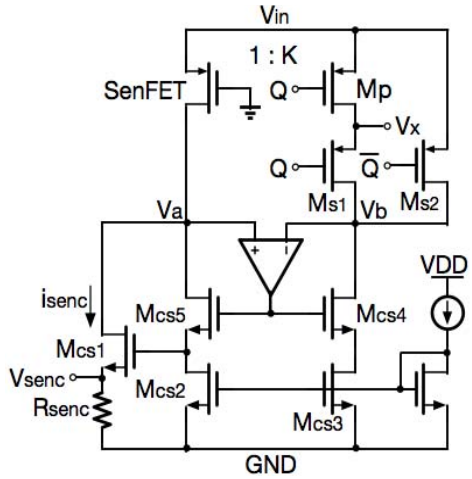

Fig. 12. Conventional current sensor [4].

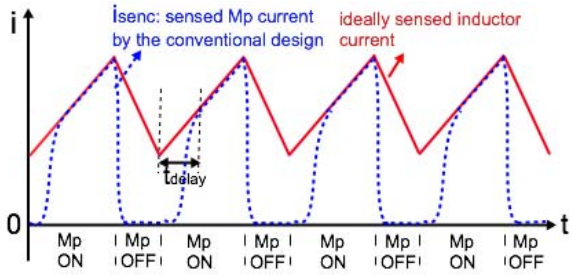

Fig. 13. Waveforms of i_{senc} (blue dashed line) and the ideally sensed inductor current (red solid line).

C. Continuous-Sensing-Technique for Fast-Response Current Sensor

The current sensor has been used to sense the inductor current in the current-mode dc–dc converter [4], [5], [25], [26]. The conventional design is shown in Fig. 12 where a sense FET (SenFET) is implemented to sense the current passing through the high side power FET M_P at the ratio of k to 1 ($k \gg 1$). M_P and M_{s1} are switched ON simultaneously when the gate control signal Q is low. Meanwhile, the current sensor works in the "active sensing mode" and the SenFET keeps tracking the current passing through M_P using an almost equalized drain-to-source voltage level. In the other words, V_a is adaptively adjusted to V_b through the feedback of OpAmp. The outputs of the current sensor are i_{senc} and V_{senc}, which represent the sensed current and voltage with the required ratios, respectively.

Alternatively, V_b will be at the same voltage level as V_{in} in the case where M_{s2} is switched ON by the high Q signal ($\bar{Q}$ connected at the gate of M_{s2} represents the complement signal of Q). In this situation, V_b equals to V_{in} as well as V_a, the output sensed current i_{senc} is negligible. The OpAmp is in its "sleeping mode." The current sensor will only change back to the "active sensing mode" once Q switches from high to low in the next switching phase, which means that the OpAmp is required to "wake up" instantly thus to accurately sense the current passing through M_P by tracking the changes at node V_b. However, the reaction time that the OpAmp needs to

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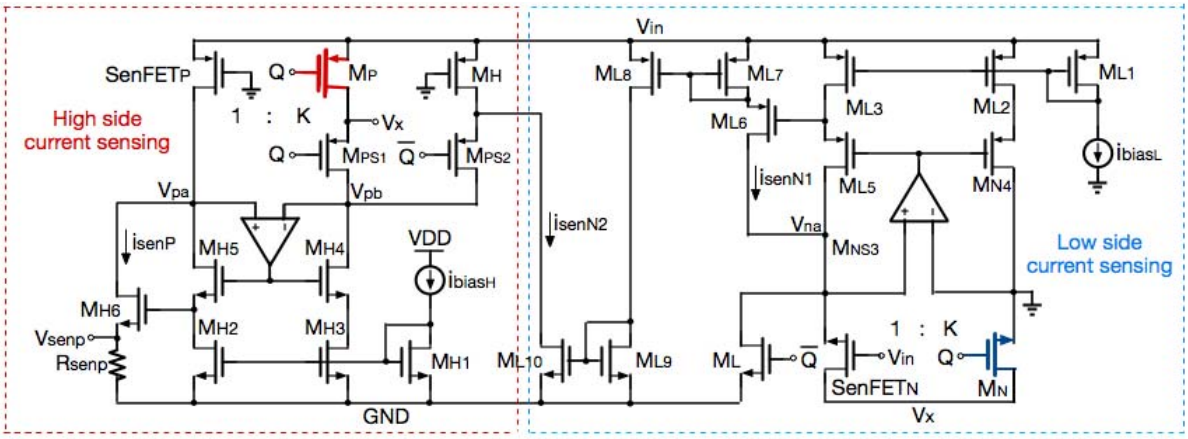

Fig. 14. Proposed continuous-sensing current sensor.

adjust itself from one set of dc operating points to the other must be considered. It causes delays (t_{delay}) at the beginning of every sensing stage as illustrated in Fig. 13—the blue dashed line represents the sensed M_P current by the conventional current sensor and the red solid line represents the ideally sensed inductor current. Obviously, the problem will become more severe when the on-time of M_P is short.

To solve the stated problem, a continuous-sensing-technique is proposed to sense the current passing through M_P without any delay (t_{delay}). As shown in Fig. 14, the proposed current sensor consists of two sensing stages, namely, the high side current sensing stage (which senses the power PMOS M_P drain current when Q is low) and the low side current sensing stage (which senses the power NMOS M_N drain current when Q is high). The low side sensed M_N current (i_{senN2}) will be connected to the high side current sensing stage through M_H and M_{PS2}. With that, the high side current sensing stage senses the M_P drain current when Q is low. M_{ps2} will be turned ON and the current introduced by the low side current sensor (i_{senN2}) will be connected to the high side current sensing stage once M_{ps1} is switched OFF when Q is high. With this additional current source, the high side current sensing stage will continuously be active and sense the current i_{senN2} by tracking V_{pa} to V_{pb}. M_{ps2} will be switched OFF while M_{ps1} and M_p are switched ON when Q changes to low, and the power MOSFET sensing mode will then be active again. There is no delay in between the two switching phases because the two input nodes of the OpAmp (V_{pa} and V_{pb}) are continuously well-controlled, so do the dc operating points. Since no "wake up" time is needed, there is no delay for the high side current sensing stage. The delay at the low side current sensing stage will not affect the sensing accuracy in the peak current-mode control. The simulation results can be found in Fig. 15. The output voltage/current ($V_{\text{senp}}/I_{\text{senp}}$) of the current sensor is proved to have negligible delays.

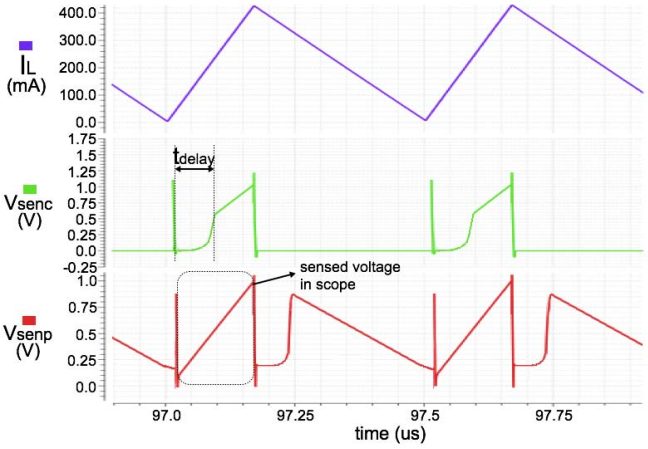

Fig. 15. Simulated waveforms of the inductor current (purple waveform), the output voltage of the conventional current sensor (green waveform), and the proposed current sensor (red waveform).

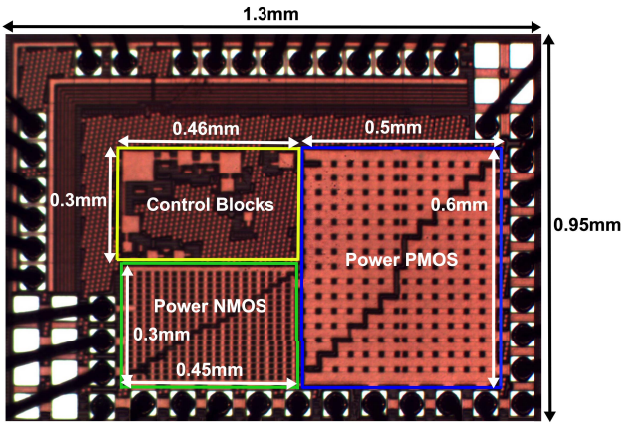

Fig. 16. Micrograph photograph of the proposed buck dc–dc converter.

IV. Experimental Results

The proposed current-mode buck dc–dc converter was fabricated using a standard 0.18-μm CMOS process, and the chip's micrograph is shown in Fig. 16. The total footprint occupies an active silicon area of 0.573 mm^2, in which the power transistors occupy an area of 0.435 mm^2 and the controller takes up an area of 0.138 mm^2. The designed converter can be powered with the Li-ion battery of input voltage range from 2.7 to 4.2 V, and a voltage output of 1.2–2.5 V. The experi-

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TABLE I

EXPERIMENTAL PARAMETRIC PERFORMANCE OF THE CURRENT-MODE BUCK CONVERTER

Parameter	Value
Input voltage (V_{in})	2.7 V-4.2 V
Output voltage (V_{out})	1.2 V-2.5 V
Inductor/Capacitor	1.5 µH/10 µF
Maximum output current	1 A
Switching frequency	1 MHz-2 MHz
Steady state output voltage ripple	23 mV
Maximum efficiency	94% @300 mA
Load regulation	0.018 mV/mA
Line regulation	0.0056 mV/mV
Total die size	1.235 mm^2
Soft-start delay	1.05 ms

mental parametric performance is summarized in Table I. The following results are obtained using 3.8-V input voltage and 1.8-V output voltage with a switching frequency of 1.5 MHz unless otherwise stated.

A variable resistor was connected at the output of the converter in series with a switch to measure the load transient performance. The 1-kHz switching frequency of the switch ensures the periodic change to a different load current on the top of the existing load. Fig. 17 shows the load transient response of the prototype in different conditions. The output recovers very quickly despite the variations of output voltage and load steps. The settling times are 6 μs/5.5 μs with output voltage overshoot/undershoot of 35 mV/28 mV, respectively, as shown in Fig. 17(a), when the converter operates under 500-mA-load step and 1.8-V output voltage. The recovery time is also proven to be as short as 5.5 μs with 30-mV output voltage ripple [as shown in Fig. 17(b)], when the output voltage decreases to 1.2 V. Even with a higher load step of 1 A, the output voltage overshoot and undershoot are both kept at small values of 60 mV, and the corresponding recovery times are 9.5 and 9.4 μs, respectively, as shown in Fig. 17(c). At the same time, an excellent load regulation of 0.018 mV/mA is obtained for a load current step from 50 μA to 1 A in 1 μs, which can be observed from Fig. 17(c).

Fig. 18 shows the measured performance of the output voltage V_{out} and the inductor current I_L during the start-up period. It can be seen that V_{out} gradually ramps up and settles at 1.8 V within approximately 1050 μs with well-controlled I_L. The steady-state performances of the proposed converter are shown in Figs. 19 and 20. The former shows the measured waveforms of the inductor current and the output voltage when the input voltage is 3.3 V, and the latter shows the same parameters when the input voltage is 4.2 V. The experimental results indicate an excellent line transient of 0.0056 and the output voltage ripples of 23 mV in the steady state. The efficiency as a function of load current can be found in Fig. 21. A peak efficiency of 94% at 300 mA has been achieved.

Table II illustrates the comparison of the performance of the proposed converter with respect to prior arts. The proposed

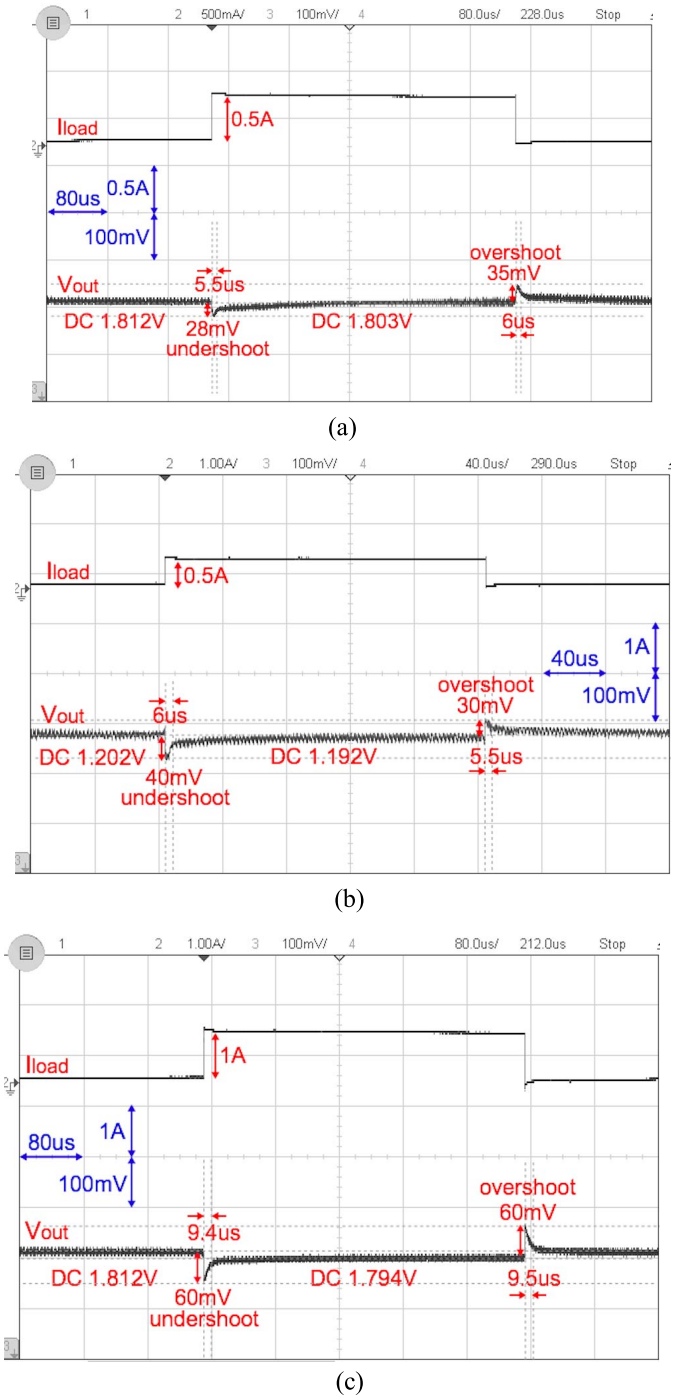

Fig. 17. Measured load transient response when V_{in}=3.8 V. (a) Load steps from 50 μA to 500 mA in 1 μs at 1.8-V output voltage. (b) Load steps from 50 μA to 500 mA in 1 μs at 1.2-V output voltage. (c) Load steps from 50 μA to 1000 mA in 1 μs at 1.8-V output voltage.

converter is among the best in overall performance, as shown in Table II. Compared to the work done in [7] and [30], the higher output overshoot/undershoot voltage is mainly due to the shorter load transient step time. (The load transient steps are 0.5 A/1 μs and 1 A/1 μs in this paper, while the load transient steps are 0.4 A/3 μs and 0.45 A/5 μs in [7] and [30], respectively.) Furthermore, it has a shorter recovery time than [7]. Despite the fact that the works conducted

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TABLE II
COMPARISON OF THE CHARACTERISTICS OF THE PROPOSED DC–DC CONVERTER WITH RESPECT TO PRIOR ARTS

	This work		[6] 2017	[27] 2016	[28] 2015	[13] 2013	[29] 2013	[3] 2012	[30] 2012	[7] 2012	[31] 2010
CMOS Technology (μm)	0.18		0.35	0.35	0.35	0.18	0.35	0.35	0.18	0.25	0.35
Control mechanism	Current-mode PWM		Current-mode PWM	DT-DSM	Voltage-mode PWM	Hysteresis	Adaptive on-time	Current-mode PWM	Digital PWM	Current-mode PWM	Voltage-mode PWM
Inductor (μH)	1.5		4.7	4.7	4.7	4.7	4.7	4.7	10	4.7	4.7
Capacitor (μF)	10		4.7	4.7	10	47	8.9	10	10	10	4.7
Input voltage (V)	2.7-4.2		2.7-4.2	3.6-5	1.8-3.6	0.9-1.5	3.3-4.2	2.7-3.6	1.8-3.3	2.7-4.3	2.5-3.5
Output voltage (V)	1.2-2.5		1.8	1-3	1-2.5	0.3-0.9	1.2	2	1.2	1.8	0.8-2.4
Max. load current (A)	1		0.6	0.5	0.3	0.32	0.8	0.5	0.5	0.5	0.6
Switching frequency (MHz)	1.5		1	5.12	1	1	0.75	1	1	1.5	1
Peak efficiency (%)	94		95	89	95.78	91.5	86.6	93	92	N.A.	97
Load transient step (A)	0.5	1	0.4	0.27	0.16	0.32	0.745	0.4	0.45	0.4	0.5
V_{out} overshoot/ undershoot (mV)	35/28	60/60	76/88	100/100	40/40	75/150	75/75	38/60	15/15	10/10	80/80
Recovery time (us)	6/5.5	9.5/9.4	2.6/2.4	10/10	2/2	11/5	3.6/3.6	12/6	4/4	20/20	7/7
Load regulation (mV/mA)	0.018		N.A.	N.A.	0.02525	0.083	N.A.	N.A.	0.011	0.025	0.016
Line regulation (mV/mV)	0.0056		N.A.	N.A.	0.0088	0.0034	N.A.	N.A.	0.004	0.027	0.003
Additional function	Soft-start		N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
Chip area (with PADs) (mm^2)	1.235		2.242	2.21	2.25	1.648	1.9	3.8	1 (active area)	1.65	1.375
*FOM (%)	8.15		11.3	419	23.5	621	11.4	51.8	13.3	35.3	24.7

$$*FOM = \frac{fLC(t_{HtoL}+t_{LtoH})(V_{ovr}+V_{udr})}{4I_{step}}$$

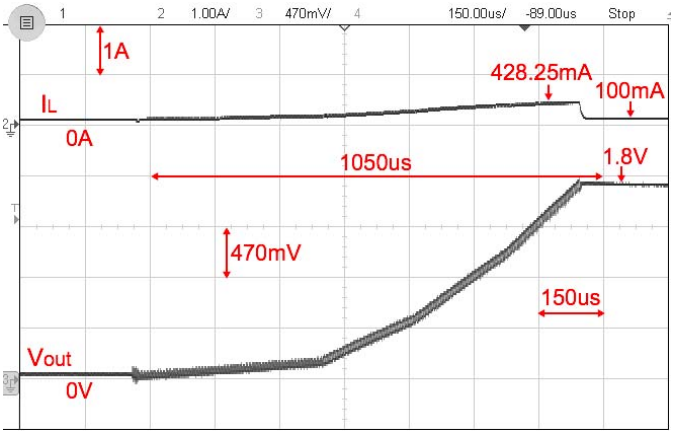

Fig. 18. Measured waveforms of the proposed soft-start.

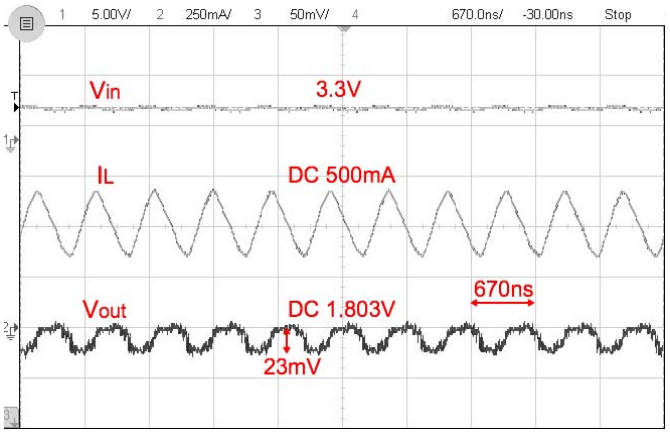

Fig. 19. Steady-state measurement when V_{in}=3.3 V, I_L=500 mA, and V_{out}= 1.8 V.

in [6], [28], [29], and [30] had faster recovery times than the proposed converter, they were either tested with smaller load transient steps, used nonlinear control methods, or suffered from higher output overshoot/undershoot voltage. Therefore, the figure of merit (FOM) is designed in (11) which takes into consideration major factors such as switching

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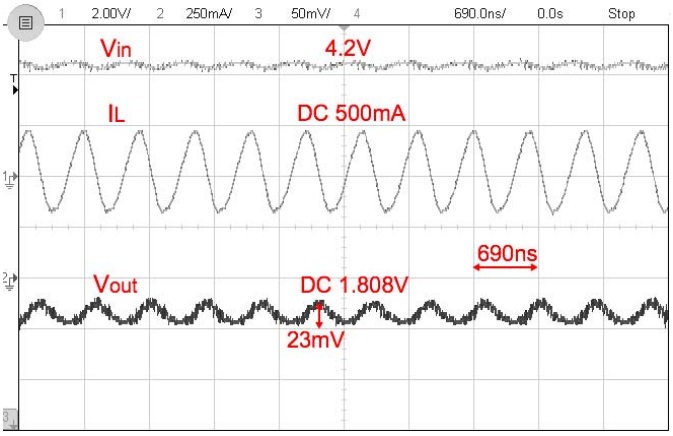

Fig. 20. Steady-state measurement when V_{in}=4.2 V, I_L=500 mA, and V_{out}= 1.8 V.

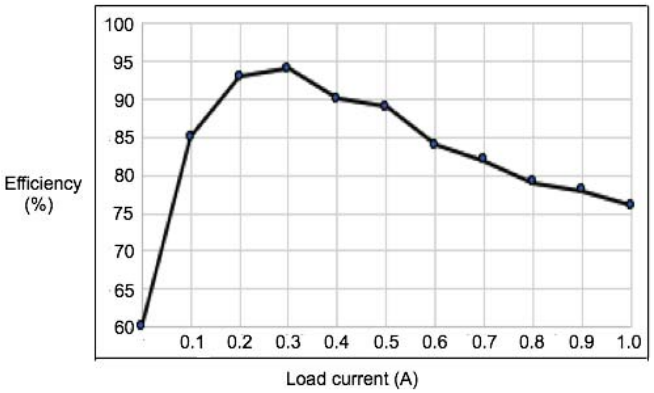

Fig. 21. Conversion efficiency plot when $V_{\text{in}} = 3.8\ V$ and V_{out}= 1.8 V.

frequency (f, MHz), capacitor (C, μF), inductor (L, μH), load step (I_{step}, mA), output voltage overshoot/undershoot ($V_{\text{ovr}}/V_{\text{udr}}$, mV), and the corresponding recovery time ($t_{\text{HtoL}}/t_{\text{LtoH}}$, μs), and directly describes the comprehensive performance of a dc–dc converter. The smaller the FOM, the better is the evaluation of the performance. The proposed converter not only possesses the lowest FOM value but also achieves excellent load and line regulations. Furthermore, the chip occupies the smallest footprint among the studies in Table II. It is experimentally proven to realize the soft-start function inherently, which usually requires an additional start-up circuit in [17]–[20]

$$\text{FOM} = \frac{fLC(t_{\text{HtoL}} + t_{\text{LtoH}})(V_{\text{ovr}} + V_{\text{udr}})}{4I_{\text{step}}}. \tag{11}$$

V. Conclusion

A compact fast transient response current-mode buck converter with inherent soft-start is presented in this paper. Experimental results show that the designed converter can achieve a fast load transient response under different load current steps (500 mA and 1 A) with different output voltages (1.2 and 1.8 V). The soft-start period of more than 1 ms is also inherently realized. The controller is simple to implement, and yet demonstrates great performance in both load and line regulations. The proposed converter is appropriate for applications which necessitate the fast transient response over a large load range, especially for use in conjunction with microprocessors.

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