Many-Objective Sizing Optimization of a Class-C/D VCO for Ultralow-Power IoT and Ultralow-Phase-Noise Cellular Applications

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***Abstract*— In this paper, the performance boundaries and corresponding tradeoffs of a complex dual-mode class-C/D voltage-controlled oscillator (VCO) are extended using a framework for the automatic sizing of radio frequency integrated circuit blocks, where an all-inclusive test bench formulation enhanced with an additional measurement processing system enables the optimization of "everything at once" toward its true optimal tradeoffs. VCOs embedded in the state-of-the-art multistandard transceivers must comply with extremely high performance and ultralow power requirements for modern cellular and Internet of Things applications. However, the proper analysis of the design tradeoffs is tedious and impractical, as a large amount of conflicting performance figures obtained from multiple modes, test benches, and/or analysis must be considered simultaneously. Here, the dual-mode design and optimization conducted provided 287 design solutions with figures of merit above 192 dBc/Hz, where the power consumption varies from 0.134 to 1.333 mW, the phase noise at 10 MHz from −133.89 to −142.51 dBc/Hz, and the frequency pushing from 2 to 500 MHz/V, on the worst case of the tuning range. These results pushed this circuit design to its performance limits on a 65-nm CMOS technology, reducing 49% of the power consumption of the original design while also showing its potential for ultralow power with more than 93% reduction. In addition, worst case corner criteria were also performed on the top of the worst case tuning range optimization, taking the problem to a human-untrea table LXVI-D performance space.**

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***Index Terms*— Dual-mode voltage-controlled oscillator (VOC), electronic design automation (EDA), many-objective optimization, multitest bench sizing optimization, radio frequency (RF) integrated circuits (ICs).**

I. Introduction

VOLTAGE-CONTROLLED oscillators (VCOs) play a key role in modern radio frequency (RF) integrated circuit (IC) multistandard transceivers and, therefore, are subject to continuous research efforts that push the boundaries of their multifaceted performance/power efficiency in the state-of-the-art applications and integration technologies [1]–[5]. Usually, different wireless systems have various requirements for the VCO performance. For Internet of Things (IoT) applications, the VCO should maintain a low power consumption, while the phase noise performance can be quite relaxed, e.g., −102 dBc/Hz at 2.5-MHz offset for the Bluetooth low-energy receiver at 2.4-GHz carrier frequency [6]. On the other hand, the cellular applications require very stringent phase noise performance, e.g., −162 dBc/Hz at 20-MHz offset at 900-MHz carrier frequency for the Global System for Mobile transmitter (TX) [7] and −160 dBc/Hz at 30-MHz offset at ∼2-GHz carrier frequency for the long-term evolution/wideband code division multiple access TX [8].

The design of VCOs is usually time-consuming, even after a particular architecture has been selected. In addition to the phase noise and power consumption, other specifications such as the frequency tuning range and frequency pushing due to the supply voltage variation also need to be carefully considered in a practical design. According to the time-variant phase noise model [9], for a typical voltage-biased VCO employing cross-coupled nMOS transistors (Fig. 1) oscillating at ω_0, its phase noise at offset frequency $\Delta\omega$ can be expressed as [1], [2]

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{\Gamma_{T,\text{rms}}^2}{QV_P^2}\cdot\frac{kT}{C}\cdot F\cdot\frac{\omega_0}{(\Delta\omega)^2}\right] \quad (1)$$

where Q is the tank quality factor, V_P is the differential output amplitude, C is the total tank capacitance, $\Gamma_{T,\text{rms}}$ is the rms impulse sensitivity functions of the parallel resistance representing the conversion from tank thermal noise to phase noise, and F is the noise factor defined by the ratio between the total phase noise and the phase noise induced by the tank loss. To meet the phase noise requirement at a certain frequency,

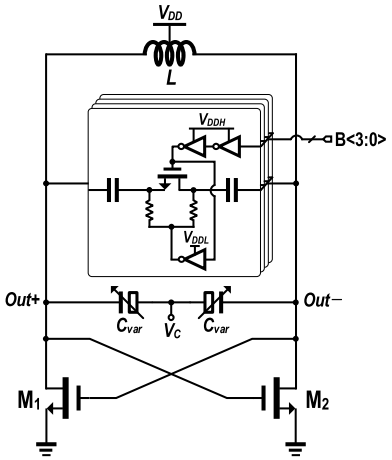

Fig. 1. Dual-mode class-C/D VCO schematic with SCA for an increased tuning range.

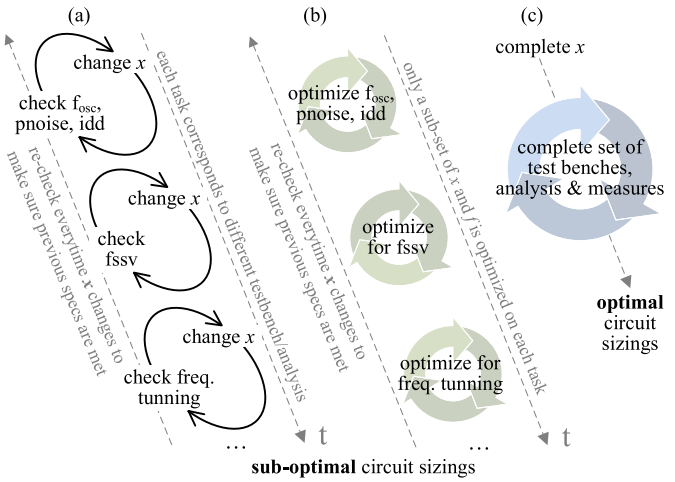

Fig. 2. (a) Knowledge-based manual design. (b) Mixed iterative/sequential optimization design approach. (c) Adopted optimize "everything-at-once" approach, where $\boldsymbol{x}$ is the design variables' array.

a proper tank capacitance C and inductance L need to be chosen. However, it is difficult to obtain accurate values for C and L using (1) since the values of F depend on the working mode of M_1/M_2, related to the gate-biasing voltage and transistor sizes. If taking the noise contributions for the transistor channel conductance (G_{DS}) into consideration [2], the situation becomes even more complex. Furthermore, for each iteration, when the L value is changed, the switched-capacitor array (SCA) and varactors also need to be redesigned to meet the frequency-tuning range requirement, which would change the tank Q and, in turn, affect the phase noise performance. In the practical design, even more iterations are required to guarantee satisfactory VCO performances in the presence of process, voltage, and temperature variations. The recent works [3], [4] also reveal that the phase noise and frequency pushing can be improved by utilizing the common-mode resonance at the double-oscillation frequency, which requires extra design efforts to balance the differential-mode and common-mode tank inductances and capacitances. Thus, numerous nonsystematic iterations are inevitable to attain high-quality designs.

In this context, this paper describes an electronic design automation (EDA) tool and methods used to bypass the difficulties faced while sizing complex RF IC blocks. This paper is organized as follows. In Section II, we conduct a brief state-of-the-art review on automatic RF IC sizing tools and particularly applied to the VCO design, and also discuss the innovative contributions of this paper. In Section III, we overview the optimization-based IC sizing and all-inclusive test bench concepts. In Section IV, we describe the automatic design methodology, including the postprocessing of the measurements. Then, in Section V, we provide the complete setup adopted for the class-C/D VCO as well as the optimization results. In Section VI, we carry a comparison with the mixed iterative/sequential optimization approach, and finally, in Section VII, we address the conclusions.

II. Related Works and Contributions

To overcome the difficulties found on the manual sizing of RF IC blocks, different optimization-based sizing approaches were developed [10], [11]. These EDA tools use algorithms that efficiently explore the design space, instead of iterating over designer-defined analytical equations [12]. They can be applied over performance models that capture several circuits and inductor characteristics of the RF circuits and, particularly, VCOs such as in [13]; however, the use of foundry-provided device models and a circuit simulator as an evaluation engine, i.e., simulation-based sizing, proved to be the most accurate and widely adopted approach for RF [14]–[19], despite its increased computational effort. There are several commercially available solutions, e.g., Cadence's Virtuoso GXL [20] or MunEDA's DNO/GNO [21] that also follows the simulation-based architecture, and while useful, most of these tools still take a limitative single-objective approach being used mostly to adjust the manual sizing in a semiautomated manner. Therefore, these simulation-based methodologies are continuously subject to research efforts by the research community to cope with the most recent design challenges [22]–[24].

Developed methodologies are usually applied to simpler VCO topologies for a small number of design variables and considering only a small set of performance figures. To exemplify, in [19], the cross-coupled double-differential VCO was optimized for a 4-D performance space (oscillation frequency f_{osc}, phase noise, power, and oscillation amplitude Osc_{Amp}). The optimization was done on a 7-D design variable space. On the other hand, in [23], the VCO was optimized for a 9-D performance space (frequency-tuning range, phase noises, power, Osc_{Amp}, and area). In this case, a 9-D design variable space was considered. In other works [16]–[18], the performance and design variable spaces are similar, and hardcoded formulas are used to compute other metrics, e.g., figure of merit (FOM). Following, when faced with a complex real-world VCO design, designers in both academic and industrial environments end up using EDA tools to solve only subproblems of the manual design, i.e., change only a subset of the design variables $\boldsymbol{x}$ to tackle local optimization (LO) targets, as illustrated in Fig. 2(b). This mixed iterative/sequential optimization design approach leads

to suboptimal solutions, as the tradeoffs between conflicting performance figures are not properly weighted. Therefore, for modern VCO applications, this approach does not fit, as more complex topologies and a wider set of requirements must be balanced simultaneously, e.g., multimode operation, digitally controlled frequency-tuning ranges, or attain a limited frequency pushing due to supply voltage variation.

This paper applies and adapts an EDA framework to bypass the difficulties faced on the sizing of complex RF IC blocks and, particularly, a dual-mode class-C/D VCO. The major contributions of this paper can be summarized as follows.

1) Adoption of an EDA framework to fully optimize a complex class-C/D VCO for the state-of-the-art IoT and cellular specifications.
2) Study and discussion of the possibility to meet extreme operational requirements in a single optimization run with the same framework setup, by analyzing the complete tradeoffs between power consumption, phase noise, and frequency pushing, obtained with a many-objective optimization. A study that is impossible to perform using commercially available solutions.
3) Unlike previous research works in VCO sizing optimization, here, the circuit's performance space greatly surpasses what can be found on EDA solutions in the literature. Two human-untreatable 18-D and 66-D performance spaces, defined over two different modes, i.e., worst case mode in typical conditions and worst case mode in worst case corner (WCC) conditions, respectively, for the same 28-D design variable space that affects the sizing of 43 devices (RF and digital components).
4) The adopted automatic design methodology is built over the established all-inclusive test bench formulation for optimization-based RF IC sizing but enhanced with parsers for the native output formats of most widely used off-the-shelf simulators and a comprehensive set of post-processing options. As such, the proposed formulation enables the optimize "everything-at-once" approach of Fig. 2(c), leading to a more systematic design flow that reduces the risk of bad design decisions while balancing all the design challenges simultaneously.

III. Preliminaries

This section reviews important concepts for analog and RF IC automation, i.e., the optimization-based sizing and all-inclusive test bench formulation.

A. Optimization-Based Rf Ic Sizing

In the traditional optimization-based sizing, the kernel is responsible for proposing P different sizing solutions for circuit simulation, each one with a new set of $\boldsymbol{x}$ design variables (e.g., devices' widths, lengths, and number of fingers) and is set to solve the constrained many-objective problem

$$\begin{aligned} &\text{find } x \text{ that min } f_m(x) \quad m = 1, 2, \ldots M \\ &\qquad \text{s.t. } g_j(x) \geq 0 \quad j = 1, 2, \ldots J \\ &\qquad\quad x_i^L \leq x_i \leq x_i^U \quad i = 1, 2, \ldots N \end{aligned} \tag{2}$$

where $\boldsymbol{x}$ is the vector of N design variables, $g(x)$ is the J constraint functions, and the output is a Pareto-optimal front (POF) representing the tradeoffs between M objective functions $f(x)$. In this problem, the number of design variables defines the search space order, while the variable ranges (minimum, maximum, and step values) define the size of the search space.

B. All-Inclusive Test Bench Optimization

The circuit design specifications s are traditionally formulated as

$$\begin{aligned} s_j^L(x) &= p_i(x) \geq P_j^L \quad j = 1, 2, \ldots, L, \ i \in \{1, 2, \ldots A\} \\ s_j^U(x) &= p_i(x) \leq P_j^U \quad j = 1, 2, \ldots, U, \ i \in \{1, 2, \ldots A\} \end{aligned} \tag{3}$$

where a set of LB lower bounds P_j^L and UB upper bounds P_j^U for some of the A-circuit performance characteristics $p_j(x)$ are imposed during optimization. The previous formulation applies directly only if the performance characteristics $p_j(x)$ match the measured values m_i [25]. However, for a complex set of performance figures, some $p_j(x)$ are functions of multiple measurements that are obtained from the wide range of alternative parameterized test setups (test benches), each running multiple analysis that need to be evaluated for each new set of $\boldsymbol{x}$. Therefore, the problem is reformulated as

$$f_m(x) = \begin{cases} p_m\left(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots\right) \\ \qquad \text{when minimizing } p_m(\ldots) \\ -p_m\left(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots\right) \\ \qquad \text{when maximizing } p_m(\ldots) \end{cases}$$

$$g_j^L(x) = \begin{cases} p_i\left(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots\right) \\ \qquad \text{when } s_j^L(x) \text{ is } p_i(\ldots) \geq 0 \\ \dfrac{p_i\left(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots\right) - P_j^L}{\left|P_j^L\right|} \\ \qquad \text{when } s_j^L(x) \text{ is } p_i(\ldots) \geq P_j^L \end{cases}$$

$$g_j^U(x) = \begin{cases} -p_i\left(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots\right) \\ \qquad \text{when } s_j^U(x) \text{ is } p_i(\ldots) \leq 0 \\ \dfrac{P_j^U - p_i\left(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots\right)}{\left|P_j^U\right|} \\ \qquad \text{when } s_j^L(x) \text{ is } p_i(\ldots) \leq P_j^U \end{cases} \tag{4}$$

with $k1, k2, \ldots \in \{1, 2, \ldots, K\}$, $l1 \in \{1, 2, \ldots, L^{k1}\}$, $l2 \in \{1, 2, \ldots, L^{k2}\}$, etc. where upper case K [not to be confused with lower case k from (1)] is the number of test benches with common design variables vector $\boldsymbol{x}$ that originate, after independent simulations, K measure sets. The measured set for the kth testbench contains the measured values m_l^k, with $l = 1, 2, \ldots, L^k$.

IV. Automatic Design Methodology

Fig. 3 illustrates the proposed design methodology, built over a Java framework for the automatic synthesis of analog ICs, analog IC design automation [26].

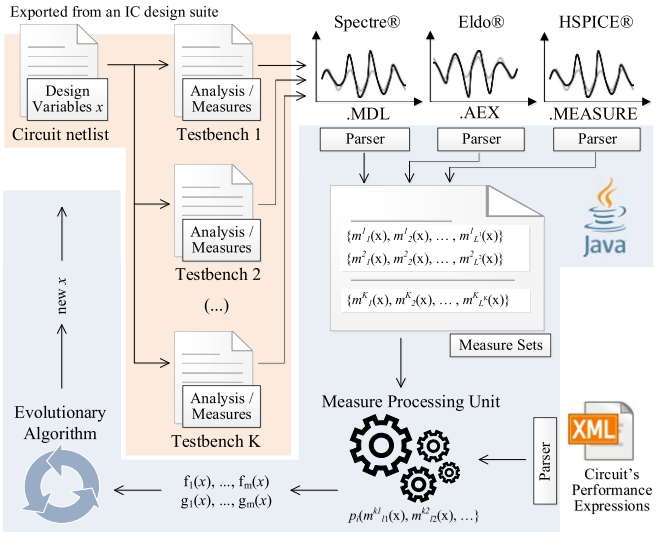

Fig. 3. Architecture of the multitest bench RF IC sizing optimization.

```
expr:      ['-' | '+' ] term {'+' term | '-' term}.
term:      factor {'*' factor | '/' factor | '%' factor}.
factor:    primary {'^' factor}.
primary:   variable | number | '(' expr ')' |
           'exp' '(' expr ')' | 'ln' '(' expr ')' |
           'min' '(' expr (',' expr) * ')' | 'max' '(' expr (',' expr) * ')' |
           'sqrt' '(' expr ')' |
           'cond' '(' compExpr ',' expr ',' expr ')' |
                  '(' compExpr ')' '?' '(' expr ')' ':' '(' expr ')'  |
           'not' '(' expr ')' |'and' '(' expr (',' expr) * ')' |
                  'or' '(' expr (',' expr) * ')' |
           'avg' '(' expr (',' expr) * ')' | 'rms' '(' expr (',' expr) * ')' |
           'db' '(' cplxnumber ')' | 'mag' '(' cplxnumber ')' |
                  'ph' '(' cplxnumber ')'
compExpr: term  compOper term
compOper: '=' | '<' | '>' | '<>' | '<=' | '>='
number:    intnumber | realnumber | scinumber | cplxnumber
cplxnumber: (intnumber | realnumber | scinumber) ('-' | '+') i (intnumber |
realnumber | scinumber)
scinumber: realnumber E ['-' | '+' ] intnumber
realnumber:          [ intnumber ] . [ intnumber ]
intnumber: digit {digit}.
digit:     (0 | 1 | 2 | 3 | ... | 9)
variable:  [a-zA-Z]+
```

Fig. 4. EBNF for the usable expressions.

```
<Measure name="fssv_b0000" expr="abs(fosc_b0000_400mV-
fosc_b0000_350mV)/0.05"/>
<Measure name="fssv_b1111" expr="abs(fosc_b1111_400mV-
fosc_b1111_350mV)/0.05"/>
<Measure name="FOM_b0000" expr="-10*LOG10((power_b0000*1E3)*
(10E6/fosc_b0000_350mV)*(10E6/fosc_b0000_350mV)) - PN_b0000_10M)"/>
<Measure name="FOM_b1111" expr="-10*LOG10((power_b1111*1E3)*
(10E6/fosc_b1111_350mV)*(10E6/fosc_b1111_350mV)) - PN_b1111_10M"/>
```

Fig. 5. XML description for the postprocessed measures of Table II.

A. Design Flow

The architecture represents the K test benches of (4) as parameterized netlists with common design variables $\boldsymbol{x}$. All the circuit netlists and test benches required for optimization can be exported from a common IC design suite, e.g., Cadence, and are specific to the simulator being used. The measured set for the kth testbench contains the measured values m_l^k, with $l = 1, 2, \ldots, L^k$. Therefore, the native simulator measure descriptions necessary to obtain m_l^k values are also incorporated in the test benches' setup. At each iteration of the optimization process, the framework simulates the K test benches in parallel or sequentially, depending on the available computational resources, and parsers are internally provided for each of the output standard formats, i.e., .MDL (Cadence's Spectre), .AEX (Mentor Graphics' Eldo), and .MEASURE (Synopsys HSPICE).

After the acquisition of the measured values, the internal measure sets become independent of the origin of the data, and therefore, treating the data from one test bench or any from multiple simulators is equivalent. The measured values are then passed to the measured processing unit to obtain the circuit's performance expressions that define the objectives and constraints, $f_m(x)$ and $g_m(x)$, respectively, that are considered in the evolutionary algorithm. It is important to note that these circuit expressions are not performance equations as used in the equation-based circuit optimization, as the expressions considered are always functions of the simulations' output.

Therefore, a formulation for the optimization objectives and constraints closer to the application that depends directly from the simulations' output and more familiar to IC designers was derived from (4) and embedded into the proposed EDA framework. Here, the expressions for $p_m(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots)$ and $p_i(m_{l1}^{k1}(x), m_{l2}^{k2}(x), \ldots)$ are defined by the designer using a set of provided logical (conditional statements, equal, larger, and smaller) and arithmetic operators ($+$, $-$, $/$, $*$). Moreover, in addition to the arithmetic and logical operators, common operations such as max, min, rms, db, and mag, are also supported. The parser itself is a recursive descent parser for the extended Backus–Naur form (EBNF), as shown in Fig. 4. The implementation of the expression parser starts from the expressions' description, which is made by the designer using an extensible markup language (XML) input file, which is also used for the tools' setup, in the format illustrated in Fig. 5.

This setup enhances the traditional simulation-based sizing and optimization of RF ICs for complex measures and allows the tool to enforce simultaneously all the required specifications (e.g., optimization constraints), instead of iterating over several optimizations or manual parameter tuning considering subproblems. The implemented postprocessing also enables the extension, as well as the unification, of complex measurement description among multiple simulators. This is especially relevant when simulators' native measure statements are limited or required more tools to process the output, which may imply additional licensing costs.

B. Evolutionary Algorithm

Specifically, the all-inclusive test bench formulation of Section III is dealt here using the nondominated sorting genetic algorithm (NSGA)-II [28], whose pseudocode is introduced in Algorithm 1. Further discussion on the algorithms' operations can be remitted for the original publication. Nonetheless, the proposed problem is generic and can be easily applied to many other metaheuristic optimization algorithms.

Algorithm 1 NSGA-II Procedure

1. Set g = 0, create random population R_0 of size 2N
2. Simulate population R_0 in the K test benches
3. Non-dominated sorting algorithm to identify the non-dominated fronts F_1, F_2, …, F_f in R_g
4. for i=1,…,f do
5. Calculate crowding distance of the solutions in F_i
6. Create P_{g+1} as follows:
   If $|P_{g+1}|+|F_i| \leqslant N$, then set $P_{g+1} = P_{g+1} \cup F_i$;
   If $|P_{g+1}|+|F_i| > N$, then add the least crowded N - $|P_{g+1}|$ solutions from F_i to P_{g+1}
8. Binary tournament selection to select parents from P_{g+1}
9. Crossover and mutation to P_{g+1} to create offspring Q_{g+1} of size N
10. Simulate offspring Q_g in the K test benches
11. Set $R_{t+1} = P_{t+1} \cup Q_{t+1}$
12. Set g = g + 1 and **go to 3**.

The proposed approach is flexible to any analog and RF circuit class of any complexity, e.g., VCOs, low-noise amplifiers, and mixers, and the inputs required from the designer are only the functional parameterized circuit netlist(s) and testbench(es) with corresponding analyses and measures. Moreover, the ranges of the design variables and design specifications can be specified using a graphical interface developed for the framework. As evolutionary algorithms have been widely proved on higher dimensional design spaces, scalability (in the sense of design space dimensionality) is not a major issue. The VCO addressed in this paper contains 28 optimization variables; however, a higher number could be used if needed for a more complex circuit topology. The major concern in terms of scalability is the amount of time that may be required to perform the evaluation of a candidate sizing, i.e., the time it takes each candidate sizing to be simulated in the complete set of K test benches. If the evaluation of a single sizing takes too long, the time required to carry an optimization can be prohibitive, even considering parallelization in modern workstations. Moreover, of only a few generations are performed, the optimization process will reach only very suboptimal solutions to the problem.

V. Optimization Setup and Results

Fig. 1 introduced the schematic of the VCO where we applied the proposed optimization method. We used a low supply voltage of 0.35 V to achieve a power-efficient design in a 65-nm CMOS technology node. The VCO can operate in either the class-C or class-D mode depending on the size of M_1/M_2. For IoT applications, we need a small size for M_1/M_2 and the VCO operating in the class-C mode to reduce the power consumption. For cellular applications, a larger size of M_1/M_2 is necessary to enable the VCO operating in the class-D mode, which boosts the output swing to $\sim 3\ V_{DD}$, thus reducing the phase noise [27]. We also employ a 4-bit binary-sized SCA together with accumulation-mode varactors to tune the VCO frequency from 3.8 to 4.9 GHz continuously. The SCA biasing voltages V_{DDH} and V_{DDL} are 1 and 0.5 V, respectively. The inductor topology adopted is an octagonal spiral inductor in ultrathick metal, and the inductor model provided by the foundry supports the change of different dimension parameters.

TABLE I
Optimization Variables and Description

Variable	Units	Min.	Grid	Max.
ind_radius	µm	15	5	90
ind_nturns	-	1	1	6
ind_spacing	µm	2	1	4
ind_width	µm	3	1	30
mccl, m1l	nm	60	20	240
mccw, m1w	µm	0.6	0.2	6
mccnf, m1nf	-	1	1	32
mccm	-	1	1	100
moscapw	µm	0.4	0.2	3.2
moscapl	µm	0.2	0.2	3.2
mimvw, mimvl, mim1w	µm	2	0.2	20
r1l, r2l, r3l, r4l	µm	1	0.2	10
r1m, r2m, r3m, r4m	-	1	1	20
nfn1, nfn2, nfp1, nfp2	-	1	1	100

A. Design Variables

The netlist of the VCO was fully parameterized (*LC* tank, 4-bit binary-sized SCA, and SCA control) using a commercial IC design suite and the netlists exported. In total, there are 28 optimization variables related to the sizing of 43 devices. Table I details the limits and ranges of each variable, where ind_radius, ind_nturns, ind_spacing, and ind_width are the inner radius, number of turns, spacing between conductors, and conductor width, respectively, of the inductor L; mccl, mccw, mccnf, and mccm are the length per finger, width per finger, number of fingers, and device multiplier, respectively, of the cross-coupled M_1/M_2 transistors; moscapw and moscapl are the width and length per finger (for eight-finger structures), respectively, of the varactors; mimvw and mimvl are the width and length, respectively, of the metal–insulator–metal (MIM) capacitors of the tank; m1l, m1w, and m1nf are the length per finger, width per finger, and number of fingers, respectively, of the n-type transistors from the 4-bit SCA, using a device multiplier ratio of 8:4:2:1; mim1w is simultaneously the width and length of the MIM capacitors from the 4-bit SCA, using a device multiplier ratio of 8:4:2:1; and r1l and r1m are the segment length and multiplier, respectively, for a fixed segment width of 0.5 μm of the resistors from the first bit of SCA. r2l, r2m, r3l, r3m, r4l, and r4m are the respective variables for the second, third, and fourth bits; nfn1 and nfp1 are the numbers of fingers from n-type/p-type transistors from the VDDH inverters of the 4-bit SCA, for a fixed length per finger of 60 nm and width per finger of 500 nm; and nfn2 and nfp2 are used for the VDDL inverters.

B. Test Benches and Measurements

For each different tuning frequency of the SCA control $B\langle 3{:}0\rangle$, we define two different test benches. In the first, we perform a steady state (SST) and SST noise analyses to extract f_{osc}, phase noises, and power for the standard supply voltage, and in the second test bench, we only perform an

TABLE II
MEASURES AND TEST BENCHES

Measure	Units	Description	Measured from / Computed by
$f_{osc}[b_{0000}]$@0.35V	GHz	f_{osc} for b_{0000} at 0.35V supply	SST@0.35V_{0000}
$f_{osc}[b_{1111}]$@0.35V	GHz	f_{osc} for b_{1111} at 0.35V supply	SST@0.35V_{1111}
$f_{osc}[b_{0000}]$@0.40V	GHz	f_{osc} for b_{0000} at 0.40V supply	SST@0.40V_{0000}
$f_{osc}[b_{1111}]$@0.40V	GHz	f_{osc} for b_{1111} at 0.40V supply	SST@0.40V_{1111}
PN[b_{0000}]@10kHz	dBc/Hz	Phase noise at 10KHz for b_{0000}	SST@0.35V_{0000}
PN[b_{0000}]@100kHz	dBc/Hz	Phase noise at 100KHz for b_{0000}	SST@0.35V_{0000}
PN[b_{0000}]@1MHz	dBc/Hz	Phase noise at 1MHz for b_{0000}	SST@0.35V_{0000}
PN[b_{0000}]@10MHz	dBc/Hz	Phase noise at 10MHz for b_{0000}	SST@0.35V_{0000}
PN[b_{1111}]@10kHz	dBc/Hz	Phase noise at 10KHz for b_{1111}	SST@0.35V_{1111}
PN[b_{1111}]@100kHz	dBc/Hz	Phase noise at 100KHz for b_{1111}	SST@0.35V_{1111}
PN[b_{1111}]@1MHz	dBc/Hz	Phase noise at 1MHz for b_{1111}	SST@0.35V_{1111}
PN[b_{1111}]@10MHz	dBc/Hz	Phase noise at 10MHz for b_{1111}	SST@0.35V_{1111}
power[b_{0000}]	mW	Power consumption for b_{0000}	SST@0.35V_{0000}
power[b_{1111}]	mW	Power consumption for b_{1111}	SST@0.35V_{1111}
fssv[b_{0000}]	MHz/V	Frequency sensitivity for b_{0000}	XML (Fig. 5)[1]
fssv[b_{1111}]	MHz/V	Frequency sensitivity for b_{1111}	XML (Fig. 5)[2]
FOM[b_{0000}]	dBc/Hz	Figure-of-merit for b_{0000}	XML (Fig. 5)[3]
FOM[b_{1111}]	dBc/Hz	Figure-of-merit for b_{1111}	XML (Fig. 5)[4]

[1] $abs[(f_{osc}[b_{0000}]@0.35V - f_{osc}[b_{0000}]@0.35V)/0.05]$
[2] $abs[(f_{osc}[b_{1111}]@0.35V - f_{osc}[b_{1111}]@0.35V)/0.05]$
[3] $-10*\log_{10}[(power[b_{0000}]*1E3)*(10E6/f_{osc}[b_{0000}]@0.35V)] - PN[b_{0000}]@10MHz$
[4] $-10*\log_{10}[(power[b_{1111}]*1E3)*(10E6/f_{osc}[b_{1111}]@0.35V)] - PN[b_{1111}]@10MHz$

SST analysis to extract f_{osc} for a supply voltage of 0.4 V. These test benches are henceforward designated by SST at 0.35_{bxxxx} and SST at 0.40_{bxxxx}, respectively. To optimize the complete tuning range meticulously, 32 test benches would be required to sweep all combinations from SCA control. Usually, the SCA will have the lowest Q-factor when all the switches are ON ($B\langle 1111\rangle$), which degrades the phase noise and increases the power consumption of the VCO [29]. On the other hand, the tank capacitor is dominated by the nonlinear parasitic capacitance when all the switches in the SCA are OFF ($B\langle 0000\rangle$), which degrades the $1/f^3$ phase noise performance through amplitude modulation-to-phase modulation noise conversion [30]. Thus, as a proof of concept, only the 4.9-GHz ($B\langle 0000\rangle$) and 3.8-GHz ($B\langle 1111\rangle$) tunings representing the two extreme cases here are detailed and used for optimization. Nevertheless, the continuous tuning between 3.8 and 4.9 GHz is guaranteed by the device multiplier ratio of 8:4:2:1 on the 4-bit SCA, as detailed in Section V-A. Table II schematizes the complete list of measurements adopted. We used the postprocessing introduced in Section IV to define the XML of two types of measures as presented in Fig. 5, namely, frequency sensitivity due to a supply variation f_{ssv} of 50 mV

$$f_{\text{ssv}} = \left| \frac{f_{\text{osc}} \text{ at } V\text{dd}_2 - f_{\text{osc}} \text{ at } V\text{dd}_1}{V\text{dd}_2 - V\text{dd}_1} \right| \text{ [Hz/V]} \quad (5)$$

where f_{osc} at $V\text{dd}_1$ is the oscillation frequency at the reference supply voltage $V\text{dd}_1$, i.e., 0.35 V, and f_{osc} at $V\text{dd}_2$ at a different supply voltage, i.e., 0.4 V, and second, FOM, given by

$$\text{FOM} = -10\log\left[\frac{P_{\text{dc}}}{1\text{ mW}} \cdot \left(\frac{\Delta\omega}{\omega_0}\right)^2\right] - L(\Delta\omega) \text{ [dBc/Hz]} \quad (6)$$

TABLE III
OPTIMIZATION OBJECTIVES FOR IOT, CELLULAR, AND DUAL MODE

	Metric	Target	Units
A. IoT	Max(power[b_{0000}], power[b_{1111}])	minimize	mW
	Min(FOM[b_{0000}], FOM[b_{1111}])	maximize	dBc/Hz
	Max(fssv[b_{0000}], fssv[b_{1111}])	minimize	Hz/V
B. Cellular	**Metric**	**Target**	**Units**
	Max(PN[b_{0000}]@10MHz, PN[b_{1111}]@10MHz)	minimize	dBc/Hz
	Min(FOM[b_{0000}], FOM[b_{1111}])	maximize	dBc/Hz
	Max(fssv[b_{0000}], fssv[b_{1111}])	minimize	Hz/V
C. Dual-mode	**Metric**	**Target**	**Units**
	Max(power[b_{0000}], power[b_{1111}])	minimize	mW
	Max(PN[b_{0000}]@10MHz, PN[b_{1111}]@10MHz)	minimize	dBc/Hz
	Max(fssv[b_{0000}], fssv[b_{1111}])	minimize	Hz/V

where ω_0 is the oscillation frequency, P_{dc} is the power consumption, $\Delta\omega$ is the offset from the output frequency, and $L(\Delta\omega)$ is the oscillator phase noise. The tradeoff reflects the fact that the FOM allows the assessment of the overall performance of the VCO, which is better with a higher absolute value of FOM.

C. Optimization Objectives and Constraints

Three different sets of objectives for three independent optimizations were tested, where postprocessing was defined to ensure that the optimization process always tries to improve the worst case performance and therefore obtain the global optimum solutions as follows.

1) The first set is targeted for IoT, i.e., ultralow power consumption with relaxed phase noise, using the high-FOM constraint to still aim for the best overall performance possible. Therefore, postprocessing was defined to simultaneously minimize the largest power value measured, maximize the lowest FOM value measured, and minimize the highest f_{ssv} value measured (Table III).
2) The second set is targeted for cellular applications, i.e., stringent phase noise performance. It is intended to simultaneously minimize the worst phase noise at 10 MHz value measured, maximize the lowest FOM value measured, and minimize the highest f_{ssv} value measured (Table III). In addition, an alternative setup was defined which targets individual specification figures without attempting to bias the optimization toward either cellular or IoT specifications.
3) This third set allows the exploration of the topology for both extreme specifications in a single optimization run, i.e., dual-mode, by minimizing the largest power value measured, minimize the worst value of phase noise at 10 MHz measured, and minimize the highest f_{ssv} value measured (Table III). In this case, the FOM is inherently optimized.

Moreover, the third column of Table IV details the optimization constraints, which are set on the f_{osc} to meet the desired range, at phase noises FOMs above 190 dBc/Hz and f_{ssvs} below 500 MHz/V. Additional constraints could be set

TABLE IV
OPTIMIZATION CONSTRAINTS AND PERFORMANCE COMPARISON

Measure	Units	Constraint Target(s)	*JSSC sim.*[1]	*JSSC meas.*[2]	IoT_a[4]	$Dual_a$[4]	Cel_b[5]	$Dual_b$[5]	IoT_c[6]	Cel_c[6]	$Dual_c$[6]
$f_{osc}[b_{0000}]$@0.35V	GHz	≥ 4.8 ≤ 5.0	4.800	4.800	4.870	4.832	4.832	4.805	4.900	4.958	4.991
$f_{osc}[b_{1111}]$@0.35V	GHz	≥ 3.7 ≤ 3.9	3.000	3.000	3.871	3.814	3.814	3.888	3.859	3.703	3.730
$f_{osc}[b_{0000}]$@0.40V	GHz	n/d	n/a	n/a	4.852	4.829	4.829	4.782	4.900	4.957	4.991
$f_{osc}[b_{1111}]$@0.40V	GHz	n/d	n/a	n/a	3.861	3.811	3.811	3.891	3.859	3.703	3.730
$PN[b_{0000}]$@10kHz	dBc/Hz	≤ -59	n/a	n/a	-74.5	-72.4	-72.4	-81.3	-69.1	-71.5	-71.2
$PN[b_{0000}]$@100kHz	dBc/Hz	≤ -86	-100.0	-90.5	-94.8	-94.1	-102.9	-102.5	-92.5	-97.3	-97.2
$PN[b_{0000}]$@1MHz	dBc/Hz	≤ -108	-124.0	-118.5	-114.8	-114.3	-123.1	-122.7	-113.1	-118.7	-118.7
$PN[b_{0000}]$@10MHz	dBc/Hz	≤ -129	-144.0	-143.5	-134.6	-134.2	**-143.0**[5]	**-142.5**[5]	-133.0	-138.8	-138.6
$PN[b_{1111}]$@10kHz	dBc/Hz	≤ -65	n/a	n/a	-78.0	-77.4	-75.0	-74.8	-74.3	-78.35	-78.8
$PN[b_{1111}]$@100kHz	dBc/Hz	≤ -92	-108.0	-100.5	-98.3	-97.7	-102.2	-101.7	-96.4	-100.9	100.8
$PN[b_{1111}]$@1MHz	dBc/Hz	≤ -113	-129.5	-127.0	-114.8	-117.8	-124.4	-123.8	-116.7	-121.3	-121.2
$PN[b_{1111}]$@10MHz	dBc/Hz	≤ -134	-150.0	-149.5	-137.7	-137.3	**-143.0**[5]	**-142.7**[5]	-136.4	-140.3	-140.2
$power[b_{0000}]$	mW	n/d	2.1[3]	4.0	**0.117**[4]	**0.133**[4]	1.598	1.059	0.188	0.765	0.758
$power[b_{1111}]$	mW	n/d	5.4	6.8	**0.117**[4]	**0.134**[4]	1.597	1.058	0.188	0.767	0.760
$fssv[b_{0000}]$	MHz/V	≤ 500	600	n/a	352	64	422	470	**< 1**[6]	**6**[6]	**2**[6]
$fssv[b_{1111}]$	MHz/V	≤ 500	175	n/a	196	62	86	58	**< 1**[6]	**6**[6]	**2**[6]
$FOM[b_{0000}]$	dBc/Hz	≥ 190	194.4	191.0	197.7	196.6	194.6	195.2	194.1	193.9	193.7
$FOM[b_{1111}]$	dBc/Hz	≥ 190	192.2	190.0	198.8	197.7	192.7	193.6	195.4	192.9	192.9
$PN[b_{0000}]$@10MHz comparison			ref.	-	+6.5%	+6.8%	+0.7%	+1.0%	+7.6%	+3.6%	+3.8%
$power[b_{0000}]$ comparison			ref.	-	-94.4%	-93.7%	-23.9%	-49.6%	-91.0%	-63.6%	-63.9%
$fssv[b_{0000}]$ comparison			ref.	-	-41.3%	-89.3%	-29.7%	-21.7%	-99.8%	-98.5%	-99.5%
$FOM[b_{0000}]$ comparison			ref.	-	-1.8%	-1.1%	-0.1%	-0.4%	+0.2%	+0.3%	+0.4%

[1]Simulation values on a 65 nm technology, 0.4 V supply and tuning range from 3.0 GHz to 4.8 GHz [27]; [2]Measurements on the same conditions of *JSSC sim.*; [3]Value inferred from Eq. (25) of [27], due to its excellent agreement between theoretical and simulated values; [4]Points from the IoT and Dual-mode optimizations with lowest power; [5]Points from the Cellular and Dual-mode optimizations with lowest phase noise; [6]Points from the IoT, Cellular and Dual-mode optimizations with lowest *fssv*.

on power consumptions; however, these were intentionally left unconstrained to visualize the complete design tradeoffs.

D. Optimization Runs, Results, and Analysis

In this paper, the circuit simulator adopted was the Mentor Graphics' Eldo RF. The three optimizations detailed in Section V-C were carried with populations of 512 elements and optimized for 1000 generations. The POFs of IoT, cellular, and dual-mode optimizations provided 59 423, and 287 optimal sizing solutions, respectively, are drawn in Figs. 6–8. Each optimization took approximately 100 h in an Intel-Xeon-CPU E5-2630-v3@2.40 GHz with 64 GB of RAM workstation using eight cores for parallel evaluation.

Due to the nature of the FOM metric, in Fig. 6(b), power consumption is almost linearly correlated with the FOM. Only at extreme ultralow-power values (and therefore ultrahigh FOMs), the f_{ssv} becomes significantly worst, i.e., equal to and higher than 150 MHz/V, as depicted in Fig. 6(a). For Fig. 7(b), despite the FOM dependence from phase noise, the POF presents three different regions spreading through different ranges of FOM. At a first glance, the lower region of the figure with better phase noise values seems to dominate the intermediate region; however, due to the dimensionality introduced with the f_{ssv}, it is possible to visualize in Fig. 7(a) boundaries of a tradeoff not explored in previous works.

The dual-mode POF of Fig. 8 inherently optimized the FOM metric, with all solutions equal to or above 192 dBc/Hz. From the projection of Fig. 8(b), it is clear to observe two distinct regions of the design space: a smaller one tailored for IoT application, with power ranging from 0.134 to 0.174 mW for worst phase noise values (between −133.9 and −134.5 dBc/Hz) and a larger region for cellular application,

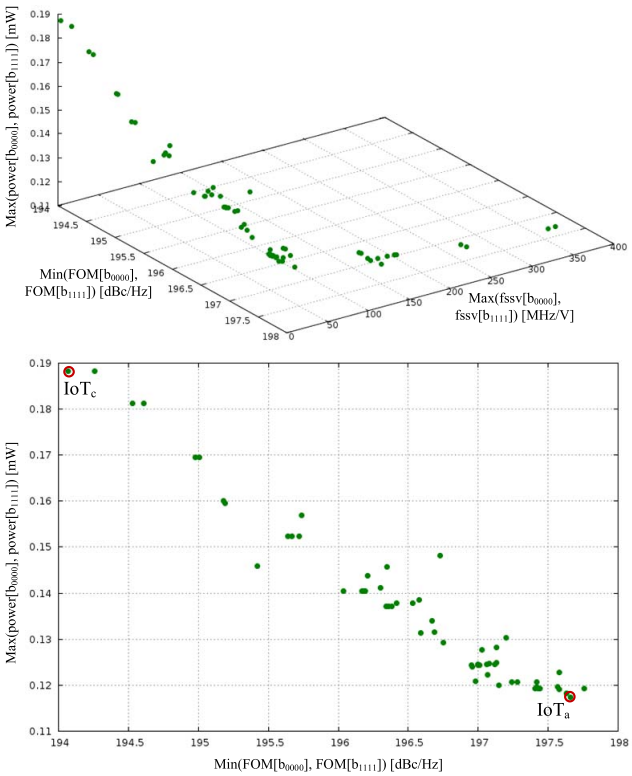

Fig. 6. POF for the IoT application tradeoff of Table III with 59 optimal sizing solutions. The solutions spread from 0.117- to 0.188-mW power, 194.1–197.8-dBc/Hz FOM, and ⟨1–352-MHz/V f_{ssv}. (a) 3-D representation. (b) Projection power versus FOM.

with phase noises ranging from −137.8 to −142.5 dBc/Hz for worst power values (between 0.559 and 1.333 mW). The detailed performances of some sizing solutions from the

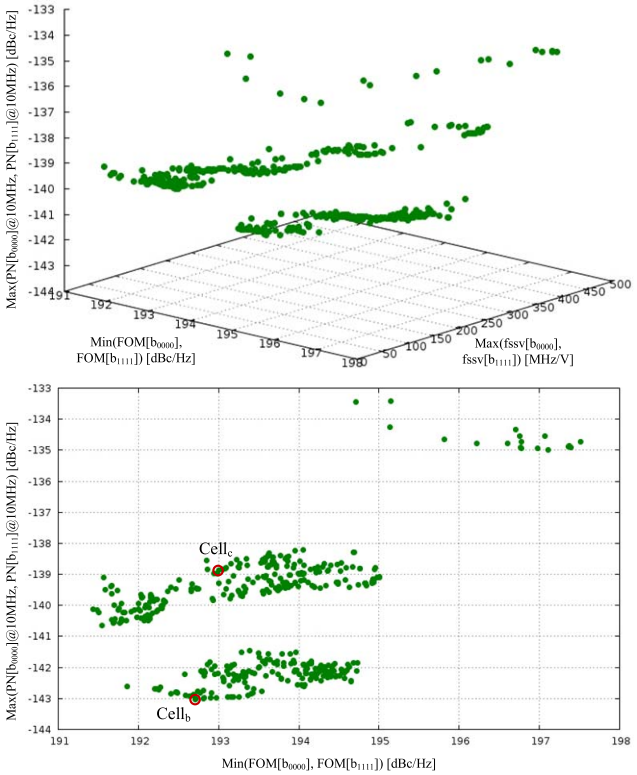

Fig. 7. POF for the cellular application tradeoff of Table III with 423 optimal sizing solutions. The solutions spread from −133.4- to −143.0-dBc/Hz phase noise, 191.4–197.5-dBc/Hz FOM, and 6–500-MHz/V f_{ssv}. (a) 3-D representation. (b) Projection phase noise versus FOM.

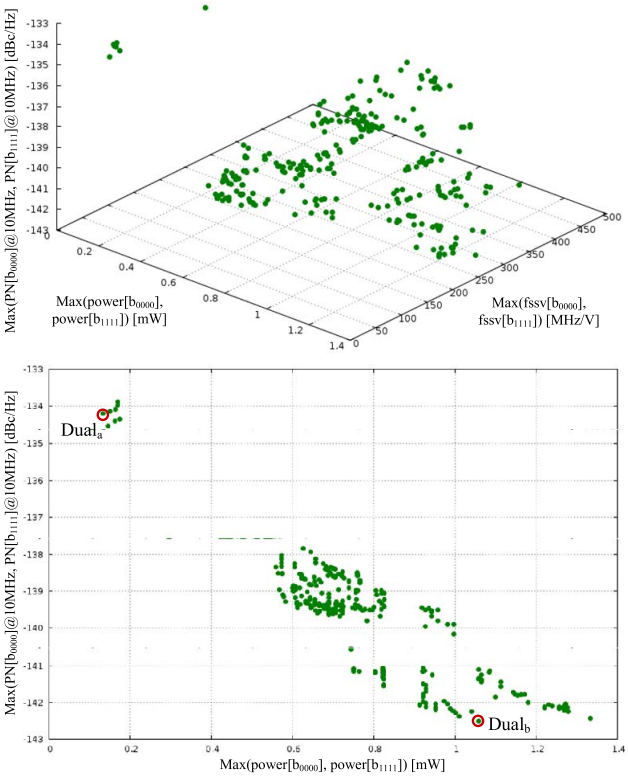

Fig. 8. POF for the dual-mode tradeoff of Table III with 287 optimal sizing solutions. The solutions spread from 0.134- to 1.333-mW power, −133.9- to −142.5-dBc/Hz phase noise, and 2–500-MHz/V f_{ssv}. (a) 3-D representation. (b) Projection phase noise versus power.

TABLE V
SIZING OF THE HIGHLIGHTED SOLUTIONS FROM THE DUAL-MODE POF

Variable	Unit	Dual_a	Dual_b	Dual_c
ind_radius	µm	90.0	90.0	90.0
ind_nturns	unit	1	2	1
ind_spacing	µm	4.0	4.0	4.0
ind_width	µm	30.0	26.0	16.0
mccl, m1l	nm	80, 60	80, 60	100, 80
mccw, m1w	µm	0.6, 5.6	0.6, 2.4	0.6, 5.8
mccnf, m1nf	unit	15, 31	14, 32	10, 32
mccm	unit	93	9	89
moscapw	µm	0.8	0.4	1.2
moscapl	µm	0.2	0.6	0.2
mimvw,mimvl,mim1w	µm	20.0, 20.0, 12.0	9.0, 11.0, 7.0	20.0, 19.0, 13.0
r1l, r2l	µm	9.4, 9.0	7.0, 9.2	8.4, 5.0
r3l, r4l	µm	9.6, 10.0	9.4, 9.2	10.0, 7.2
r1m, r2m, r3m, r4m	unit	1, 1, 2, 1	2, 1, 1, 4	1, 2, 3, 4
nfn1, nfn2, nfp1, nfp2	unit	1, 75, 67, 65	14, 55, 7, 75	36, 15, 12, 6

three optimizations are highlighted in the last columns of Table IV. As observable, the dual optimization matched the best results of both independent optimizations. For replicability purposes, the specific sizing values of each highlighted solution from the dual-mode POF, i.e., Dual_a, Dual_b, and Dual_c, are presented in Table V.

The simulated performances of the original publication [27] (JSSC sim.) are used as reference values to benchmark the optimized fronts with respect to the remaining state-of-the-art in the VCO design, even though the circuit was originally sized for a 0.4-V supply voltage and a 3.0–4.9-GHz tuning range, which benefits the phase noises, especially at the lower range, i.e., $B = \langle 1111 \rangle$. The measured performances (JSSC meas.) are also highlighted, which provide some insights of expected performance degradation after manufacturing. For a fair comparison, from $B\langle 0000 \rangle$ power and phase noises of columns JSSC sim., Cel_b and Dual_b of Table IV, the proposed methodology found solutions with less 23.9% and 49.6% power consumption than original sizing, for similar phase noise reference values (−143.0 and −142.5 dBc/Hz, respectively), which is also reflected positively on the FOM. Phase noise values of −144.0 dBc/Hz were also achieved, but only when allowing the optimization process to accept solutions with f_{ssv} worse than 500 MHz/V. By observing the JSSC sim., IoT_a and Dual_a columns of Table IV, the potential to address this circuit in ultralow-power applications is proved, as power consumption was reduced more than 93% in both cases with respect to the original prelayout design, achieving impressive FOMs above 197.7 dBc/Hz for the higher tuning range and 198.8 dBc/Hz for the lower tuning range. Moreover, when the original circuit is tuned to 3.7 GHz ($B = \langle 1111 \rangle$), it consumes 3.54-mW prelayout with an FOM of 192.87 dBc/Hz and 400 MHz/V f_{ssv}, suboptimal results when comparing with the optimized ones. Obtained results are extremely promising even when expecting a significant increase in power consumption after manufacturing, whereas phase noise values held, with only a significant mismatch between the simulation and measured phase noise at the 100-kHz offset from central oscillation frequency.

Finally, in the last columns of Table IV, i.e., IoT_c, Cell_c, and Dual_c, the points with better f_{ssv} from each optimization are highlighted (all below 6 MHz/V). Due to the nature of the many-objective optimizations performed, this complex tradeoff was explored and weighted at each evaluation, achieving solutions with extremely low frequency pushing figures, unlike previously published results [27]. This fact is extremely relevant, as this metric is one of the most critical issues in the design of class-C/D VCOs for a real-life product, especially at low V_{dd} values.

E. Worst Case Corner Dual-Mode Optimization

When designing a circuit, the designer must consider that some variation will occur between the simulated and the fabricated designs. There are different variation causes, e.g., environmental variations (temperature, power supply voltage, etc.) or process variations. While the environmental variations affect the circuit after its fabrication, process variations are introduced during the lithographic process. In Sections V-B, C and D, some sort of environment variation was already considered by the introduction of f_{ssv} metric. However, to study the impact of process variations in the VCO, the following process corners were considered: slow nMOS/slow pMOS (SS); slow nMOS/fast pMOS (SF); and fast nMOS/slow pMOS (FS). Therefore, six additional test benches were added to the previous typical (TT) setup. Except for f_{ssv}, the measures from Table II were quadruplicated. This resulted in a 66-D performance space spread through two different modes ($B\langle 0000\rangle$ and $B\langle 1111\rangle$), resultant from 10 different test benches (SST at $0.35\text{V}_{0000}\{\text{TT}\}$, SST at $0.35\text{V}_{1111}\{\text{TT}\}$, SST at $0.40\text{V}_{0000}\{\text{TT}\}$, SST at $0.40\text{V}_{0000}\{\text{TT}\}$, SST at $0.35\text{V}_{0000}\{\text{SS}\}$, SST at $0.35\text{V}_{1111}\{\text{SS}\}$, SST at $0.35\text{V}_{0000}\{\text{SF}\}$, SST at $0.35\text{V}_{1111}\{\text{SF}\}$, SST at $0.35\text{V}_{0000}\{\text{FS}\}$ and SST at $0.35\text{V}_{1111}\{\text{FS}\}$) simulated with the same 28-D design variable space $\boldsymbol{x}$ of Table I.

A new set of optimization targets was defined to meet the two extreme specifications, i.e., dual-mode, where post-processing was made to ensure that the optimization process always tries to improve the WCC performance from the worst case mode and, therefore, obtain the global optimum solutions, according to Table VI. Since the optimization verifies the imposed constraints on every process corner considered, some changes were performed in the optimization constraints outlined in the third column of Table IV; the phase noise constraints were relaxed by 5 dBc/Hz, the FOM constraints were relaxed by 5 dBc/Hz, and the f_{ssv} constraints were relaxed by 500 MHz/V, according to the third column of Table VII. To clarify, for example, if any of the modes or corner simulation fails the desired oscillation frequency, the solution is discarded by the optimization kernel.

The optimization was carried out with a population of 512 elements and optimized for 200 generations, using the dual-mode POF of Fig. 8 as the starting point. However, all sizing solutions of Fig. 8 are unfeasible (fail at least one constraint) in the presence of process corners at generation number 1. The optimization took approximately 50 h. The WCC optimization provided 104 optimal sizing solutions,

TABLE VI
OPTIMIZATION OBJECTIVES FOR WCC DUAL-MODE APPLICATION

Metric	Target	Units
Max(power[b_{0000}]{TT}, power[b_{1111}]{TT}, power[b_{0000}]{SS}, power[b_{1111}]{SS}, power[b_{0000}]{SF}, power[b_{1111}]{SF}, power[b_{0000}]{FS}, power[b_{1111}]{FS})	Min.	mW
Max(PN[b_{0000}]@10MHz{TT}, PN[b_{1111}]@10MHz{TT}, PN[b_{0000}]@10MHz{SS}, PN[b_{1111}]@10MHz{SS}, PN[b_{0000}]@10MHz{SF}, PN[b_{1111}]@10MHz{SF}, PN[b_{0000}]@10MHz{FS}, PN[b_{1111}]@10MHz{FS})	Min.	dBc/Hz
Max(fssv[b_{0000}]{TT}, fssv[b_{1111}]{TT})	Min.	Hz/V

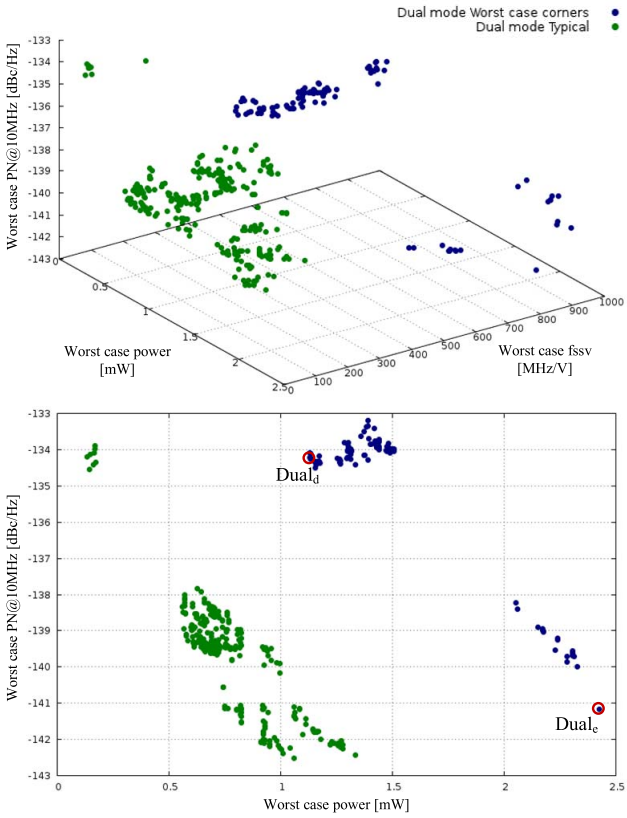

Fig. 9. POF for the WCC dual-mode tradeoff of Table VI with 104 optimal sizing solutions. The performances shown are the worst possible for each corner/mode of the design. The solutions spread from 1.130- to 2.426-mW power, −133.2- to −141.2-dBc/Hz phase noise, and 156–948-MHz/V f_{ssv}. (a) 3-D representation. (b) Projection worst case phase noise versus worst case power. The solutions are plotted against the typical dual-mode POF of Fig. 8.

drawn in Fig. 9 against the POF of Fig. 8, where the performances shown are the worst possible for each corner/mode of the design.

Similar to the typical POF of Fig. 9, it is clear to observe two distinct regions of the design space, but instead, the larger one is the one presenting smaller power consumptions values, with worst case power ranging from 1.130 mW (0.649 mW in TT) to 1.506 mW (0.822 mW in TT) for worst phase noise values (between −133.2 and −134.0 dBc/Hz) and a smaller region presenting smaller phase noise values, with worst case phase noises ranging from −138.2 to −141.2 dBc/Hz for worst power values (between 2.058 and 2.426 mW). The detailed performances of some sizing solutions from the optimization are highlighted in the last columns of Table VII.

TABLE VII
OPTIMIZATION CONTRAINTS AND PERFORMANCE COMPARISON FOR WCC

Measure	Units	Constraint Target(s)	$Dual_d$[1]				$Dual_e$[2]				$Dual_f$[3]			
			TT	SS	SF	FS	TT	SS	SF	FS	TT	SS	SF	FS
$f_{osc}[b_{0000}]$@0.35V	GHz	$\geq 4.8 \leq 5.0$	4.849	4.820	4.873	4.829	4.850	4.820	4.882	4.822	4.927	4.866	4.933	4.924
$f_{osc}[b_{1111}]$@0.35V	GHz	$\geq 3.7 \leq 3.9$	3.878	3.712	3.893	3.866	3.894	3.706	3.897	3.893	3.886	3.704	3.891	3.883
PN$[b_{0000}]$@10kHz	dBc/Hz	$\leq$ -54	-72.2	-74.7	-74.0	-71.5	-80.4	-80.6	-80.4	-81.0	-68.6	-72.2	-70.3	-68.1
PN$[b_{0000}]$@100kHz}	dBc/Hz	$\leq$ -81	-94.2	-94.8	-94.8	-93.9	-101.8	-101.2	-101.4	-102.3	-92.9	-94.0	-93.6	-92.3
PN$[b_{0000}]$@1MHz	dBc/Hz	$\leq$ -103	-114.5	-114.8	-114.9	-114.2	-122.0	-121.2	-121.5	-122.5	-113.6	-114.2	-114.1	-113.1
PN$[b_{0000}]$@10MHz	dBc/Hz	$\leq$ -124	-134.4	-134.7	-134.8	**-134.1**[w]	-141.6	-141.2	-141.3	-141.7	-133.9	-134.5	-134.4	**-133.4**[w]
PN$[b_{1111}]$@10kHz	dBc/Hz	$\leq$ -60	-75.2	-78.2	-76.9	-73.8	-73.5	-76.1	-74.5	-73.6	-72.5	-77.4	-74.8	-71.5
PN$[b_{1111}]$@100kHz	dBc/Hz	$\leq$ -87	-97.0	-98.3	-97.6	-96.2	-100.4	-101.3	-100.8	-100.5	-95.7	-97.7	-96.7	-94.9
PN$[b_{1111}]$@1MHz	dBc/Hz	$\leq$ -108	-117.1	-118.2	-117.7	-116.6	-122.5	-122.2	-122.4	-122.6	-116.2	-117.7	-117.0	-115.5
PN$[b_{1111}]$@10MHz	dBc/Hz	$\leq$ -129	-136.9	-138.0	-137.5	-136.2	-141.7	-141.8	-141.9	**-141.2**[w]	-136.2	-137.6	-136.9	-135.4
power$[b_{0000}]$	mW	n/d	0.649	0.246	0.339	1.120	1.499	0.615	0.807	**2.426**[w]	0.780	0.275	0.374	1.409
power$[b_{1111}]$	mW	n/d	0.650	0.246	0.336	**1.130**[w]	1.499	0.615	0.805	2.424	0.781	0.275	0.370	**1.421**[w]
fssv$[b_{0000}]$	MHz/V	$\leq$ 1000	**674**[w]	-	-	-	**808**[w]	-	-	-	**156**[w]	-	-	-
fssv$[b_{1111}]$	MHz/V	$\leq$ 1000	282	-	-	-	16	-	-	-	22	-	-	-
FOM$[b_{0000}]$	dBc/Hz	$\geq$ 185	190.0	194.5	193.2	187.3	193.6	196.9	196.0	191.5	188.9	193.8	192.5	185.8
FOM$[b_{1111}]$	dBc/Hz	$\geq$ 185	190.5	195.5	194.0	187.4	191.8	195.3	194.6	189.3	189.0	194.5	193.0	185.7

[1]Point from the WCC Dual-mode optimization with lowest power; [2]Point from the WCC Dual-mode optimization with lowest phase noise; [3]Point WCC Dual-mode optimization with lowest *fssv*; [w]Worst-case performances.

TABLE VIII
SIZING OF THE HIGHLIGHTED SOLUTIONS FROM THE WCC DUAL-MODE POF

Variable	Unit	$Dual_d$	$Dual_e$	$Dual_f$
ind_radius	µm	55.0	85.0	55.0
ind_nturns	unit	2	1	2
ind_spacing	µm	4.0	4.0	3.0
ind_width	µm	30.0	21.0	27.0
mccl, m1l	nm	120, 140	100, 60	80, 200
mccw, m1w	µm	3.6, 2.4	1.4, 4.8	3.4, 2.0
mccnf, m1nf	unit	2, 31	10, 25	2, 30
mccm	unit	60	83	69
moscapw	µm	0.6	0.6	0.8
moscapl	µm	0.2	0.2	0.2
mimvw,mimvl,mim1w	µm	5.0, 4.0, 8.0	16.6, 15.6, 11.8	8.0, 9.0, 8.0
r1l, r2l	µm	3.6, 6.2	8.2, 7.8	5.2, 6.4
r3l, r4l	µm	3.6, 3.0	9.8, 6.2	5.8, 5.2
r1m, r2m, r3m, r4m	unit	7, 3, 1, 3	1, 5, 2, 1	9, 4, 2, 6
nfn1, nfn2, nfp1, nfp2	unit	84, 92, 42, 72	2, 53, 18, 28	70, 86, 30, 91

For replicability purposes, the specific sizing values of each highlighted solution, i.e., $Dual_d$, $Dual_e$, and $Dual_f$, are presented in Table VIII.

The major challenge for the optimizer is to match all the oscillation frequencies on TT, SS, FS, and SF corners inside the 0.2-GHz range imposed on the constraints, which had a direct negative impact on the f_{ssv} performances when comparing to the typical-only optimization. When the proper oscillation frequencies are found, the phase noises are moderately affected for better performance (SS and SF) or worse performance (FS) when compared to the typical case with variations below 4.9 dBc/Hz (about 7%) on the highlighted points. However, power consumption is strongly enhanced (SS and FS) or degraded (SF) in the corner situations when comparing to the typical case. This has a severe impact on the WCC dual-mode tradeoff of Fig. 9, especially due to the points that suffered an 82% power consumption degradation in the SF corner, e.g., solution $Dual_f$. The capabilities of the circuit to address ultralow phase noise are present in this WCC optimization; however, the potential to address this circuit in ultralow-power applications is determined by the severe impact of the FS corner.

To reach TT values closer from the optimization of Section V-D, one optimization decision that could be taken was to alleviate the constraints on the FS corner only, a decision that designers tend to do naturally when designing a circuit by hand. Nonetheless, by using this WCC optimization approach, more reliable and robust designs can be achieved compared to the optimization that solely considers the typical device models, and a different insight on how process variations affect the design tradeoffs can be taken. Ultimately, the WCC optimization brings the designer closer to a first-pass fabrication success.

VI. COMPARISON WITH MIXED ITERATIVE/ SEQUENTIAL OPTIMIZATION APPROACH

As discussed in Section II, designers often use EDA tools to solve only subproblems of the traditional manual design, i.e., a series of LOs that tackles specific design targets. To discuss the attainable output of this mixed iterative/ sequential optimization approach, four optimizations were carried sequentially based on expert designer intents. In this process, design variables optimized in previous LOs are fixed for the following LOs, and the LO's output is provided to the following LO and continuously reoptimized for different targets. Each of these LOs was carried with a population of 512 elements through 250 generations (to match the 512/1000 of the dual-mode optimization).

A. Lo-1: Inductor and Cross-Coupled Transistors

Following the traditional manual design, the first LO consists on optimizing the inductor geometry and the cross-coupled M_1/M_2transistors, according to Table IX. The optimization targets were set to guarantee a proper oscillation frequency and acceptable phase noises at the highest bit of the SCA, i.e., 3.7 GHz ($B\langle 1111\rangle$), while minimizing the power and the phase noise at 10 MHz, as outlined in Table X. It is

TABLE IX

OPTIMIZATION VARIABLES FOR LO-1

Variable	Units	Min.	Grid	Max.
ind_radius	µm	15	5	90
ind_nturns	-	1	1	6
ind_spacing	µm	2	1	4
ind_width	µm	3	1	30
mccl	nm	60	20	240
mccw	µm	0.6	0.2	6
mccnf	-	1	1	32

TABLE X

CONSTRAINTS AND OBJECTIVES FOR LO-1 AND LO-2

Measure	Units	Constraint & Objectives
$f_{osc}[b_{1111}]$@0.35V	GHz	$\geq 3.7 \leq 3.9$
$PN[b_{1111}]$@10kHz	dBc/Hz	$\leq$ -65
$PN[b_{1111}]$@100kHz	dBc/Hz	$\leq$ -92
$PN[b_{1111}]$@1MHz	dBc/Hz	$\leq$ -113
$PN[b_{1111}]$@10MHz	dBc/Hz	$\leq$ -134, minimize
$power[b_{1111}]$	mW	minimize
$fssv[b_{1111}]$	MHz/V	$\leq$ 500, minimize (LO-2)

TABLE XI

OPTIMIZATION VARIABLES FOR LO-2 (VARIABLES FROM LO-1 WERE FIXED)

Variable	Units	Min.	Grid	Max.
m1l	nm	60	20	240
m1w	µm	0.6	0.2	6
m1nf	-	1	1	32
mim1w	µm	2	0.2	20
r1l, r2l, r3l, r4l	µm	1	0.2	10
r1m, r2m, r3m, r4m	-	1	1	20

important to note that the remaining parts of the circuit must be sized for the circuit to operate properly, and therefore, the design expert provided a first-cut operational sizing for the remaining variables of Table I. From this, LO resulted a POF of 44 solutions, spreading from 0.139 to 3.081 mW of $power[b_{1111}]$, and -136.9 to -144.2 dBc/Hz of $PN[b_{1111}]$ at 10 MHz.

B. Lo-2: Sca

In this LO, the n-type transistors, MIM capacitors, and resistors from the 4-bit SCA using a device multiplier ratio of 8:4:2:1, were optimized according to Table XI. Constraints and objectives were kept that the same as LO-1 of Table X; however, f_{ssv} was introduced as the third objective. LO-1 was used as the starting point of LO-2 and resulted in a POF of 201 solutions, spreading from 0.139 to 3.047 mW of $power[b_{1111}]$, -136.8 to -144.4 dBc/Hz of $PN[b_{1111}]$ at 10 MHz, and <1–498 MHz/V of $f_{ssv}[b_{1111}]$.

C. Lo-3: Varactor

In this LO, only the varactor is optimized, according to Table XII, to cover the frequency gap of the lowest bit of the SCA, i.e., 4.9 GHz ($B\langle 0000\rangle$). The optimization targets were set to guarantee a proper oscillation frequency and acceptable phase noises while minimizing the power and the phase noise at 10 MHz, as outlined in Table XIII. LO-3 used as the starting point of the optimization output of LO-2 and resulted in a POF of only seven feasible solutions, spreading from 0.139 to 1.798 mW of $power[b_{0000}]$, and -133.1 to -139.0 dBc/Hz of $PN[b_{0000}]$ at 10 MHz.

TABLE XII

OPTIMIZATION VARIABLES FOR LO-3 (VARIABLES FROM LO-1 AND LO-2 WERE FIXED)

Variable	Units	Min.	Grid	Max.
moscapw	µm	0.4	0.2	3.2
moscapl	µm	0.2	0.2	3.2

TABLE XIII

CONSTRAINTS AND OBJECTIVES FOR LO-3

Measure	Units	Constraint Target(s) & Objectives
$f_{osc}[b_{0000}]$@0.35V	GHz	$\geq 4.8 \leq 5.0$
$PN[b_{0000}]$@10kHz	dBc/Hz	$\leq$ -59
$PN[b_{0000}]$@100kHz	dBc/Hz	$\leq$ -86
$PN[b_{0000}]$@1MHz	dBc/Hz	$\leq$ -108
$PN[b_{0000}]$@10MHz	dBc/Hz	$\leq$ -129, minimize
$power[b_{0000}]$	mW	minimize

TABLE XIV

OPTIMIZATION VARIABLES FOR LO-4 (REMAINING VARIABLES FROM LO-1, LO-2, AND LO-3 WERE FIXED)

Variable	Units	Min.	Grid	Max.
mimvw, mimvl	µm	2	0.2	20
ind_radius	µm	15	5	90
ind_nturns	-	1	1	6
ind_spacing	µm	2	1	4
ind_width	µm	3	1	30

D. Lo-4: Fixed Capacitances

In this final LO, the fixed MIM capacitors of the tank are optimized, aware that large fixed capacitors will improve the phase noise but degrade the frequency-tuning range. Inductor geometry is again reoptimized to account for the possible changes on the fixed capacitors, according to Table XIV. To allow for a direct comparison with the solutions from the dual-mode POF shown in Fig. 8, the objectives and constraints were set for the same as in Table IV. LO-4 used as the starting point of the optimization output of LO-3 and resulted in a POF of nine feasible solutions, with approximately 0.139 mW of worst case power, -133.0–133.4-dBc/Hz worst case PN at 10 MHz, and 418–440 MHz/V of worst case f_{ssv}. That is, only solutions oriented for ultralow-power IoT applications were obtained. It is important to note that if the constraints for Table IV were relaxed, it was likely that the optimization process would produce a higher number of solutions; however, those were not the intended designs.

The details of the solution with the lowest worst case power are highlighted in Table XV and compared with solution $Dual_a$. The solution presents satisfiable performances when comparing with Duala; however, the major drawback is in terms of f_{ssv}, as Duala has 69.9% and 85.5% lower $f_{ssv}[b_{1111}]$ and $f_{ssv}[b_{0000}]$, respectively. Moreover, this mixed iterative/sequential design approach does not allow obtaining any insights into the performances tradeoffs of the circuit, whereas dual-mode optimization produced 287 different sizing solutions, for both IoT and cellular applications.

This experiment was conducted with a single forward optimization set (LO-1 to LO-4), and therefore, the tradeoffs

TABLE XV
PERFORMANCE COMPARISON BETWEEN THE SOLUTION OBTAINED WITH THE MIXED ITERATIVE/SEQUENTIAL OPTIMIZATION APPROACH AND DUAL$_a$ FROM "EVERYTHING-AT-ONCE" APPROACH

Measure	Units	Constraint Target(s)	Iter./ Seq.	Dual$_a$	Comparison
$f_{osc}[b_{0000}]$@0.35V	GHz	$\geq 4.8 \leq 5.0$	4.846	4.832	-
$f_{osc}[b_{1111}]$@0.35V	GHz	$\geq 3.7 \leq 3.9$	3.745	3.814	-
PN$[b_{0000}]$@10kHz	dBc/Hz	$\leq$ -59	-71.6	-72.4	-1.1%
PN$[b_{0000}]$@100kHz	dBc/Hz	$\leq$ -86	-93.0	-94.1	-1.2%
PN$[b_{0000}]$@1MHz	dBc/Hz	$\leq$ -108	-113.1	-114.3	-1.1%
PN$[b_{0000}]$@10MHz	dBc/Hz	$\leq$ -129	-133.0	-134.2	-0.9%
PN$[b_{1111}]$@10kHz	dBc/Hz	$\leq$ -65	-76.8	-77.4	-0.8%
PN$[b_{1111}]$@100kHz	dBc/Hz	$\leq$ -92	-97.5	-97.7	-0.2%
PN$[b_{1111}]$@1MHz	dBc/Hz	$\leq$ -113	-117.6	-117.8	-0.2%
PN$[b_{1111}]$@10MHz	dBc/Hz	$\leq$ -134	-137.0	-137.3	-0.2%
power$[b_{0000}]$	mW	n/d	0.139	0.133	-4.3%
power$[b_{1111}]$	mW	n/d	0.139	0.134	-3.6%
fssv$[b_{0000}]$	MHz/V	$\leq$ 500	440	64	-85.5%
fssv$[b_{1111}]$	MHz/V	$\leq$ 500	206	62	-69.9%
FOM$[b_{0000}]$	dBc/Hz	$\geq$ 190	195.3	196.6	+0.7%
FOM$[b_{1111}]$	dBc/Hz	$\geq$ 190	197.1	197.7	+0.3%

between all conflicting performance figures were not properly weighted during LOs. To improve these results, designer insights were again fundamental to redesign iterations/optimizations; still, the output of that process will remain ultimately unpredictable, favoring the proposed "everything-at-once" approach.

VII. CONCLUSION

In RF IC manual design, analyzing multiple performance figures through multiple conflicting modes, test benches and/or analysis at once is an unbearable task. This paper presents an all-inclusive test bench formulation for many-objective sizing optimization, which allows addressing complex RF circuit blocks by following an optimize "everything-at-once" approach and, therefore, properly analyze the optimal trade-offs between all relevant performance figures. The complex class-C/D VCO topology adopted, originally proposed in a renowned international journal of the area, was optimized to produce multiple solutions that either comply with IoT and cellular requirements in a single optimization. Specifically, 28 variables and 18 performance metrics, obtained from four different test benches and/or processing were weighted simultaneously at each iteration of the evolutionary algorithm. The obtained solutions pushed to the limits this circuit topology for a 65-nm CMOS technology and allowed reducing approximately 49% of the power consumption for a similar phase noise cases of the original design, while also proving its capabilities to address ultralow power, with 93% reduction. In addition, WCC criteria were also performed on the top of the worst case tuning range optimization, providing reliable and robust designs that are evaluated and meet specifications over 66 performance metrics and bring the designer closer to a first-pass fabrication success.

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Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's (5-years), master's, and Ph.D. degrees, and the Habilitation degree for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering/IST, TU of Lisbon (since 2013 University of Lisbon), since 1980. Since 1992, he has been on leave from IST, University of Lisbon, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair Professor since 2013. In FST, he was the Dean of the Faculty from 1994 to 1997, and he has been a Vice Rector of the University of Macau since 1997 (in-charge of Research between 2008 and 2018 and now of Global Affairs, from 2018 to 2023). Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 44 theses, 23 Ph.D., and 21 masters. He was a Co-Founder of Chipidea Microelectronics (Macao) [now Synopsys] in 2001/2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in 2011 to the State Key Laboratory of China (the first in Engineering in Macao), being its Founding Director. He has co-authored seven books and 11 book chapters. He holds 30 patents, 28 USA, and two Taiwan. He has co-authored 472 papers, in scientific journals (171) and in conference proceedings (301), and other 64 academic works, in a total of 584 publications.

Dr. Martins was the Founding Chairman of both the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was a General Chair of the 2008 IEEE Asia-Pacific Conference on CAS–APCCAS'2008, and was the Vice President for Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. Since 2011, he has been the Vice President (World) Regional Activities and Membership of IEEE CASS from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, nominated the Best Associate Editor of T-CAS II from 2012 to 2013. Plus, he has been a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2019, and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)-Director of the IEEE. He was a General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference–ASP-DAC'2016 and received the IEEE Council on Electronic Design Automation Outstanding Service Award 2016. He was a Nominations Committee Member of the IEEE CASS from 2016 to 2017 and the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In representation of UM, he was one of the Vice Presidents from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities. He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999 and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese Academician living in Asia.