Fully Differential 4-V Output Range 14.5-ENOB Stepwise Ramp Stimulus Generator for On-Chip Static Linearity Test of ADCs

Guillaume Renaud, Mamadou Diallo, Manuel J. Barragan, *Member, IEEE*, and Salvador Mir, *Member, IEEE*

***Abstract*— This paper presents an on-chip stepwise ramp stimulus generator aimed at static linearity test applications for analog-to-digital converters (ADCs). The proposed ramp stimulus generator is based on a simple switched-capacitor integrator with a constant dc input. The integrator has been conveniently modified to produce a very small integration gain proportional to the capacitance difference of two capacitors, in such a way that the resulting stepwise ramp signal at the output has a step size below the least significant bit (LSB) of the target ADC under test. In order to verify the feasibility of the proposed ramp generation technique, this paper details the design and experimental characterization of a proof-of-concept stepwise ramp generator in a 65-nm CMOS technology. Experimental results on 15 fabricated samples show an average linearity of 14.5 effective bits in a differential output range of ±2 V. Moreover, a discrete-time static linearity measurement strategy is proposed and, as a proof-of-concept validation, it is verified on an off-the-shelf 11-bit ADC using the fabricated generator samples. Experimental results show an accuracy of ±0.3 LSB in the measurement of the integral nonlinearity of the ADC under test.**

***Index Terms*— Analog-to-digital conversion, built-in self-test, design-for-testability, signal generators.**

I. Introduction

THE ever-increasing integration capabilities in current nanometric technologies enable the fabrication of mixed-signal monolithic systems-on-chips (SoCs) and heterogenous systems-in-package (SiP) containing subsystems of very different nature. Testing the digital blocks in these systems is a relatively straightforward task that relies on a variety of standardized design-for-test (DfT) strategies for accessing these blocks and assessing their functionality based on structural tests. On the other hand, testing mixed-signal subsystems, even if they are embedded in a complex SoC or SiP, still relies on a set of functional specification tests specifically tailored for each particular device under test (DUT). Standard functional tests employ specialized automated test equipment for exciting the DUT with an appropriate test stimulus, acquiring the test response, and processing the test results. However, in a complex SoC/SiP, where the external access to the internal blocks is difficult, or even impossible, these operations may turn challenging to perform at a reasonable cost [1]. Indeed, according to published data, a large fraction of the total production cost of a mixed-signal SoC may be dedicated to test [2].

A promising solution to the aforementioned issues is the development of mixed-signal built-in self-test (BIST) techniques. The goal of BIST techniques is to move some of the functionality of the test instrumentation into the DUT, in such a way that generation and manipulation of test signals become internal. This approach eliminates the need of an external analog test access and has the potential of significantly reducing external test instrumentation requirements. Ideally, embedded test instruments would be included together with the DUT and only a low-performance digital tester would be needed to launch the self-test procedure and retrieve the test results. Thus, BIST may reduce the overall production cost of a complex system by taking into consideration the test of its constituent blocks at the design stage. Moreover, BIST solutions also open the door to enhanced reliability, on-line test, and diagnosis features along the complete life cycle of an integrated circuit. Indeed, reliability and quality enhancement is becoming one of the main drivers for the development of analog and mixed-signal BIST. For instance, in safety-critical applications, such as automotive, BIST is even becoming a design requirement in many integrated systems.

Static linearity test of analog-to-digital converters (ADCs) is one of the most challenging and time-consuming tests in the production test of a mixed-signal system. Standard approaches to characterize static linearity consist in applying a high-linearity stimulus to the ADC under test, retrieving and storing a high volume of ADC output samples, and processing these samples to estimate the integral nonlinearity (INL) and differential nonlinearity (DNL) metrics [3]. Given that analog-to-digital conversion is one of the basic functions in a mixed-signal system, moving static ADC testing on-chip in a full BIST framework can enable a huge reduction in the production cost of these complex systems. In this line, one of the key challenges for adapting standard ADC static tests to a full-BIST scheme is to provide an appropriate test stimulus to excite the converter. Indeed, providing an appropriate test stimulus generator for on-chip static test applications has been an open research problem for over a decade. As it is usually accepted by the industry, standard test techniques for static linearity characterization require a test stimulus whose linearity is 2–3 bits above the linearity of the ADC under test. Given that ADC resolutions are steadily increasing, this has

Manuscript received June 5, 2018; revised September 8, 2018; accepted October 16, 2018. *(Corresponding author: Manuel J. Barragan.)*

G. Renaud was with TIMA Laboratory, CNRS, Grenoble INP, Université Grenoble Alpes, 38000 Grenoble, France. He is now with CEA-Leti Minatec, 38054 Grenoble, France.

M. Diallo, M. J. Barragan, and S. Mir are with TIMA Laboratory, CNRS, Grenoble INP, Université Grenoble Alpes, 38000 Grenoble, France (e-mail: manuel.barragan@univ-grenoble-alpes.fr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2018.2876976

become a major issue for the development of on-chip static linearity test solutions.

The main goals of this paper are the design and experimental validation of a novel on-chip ramp stimulus generator suitable for on-chip static linearity test applications of ADCs. The proposed generator is based on a simple switched-capacitor (SC) integrator whose input stage has been conveniently modified to produce a very small integration gain proportional to the difference of two capacitances. Thus, as response to a dc input reference, the integrator outputs a controlled stepwise ramp signal with a small step size.

The rest of this paper is organized as follows. In Section II, we present some relevant previous studies on ramp stimulus generation for on-chip static test applications. Then, in Section III, we outline the proposed ramp generation technique and the associated discrete-time static linearity measurement strategy. Section IV details the practical implementation of the ramp signal generator in STMicroelectronics 65-nm CMOS technology. In Section V, we present some relevant experimental results to demonstrate the performance of the proposed ramp generator and the feasibility of the presented test strategy. Section VI presents a discussion on the possible applications and tradeoffs of the proposed on-chip ramp stimulus generator within a complete BIST scheme. Finally, in Section VII, we summarize the main contributions of this paper.

II. Previous Work

The development of embedded test instruments for generating linear ramp stimuli in ADC static linearity test applications remains an open research topic, and several studies in this line have been presented in the last years. Mainly, two basic architectures of on-chip ramp signal generators have been explored in the literature: 1) ramp generators based on analog integrators and 2) ramp generators based on digital-to-analog converters (DACs).

In essence, integrator-based ramp generators rely on a controlled current source that charges a capacitor in order to generate a ramp voltage signal [4]–[10]. The classic work in [4] presents a closed-loop ramp generator with a feedback circuitry that controls the slope of the generated ramp signal. However, the feedback circuitry only guarantees the correctness of the starting and ending voltages and not the linearity of the generated ramp. The work in [5] presents a quasi-static voltage ramp generator based on a cascode current source that charges a large capacitor with a small current. A voltage buffer is added at the output to prevent current leakage. Simulation results show a maximum DNL estimation error of 0.03 LSB in the static test of a 10-bit ADC.

References [6]–[8] further develop integrator-based generators by adding a calibration loop. The authors present a generation strategy based on integrating a constant current source in a large capacitor, while a calibration loop is proposed to compensate the effect of process variations in the generated ramp slope. In this line, the work in [9] proposes three different ramp generator designs featuring an adaptive scheme to calibrate the linearity of the generated ramp. Experimental results on fabricated samples show a maximum linearity of 11 bits in a voltage range from 0.7 to 1.3 V.

On the other hand, static stimulus generators based on a modified DAC design have been proposed in [11]–[13]. These studies take advantage of a deterministic dynamic element matching (DDEM) technique for relaxing the linearity requirements of the DAC for static test applications of ADCs. The authors demonstrate that an 8-bit DAC with the proposed DDEM strategy can be used for testing a 12-bit ADC. References [13] and [14] use a DAC–ADC loopback configuration in which the effective resolution of DAC and ADC are raised by appropriately scaling and shifting the output of the DAC. The use of segmented resistor-string DACs as an on-chip static stimulus generator has been explored in [15]. Digital $\Sigma\Delta$ encoding has been also proposed for generating triangular waves [16], [17]. These studies employ a digital $\Sigma\Delta$ bitstream encoding a high-resolution triangular wave followed by a 1-bit DAC and a lowpass filter to remove the shaped quantization noise.

Recent works on static linearity test of ADCs focus on relaxing the stringent requirements of standard static test. Thus, the studies in [18]–[20] present a DfT strategy aimed at relaxing the linearity of the test stimulus, while the studies in [21]–[27] are targeted at reducing the number of necessary measurements for a complete static characterization, hence reducing the static test time. Extending these DfT methodologies to a full-BIST scheme still requires the integration of a static test stimulus generator on-chip.

Some of the authors of this paper recently presented a simple discrete-time integrator-based ramp stimulus generator based on a modified SC integrator. The proposed generation strategy was first outlined in [28] and further developed in [29], where the basis of the proposed generation technique is validated using behavioral and electrical simulations. In this paper, we extend our previous work in a number of ways. First, we provide a comprehensive description of the proposed stepwise ramp signal generation technique and the associated discrete-time linearity measurement strategy. Second, we present a detailed design methodology for the proposed ramp generator including newly developed practical design equations based on an analytical study of the main nonidealities in the proposed circuitry. Third, we present in detail the design of a prototype of the proposed generator using the described design methodology in a 65-nm CMOS technology. Fourth, the developed prototype has been fabricated and experimentally characterized in the laboratory. Finally, we demonstrate the performance of the designed generator and the accuracy of the proposed discrete-time static linearity measurement strategy in an actual test application, by characterizing the static linearity of an off-the-shelf 11-bit ADC.

III. Stepwise Ramp Generation for ADC Static Linearity Measurements

A. Proposed Signal Generation Technique

Conceptually, the proposed ramp stimulus generation technique is based on the operation of a two-input SC integrator. Fig. 1 shows a simplified schematic of the proposed ramp

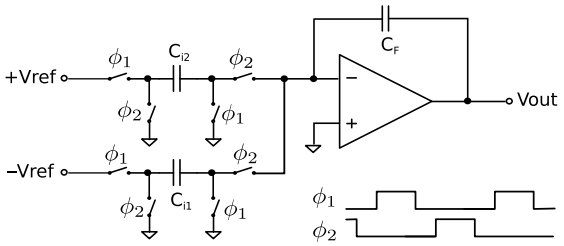


Fig. 1. (a) Conceptual schematic of the proposed ramp signal generator. (b) Diagram of the generator nonoverlapping clock phases.

generator to illustrate the generation strategy (a single-ended schematic is shown for simplicity). As shown in Fig. 1, the core of the proposed generator is an SC integrator that operates with two nonoverlapping clock phases ϕ_1 and ϕ_2. Assuming that the integrator is excited by dc voltages V_{ref} and $-V_{\text{ref}}$, the output voltage of the integrator, neglecting second-order effects, is given as

$$V_{\text{out}}(n) = V_{\text{out}}(n-1) + \frac{C_{i2} - C_{i1}}{C_F} V_{\text{ref}} \tag{1}$$

at the end of the integration phase, that is, at time $t = nT_{\text{clk}}$, where T_{clk} is the integrator clock period, C_F is the feedback capacitor, and C_{i1} and C_{i2} are the input capacitors. As can be derived from (1), the integrator output voltage evolves, ideally, as a stepwise ramp signal with a constant step that depends on the capacitance difference between the two input capacitors. Assuming that $C_F \gg C_{i2} - C_{i1}$, this step can be made small, in such a way that in a given ADC static test scenario, it could be made significantly smaller than the least significant bit (LSB) of the ADC under test. In other words, the proposed technique offers a feasible and simple strategy for providing a high-resolution discrete-time ramp stimulus that can be suitable for ADC static test. However, it has to be taken into account that practical limitations of the proposed stepwise generation strategy may impact the accuracy of the test. On the one hand, the discrete nature of the proposed ramp generator introduces a quantization error in the measurements, and on the other hand, nonidealities in the practical implementation of the ramp generator may impact the resolution and linearity of the generated ramp, degrading the accuracy of the measurements.

B. Measuring ADC Static Linearity Metrics Using Stepwise Ramp Stimuli

The static nonlinearity of an n_b-bit ADC is usually characterized in terms of the DNL and INL metrics of the set of its transition thresholds $\{t_i\}$, for $i = 1, \ldots, 2^{n_b} - 1$. In an ideally linear ADC, the code bin width, i.e., the distance between two consecutive transition thresholds, t_i and t_{i+1}, is a constant, usually called the LSB of the ADC. However, in a practical ADC, the positions of the transition thresholds are affected by a number of error sources, such as component mismatch, parametric process variations, temperature-dependent variations, and so on. Thus, DNL measures the deviation in the code widths with respect to the ideal code width, while INL measures the deviation of the transition threshold positions from their ideal positions. In this paper, we define the ideal transition levels of an n_b-bit ADC by the fit line passing through the first and last transition thresholds in the ADC static transfer curve, i.e., t_1 and $t_{2^{n_b}-1}$, respectively. The LSB, i.e., the ideal code width, is then defined by

$$\text{LSB} = \frac{t_{2^{n_b}-1} - t_1}{2^{n_b} - 2}. \tag{2}$$

The DNL and INL associated with the transition threshold t_i, for $i = 1, \ldots, 2^{n_b} - 2$, expressed in LSB units, can be evaluated as a function of the actual code widths as

$$\text{DNL}(i) = W_i - 1 \tag{3}$$

$$\text{INL}(i) = \sum_{j=1}^{i} \text{DNL}(j) = \sum_{j=1}^{i} W_j - i \tag{4}$$

where $W_i = (t_{i+1} - t_i)/\text{LSB}$ are the actual code widths of the ADC, expressed in LSB units. It is clear from (3)–(4) that characterizing the static linearity of an ADC is equivalent to accurately measuring the set of its code widths $\{W_i\}$. In this paper, we propose a simple strategy for estimating the code widths of a converter based on exciting the ADC under test with a stepwise ramp signal such as the one generated by the described ramp signal generator.

Let us consider an n_b-bit ADC excited by a linear stepwise ramp signal, as the one in (1), and let us assume that the step size, S, of the ramp stimulus is smaller than the ideal LSB of the ADC under test, that is

$$S = \frac{C_{i2} - C_{i1}}{C_F} V_{\text{ref}} < \text{LSB} \tag{5}$$

with the same notation defined in (1). In this scenario, it is possible to estimate the code widths by simply counting, in the digital domain, the number of generator clock cycles (i.e., the number of steps of the stepwise ramp) between two consecutive code transitions at the converter output. Thus, the DNL for each transition threshold can be estimated as

$$\text{DNL}^*(i) = m_i \hat{S} - 1 = \text{DNL}(i) + \epsilon_i \tag{6}$$

where $\text{DNL}(i)$ is the actual DNL associated with the transition threshold t_i, m_i is the number of steps of the stepwise ramp between transition thresholds t_i and t_{i+1}, $\hat{S}$ is the step size of the ramp stimulus normalized to the LSB, and $\epsilon_i \in (-\hat{S}, +\hat{S})$ is a quantization error term due to the discrete nature of the measurement. Under the assumption in (5) that the ramp step size is smaller than the converter LSB, (6) provides a good estimation of the converter $\text{DNL}(i)$ within the accuracy range $(-\hat{S}, +\hat{S})$. However, computing $\text{INL}(i)$ from the $\text{DNL}^*(i)$ estimation using the definition in (4) leads to inaccurate estimations of the INL

$$\text{INL}^*(i) = \sum_{j=1}^{i} \text{DNL}^*(j) = \text{INL}(i) + \sum_{j=1}^{i} \epsilon_j \tag{7}$$

where $\text{INL}(i)$ is the actual INL associated with the transition threshold t_i. That is, $\text{INL}^*(i)$ is an estimation of $\text{INL}(i)$ within the accuracy range $(-i\hat{S}, +i\hat{S})$. Note that the accuracy of this estimation decreases linearly with the transition threshold

index, i, due to the accumulation of the measurement quantization error. Indeed, for high values of i, the contribution of the accumulated error term may dominate the estimation of the INL, which renders the estimation practically meaningless. In this paper, we propose a simple postprocessing correction that allows canceling the accumulation of the quantization error. Let us assume that the magnitude of the measurement quantization error is significantly smaller than the LSB of the ADC (i.e., assuming $S \ll$ LSB) and let us denote by ϵ the average value of ϵ_i. Under these assumptions, the accumulation of the measurement error in the estimation of INL(i) can be approximated as

$$\mathrm{INL}^*(i) \simeq \mathrm{INL}(i) + \epsilon i. \tag{8}$$

According to (8), the accumulation of the error is approximately linear in the transition threshold index i, and hence, it can be easily compensated by subtracting the best-fit line of the INL$^*(i)$ curve, adapting the classical best-fit technique proposed in [30]. Thus, the compensated INL estimation, $\mathrm{INL}^*_{\mathrm{comp}}(i)$, can be expressed as

$$\mathrm{INL}^*_{\mathrm{comp}}(i) - \sum_{j=1}^{i} m_j \hat{S} - \mathrm{INL}^*(1) - \frac{\mathrm{INL}^*(2^{n_b}-1) - \mathrm{INL}^*(1)}{2^{n_b}-2}(i-1) \tag{9}$$

which, under our assumptions, can be approximated as

$$\mathrm{INL}^*_{\mathrm{comp}}(i) \simeq \mathrm{INL}(i) + \epsilon'_i \tag{10}$$

where the quantization error term is contained in the interval $\epsilon'_i \in (-\hat{S}, +\hat{S})$.

Equations (6) and (10) show that the described measurement strategy provides estimations of the DNL and INL metrics of an ADC, respectively, as a function of the discrete number of steps between two consecutive code transitions at the converter output, within the accuracy limits of the step size of the stepwise ramp stimulus used for exciting the ADC.

C. Performance Limits of the Proposed Signal Generation Technique

As shown in Section III-B, a small step size is critical for the accuracy of the proposed discrete measurement strategy. The proposed stepwise ramp generation strategy is based on introducing a small difference between the two capacitors in order to achieve a small step size. However, this technique, despite being simple, is prone to variations of the step size due to random mismatch in the capacitors and, moreover, nonidealities such as integrator leakage, amplifier offset, settling errors, noise, and so on, may have also an impact on the quality of the generated ramp stimulus in terms of resolution and linearity.

Throughout this paper, we will refer to the *resolution* of the generated stepwise ramp signal to denote the number of step levels defined by the ramp signal in a given full-scale (FS) voltage range. Thus, in this paper, we define the resolution, N, of the generated stepwise ramp, measured in bits, as

$$N = \log_2 n_{\mathrm{steps}} \tag{11}$$

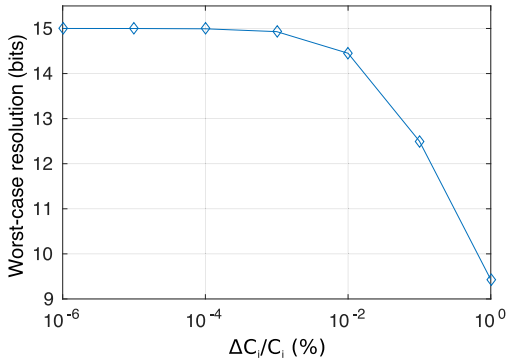


Fig. 2. Worst case resolution of the generated stepwise ramp stimulus as a function of the input capacitor mismatch, for a ramp signal generator with an ideal resolution of 15 bit.

where n_{steps} is the number of step levels in the stepwise ramp in the complete FS range. Under ideal operation conditions, n_{steps} can be expressed as

$$n_{\mathrm{steps}} = \frac{FS}{\frac{C_{i2}-C_{i1}}{C_F} V_{\mathrm{ref}}}. \tag{12}$$

On the other hand, the *linearity* of the generated stepwise ramp will be evaluated in terms of its Integral Nonlinearity, $\mathrm{INL}_{\mathrm{ramp}}$, defined as the maximum absolute deviation from the best linear fit of the generated ramp (in a least squares sense) and expressed as an equivalent number of bits, $\mathrm{ENOB}_{\mathrm{static}}$, as defined in [6]

$$\mathrm{ENOB}_{\mathrm{static}} = \log_2 \frac{\mathrm{FS}}{\mathrm{INL}_{\mathrm{ramp}}}. \tag{13}$$

1) Capacitor Mismatch: Capacitor mismatch is undoubtedly one of the key limiting factors for the resolution of the proposed ramp generator. As it is easily derived from (1), random variations of the capacitance value of capacitors C_{i1}, C_{i2}, and C_F have a direct impact on the size of the step in the stepwise ramp. The output voltage of the integrator shown in Fig. 1 at time $t = nT_{\mathrm{clk}}$ including the effect of mismatch can be modeled as

$$V_{\mathrm{out}}(n) \cong V_{\mathrm{out}}(n-1) + \left(\frac{C_{i2}-C_{i1}}{C_F} + \frac{\sqrt{2}\Delta C_i}{C_F} \right) V_{\mathrm{ref}} \tag{14}$$

where ΔC_i is the random variation of capacitance due to mismatch of the input capacitors. It is assumed that $\Delta C_{i1} \cong \Delta C_{i2}$, $C_{i1} \cong C_{i2}$, and $C_F \gg C_{i2} - C_{i1}$. As it is clear from (14), the linearity of the ramp is not affected by capacitor mismatch: the size of the step deviates from the nominal, but it remains constant throughout the complete FS of the ramp.

It is important to note that $|\Delta C_i / C_F|$ should be minimized in order to ensure that the nominal step size of the ramp is larger than the contribution of the mismatch in (14). That is, for a practical ramp generator, it has to be verified that

$$\frac{C_{i2}-C_{i1}}{C_F} \gg \sqrt{2} \left| \frac{\Delta C_i}{C_F} \right|. \tag{15}$$

Fulfilling the condition in (15) represents a feasibility limit for the practical implementation of the proposed ramp generator in a given technology. Under this feasibility condition, Fig. 2 shows the evolution of the worst case resolution for

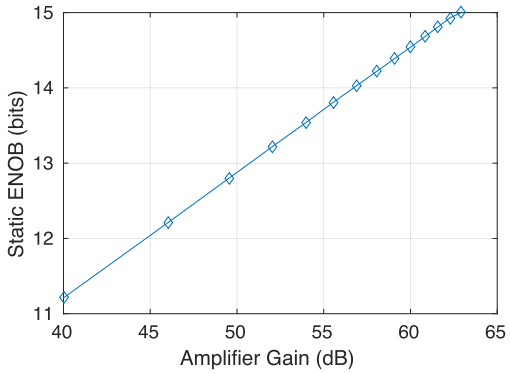


Fig. 3. Static effective number of bits of the generated stepwise ramp stimulus as a function of the amplifier gain in the integrator, for a ramp signal generator with an ideal resolution of 15 bit.

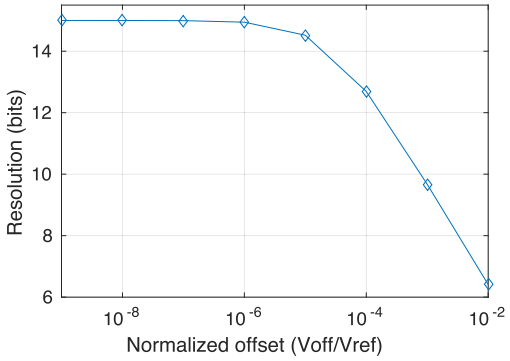


Fig. 4. Resolution of the generated stepwise ramp stimulus as a function of the amplifier input offset, for a ramp signal generator with an ideal resolution of 15 bit.

the generated ramp stimulus as a function of the maximum relative mismatch, $\Delta C_i/C_i$, affecting the input capacitors, for a ramp generator with a 15-bit ideal resolution. These results were obtained by simulating a MATLAB behavioral model of the generator in Fig. 1 under capacitor mismatch conditions, based on the analytical behavior in (14). As it is clearly shown in Fig. 2, an increase in the relative mismatch level results in a significant degradation of the resolution of the generated ramp.

2) Integrator Leakage: Integrator leakage is a direct consequence of the finite gain of the operational amplifier in the SC integrator. As a result, instead of the ideal behavior in (1), only a fraction α of the previous integrator output sample is added in each integration cycle. The output voltage of the integrator shown in Fig. 1 including the effect of leakage at time $t = nT_{\text{clk}}$ is given as

$$V_{\text{out}}(n) = \alpha V_{\text{out}}(n-1) + gV_{\text{ref}} \tag{16}$$

where α and g are given as

$$g \cong \frac{C_{i2} - C_{i1}}{C_F}\left(1 - \frac{1 + \frac{C_{i2}-C_{i1}}{C_F}}{A_0}\right) \tag{17}$$

$$\alpha \cong 1 - \frac{C_{i2} - C_{i1}}{C_F A_0} \tag{18}$$

where A_0 is the finite open-loop gain of the amplifier in the integrator. It is clear that the cumulative effect of the integrator leakage has a direct impact on the linearity of the generated ramp stimulus. Thus, Fig. 3 shows the evolution of the static ENOB of the generated ramp stimulus as a function of the amplifier gain, for a ramp generator with a 15-bit ideal resolution. These results were obtained by simulating in MATLAB a behavioral model of the generator in Fig. 1 under finite gain conditions, based on the analytical behavior in (16)–(18). As can be seen, reducing the gain of the amplifier in the integrator yields a significant degradation of the linearity of the generated ramp.

3) Amplifier Input Offset: In the proposed generator architecture depicted in Fig. 1, an uncompensated offset V_{off} at the input of the amplifier would be integrated together with the reference voltage, in such a way that the output of the integrator at time $t = nT_{\text{clk}}$ would be given as

$$V_{\text{out}}(n) = V_{\text{out}}(n-1) + \frac{C_{i2}-C_{i1}}{C_F}V_{\text{ref}} + \left(1+\frac{C_{i2}+C_{i1}}{C_F}\right)V_{\text{off}}. \tag{19}$$

The integration of the offset can significantly affect the step size of the generated ramp signal. Similar to the effect of capacitor mismatch, the offset of the amplifier affects the resolution of the generated ramp, but not its linearity. Nevertheless, taking into account that C_{i1} and C_{i2} would be approximately equal to assure a small step size under nominal conditions, an uncompensated input offset may even become the dominant contribution to the evolution of the output. In order to avoid this issue, for a practical implementation of the proposed generator, it has to be verified that

$$\frac{C_{i2} - C_{i1}}{C_F}V_{\text{ref}} \gg \left(1 + \frac{C_{i2} + C_{i1}}{C_F}\right)|V_{\text{off}}|. \tag{20}$$

Fig. 4 shows the results of a MATLAB behavioral simulation of the proposed generator taking into account the effect of a positive input offset, for a generator with a 15-bit ideal resolution and assuming $(C_{i1}/C_F) \cong (C_{i2}/C_F) = 0.1$. As it can be seen, a positive input offset can degrade significantly the resolution of the generated ramp stimulus.

An uncompensated negative offset can be even more harmful if the feasibility condition in (20) does not hold. In that case, the contribution of a negative offset in (19) could cancel the ideal integration step produced by the capacitance difference between the input capacitors, hence, destroying the functionality of the generator.

4) Settling Error: Ideally, the discrete-time integrator shown in Fig. 1 performs the cumulative sum in (1) that defines the desired ramp stimulus. However, a nonideal dynamic behavior of the integrator may introduce a settling error in the evolution of the output, hence, deviating from this ideal behavior. Neglecting second-order dynamic effects due to the parasitic resistances and capacitors associated with the SC network, the dynamic behavior of an integrator with nonideal settling can be easily modeled using a one-pole approximation for the dynamics of the amplifier, together with a maximum current limitation. In such a model, the settling of the integrator output is defined by two parameters: the Gain–Bandwidth product,

GBW, and the Slew-Rate (SR) of the amplifier. For the sake of readability, in the following analysis, we will consider a time and frequency normalization to a sampling frequency of one, that is

$$\begin{aligned} T_{\text{clk}} &= 1 \\ \text{SR} &= \text{SR}^* \times f_{\text{clk}} \\ \text{GBW} &= \text{GBW}^* \times f_{\text{clk}} \end{aligned} \tag{21}$$

where SR and GBW are the conventional slew-rate and gain-bandwidth product, and $f_{\text{clk}} = 1/T_{\text{clk}}$ is the sampling frequency. Parameters SR* and GBW* are the time-normalized versions of the slew-rate and gain–bandwidth product, respectively. Different regions of operation can be considered, depending on parameter t_0 defined as

$$t_0 = \frac{bV_{\text{ref}}}{\text{SR}^*} - \frac{1}{2\pi\,\text{GBW}^*} \tag{22}$$

where $b = ((C_{i2} - C_{i1})/C_F)$ is the integrator gain. Phenomenologically, t_0 indicates the time at which the amplifier stops slewing. If $t_0 \geqslant 0$, the amplifier output slews during its dynamic evolution, introducing this way a nonlinear contribution to the generated ramp signal. On the other hand, if $t_0 < 0$, the amplifier does not slew, the settling is then determined only by the GBW, and is exponentially shaped. At the end of the integration phase, the output voltage can be expressed as

$$V_{\text{out}}(n) = V_{\text{out}}(n-1) + bV_{\text{ref}}(1 - e^{-\pi\,\text{GBW}^*}). \tag{23}$$

It is easily seen that in this operation region, the ideal integration gain, b, is decreased by a constant factor that depends on the GBW and the sampling frequency.

In order to guarantee the linearity of the proposed ramp stimulus generator, the operation of the integrator has to be kept in the $t_0 < 0$ region to avoid nonlinear settling errors. In addition, the contribution of the linear settling error in (23) has to be minimized. In a practical implementation and for a given clock frequency for the integrator, these design conditions can be assured by making $t_0 \ll 0$, that is

$$\frac{bV_{\text{ref}}}{\text{SR}^*} \ll \frac{1}{2\pi\,\text{GBW}^*}. \tag{24}$$

5) Noise: Assuming a clean input voltage reference, the main noise contributions in the integrator in Fig. 1 are the thermal noise due to the switches and the noise due to the amplifier. These noise sources are sampled by the input capacitors C_{i1} and C_{i2} during phases ϕ_1 and ϕ_2 together with the reference voltage V_{ref}. The output voltage of the integrator in Fig. 1 at time $t = nT_{\text{clk}}$ including noise contributions is given as

$$\begin{aligned} V_{\text{out}}(n) = V_{\text{out}}(n-1) &+ \frac{C_{i2}}{C_F}[V_{\text{ref}} + N_{2\phi_1}(n-1) - N_{2\phi_2}(n)] \\ &+ \frac{C_{i1}}{C_F}[-V_{\text{ref}} + N_{1\phi_1}(n-1) - N_{1\phi_2}(n)] \end{aligned} \tag{25}$$

where $N_{2\phi_1}$, $N_{2\phi_2}$, $N_{1\phi_1}$, and $N_{1\phi_2}$ represent the noise voltages sampled by capacitors C_{i2} and C_{i1} during clock phases ϕ_1 and ϕ_2, respectively. Note that noise voltages associated with phase ϕ_1 are due to thermal noise from switches in ON state, while noise voltages associated with phase ϕ_2 have contributions from the thermal noise of ON switches and from the amplifier noise. The interested reader is referred to [31] and [32] for a detailed analysis of noise contributions in a multi-input SC integrator. Regarding the proposed ramp generation strategy, (25) imposes a lower limit on the magnitude of the reference voltage V_{ref}. In order to avoid a degradation of the generated ramp due to noise, the reference voltage has to be significantly larger than the sampled noise in the input capacitors. In a practical ADC BIST implementation, this condition can be easily ensured by codesigning the reference voltage of the ADC under test to drive both the ADC and the ramp stimulus generator.

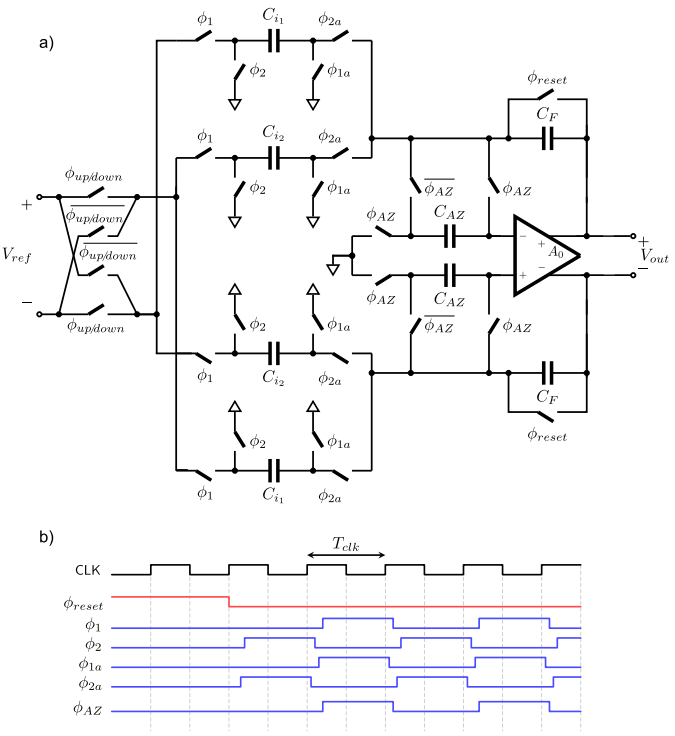


Fig. 5. (a) Block diagram of the proposed differential stepwise ramp signal generator. (b) Timing diagram for the clock phases.

IV. Practical Implementation

In order to demonstrate the feasibility of the proposed ramp stimulus generator, a proof-of-concept prototype was implemented in STMicroelectronics 2.5-V 65-nm CMOS technology. Fig. 5 shows a block diagram of the proposed fully differential implementation. The generator shown in Fig. 5 is a fully differential version of the basic generator shown in Fig. 1. The choice of a fully differential architecture minimizes the effect of parasitics in the SC network, as they naturally tend to compensate between the positive and negative signal paths, and greatly reduce other second-order effects in SC circuits, such as charge injection and clock feedthrough in the switches.

The proposed architecture includes a classical autozero to reduce the influence of the amplifier offset on the generated ramp step size [33]. A switching scheme controlled by digital signal $\phi_{\text{up/down}}$ has been added at the input in order to control the slope (positive or negative) of the generated ramp, and the

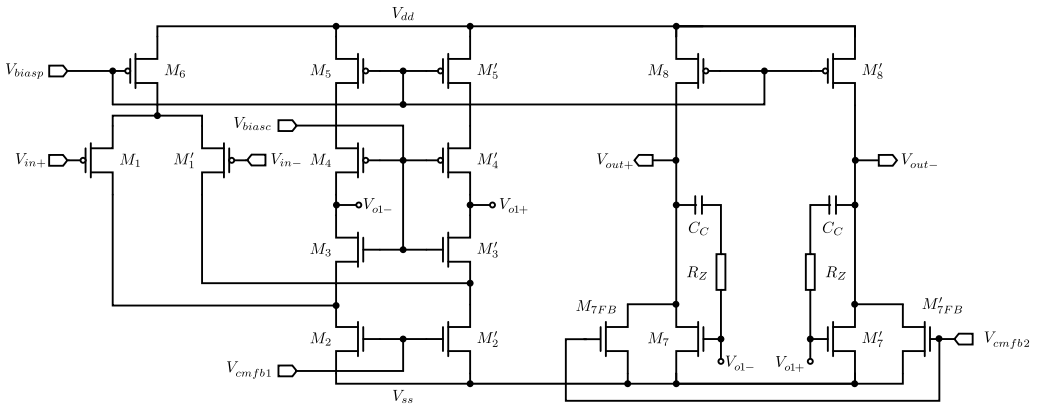


Fig. 6. Transistor-level schematic of the operational amplifier.

TABLE I

SUMMARY OF DESIGN GOALS FOR THE STEPWISE RAMP GENERATION PROTOTYPE

Differential output range	± 2 V
Nominal clock frequency, $1/T_{clk}$	up to 200 kHz
Reference voltage, V_{ref}	1 V
Ramp step size	~ 100 μV
Resolution, N	~ 15 bit
Linearity, ENOB$_{static}$	$\gtrsim 14$ bit

TABLE II

SUMMARY OF REQUIRED DESIGN PARAMETERS FOR THE BUILDING BLOCKS OF THE STEPWISE RAMP GENERATION PROTOTYPE

Amplifier	Open loop gain, A_0	> 80 dB
	Gain-bandwidth product, GBW	$\gtrsim 90$ MHz
	Slew-Rate, SR	~ 100 V/μs
	Output range	$\geqslant \pm 2$ V
	Equivalent input noise	minimize
Auto-Zero	Residual input offset	< 1 μV
Input capacitors	Mismatch, ΔC_i	$\lesssim 0.1$ fF
Switches	Charge injection	minimize

feedback capacitor can be reset by activating the control signal ϕ_{reset} in order to initialize the output ramp. In addition, as it can be seen in the timing diagram, clock phases ϕ_{1a} and ϕ_{2a} are the advanced versions of clock phases ϕ_1 and ϕ_2 that have been added to reduce charge injection during the operation of the sampling switches. The design goal for this ramp generator is to generate a quasi-static stepwise ramp with a step size around 100 μV in a differential FS range of ± 2 V, which, under ideal conditions, represents a nominal resolution around $N = 15.3$ bits. We target a linearity around $\text{ENOB}_{\text{static}} = 14$ bits, which, in a practical test scenario, would be enough for the static test of 11-bit ADCs. Table I summarizes the design goals of the ramp stimulus generator prototype.

To achieve the design goals in Table I, we take advantage of the analytical results in Section III to evaluate the required performance for each of the blocks composing the stepwise ramp generator in Fig. 5. The analysis in Section III imposes the practical limits for the implementation of the proposed stepwise ramp generator concerning technological and design parameters, i.e., the relative mismatch level affecting the input capacitors, the input offset in the integrator, the open-loop gain of the amplifier in the integrator, and the dynamic performance of the amplifier. Table II summarizes the main design parameters for the building blocks of the stepwise ramp generator to achieve the desired performance, according to the analytical results in (14)–(24). Since the problem has multiple degrees of freedom within the constraints of the feasibility conditions in (15), (20), and (24), conservative goals have been set to make the contributions of amplifier nonidealities negligible, while the requirements on mismatch have been relaxed to reduce the area of the capacitors. As it will be shown in Sections IV-A–IV-D, this choice makes the capacitor mismatch the main limiting factor for the resolution of the described implementation of the stepwise ramp generator.

Sections IV-A–IV-D illustrate in detail the implementation of the different blocks composing the ramp stimulus generator, i.e., the operational amplifier, the capacitors, and the switches.

A. Operational Amplifier

Fig. 6 shows a transistor-level schematic of the designed amplifier. The selected design is a standard fully differential two-stage folded-cascode topology with a Miller compensation using a nulling resistor (the bias voltage circuitry and common-mode feedback networks are not shown for simplicity). The selected topology offers a good tradeoff between the amplifier performance (in terms of static gain and dynamic behavior) and simplicity of design.

Two dynamic common-mode feedback networks were designed to independently compensate the output common mode deviations of both the first and second stages of the amplifier. Fig. 7 shows the schematic of the common-mode feedback networks [34]. They consist in a dynamic SC network clocked at nonoverlapping clock phases ϕ_1 and ϕ_2. The output common mode of each stage is sampled and compared to references V_{cmref1} and V_{cmref2} for the first and second stages, respectively. Then, compensation signals are fed back to the amplifier to compensate deviations of the output common mode of each stage. Common-mode compensation signal V_{cmfb1} controls the biasing of transistors M_2 and M'_2, while the compensation of the second stage is applied in current mode, through auxiliary transistors $\text{M}_{7\text{FB}}$ and $\text{M}'_{7\text{FB}}$.

Transistors were sized using the g_m/I_D methodology [35] with the design goals in Table II in the selected 2.5-V 65-nm

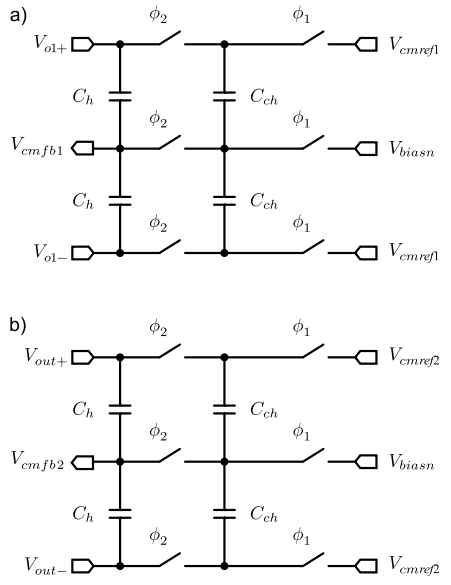


Fig. 7. Common-mode feedback circuits for (a) first stage and (b) second stage of the amplifier.

TABLE III
SIZING OF AMPLIFIER COMPONENTS

MOSFETs	W/L (μm/μm)	Capacitors	Value
M1-M1′	100/0.3	C_C	2.94 pF
M2-M2′	32/0.8	C_{ch}	495 fF
M3-M3′	30/0.48	C_h	495 fF
M4-M4′	310/1		
M5-M5′	310/1	**Resistors**	**Value**
M6	5/2	R_Z	601 Ω
M7-M7′	12/0.3		
M8-M8′	475/0.3		
M7FB-M7FB′	0.5/0.3		

TABLE IV
PERFORMANCE PARAMETERS OF THE AMPLIFIER OBTAINED BY ELECTRICAL SIMULATION

Open loop gain, A_0	93 dB
Phase Margin, PM	75°
Gain-bandwidth product, GBW	95 MHz
Slew-Rate, SR	150 V/μs
Output range	±2.3 V
Equivalent input noise	89 μV_{rms}

CMOS technology. Transistors M_2, M_2', M_7, and M_7' were biased in strong inversion to minimize the amplifier noise, while the rest of transistors were biased in moderate inversion as it offers the best area-to-performance tradeoff solution for the desired design goals. Table III lists the dimensions of the transistors, capacitors, and nulling resistors, while Table IV illustrates the main performance figures of the designed amplifier obtained by electrical postlayout simulation. All the obtained performance parameters comply with the design goals for the stepwise ramp generator listed in Table II.

B. Amplifier Offset Autozeroing

Electrical Monte Carlo simulations of the amplifier described in Section IV-A were performed using the Monte Carlo process and mismatch models provided in the Process Design Kit of the selected 65-nm CMOS technology. These simulations show an equivalent input offset that varies with a standard deviation $\sigma_{\text{Voff}} \simeq 1$ mV. According to the analysis in Section III, this input offset would not comply with the feasibility condition in (20). That is, in this scenario, the size of the step in the generated stepwise ramp would be dominated by the contribution of this random offset and not by the difference of the input capacitors as intended by design.

In order to compensate this offset, we have implemented a classical closed-loop autozeroing technique adapted from [33], as shown in Fig. 5. Capacitor C_{AZ} is used to store the amplifier offset during the sampling phase of the integrator and to subtract this offset in the integration phase. The equivalent input-referred residual offset $V_{\text{res,off}}$ can be roughly approximated by

$$V_{\text{res,off}} \sim \frac{V_{\text{off}}}{A_0} + \frac{\Delta q_{\text{inj}}}{C_{\text{AZ}}} \tag{26}$$

where V_{off} is the uncompensated input-referred offset of the amplifier, and Δq_{inj} is the difference of charge injection between the positive and negative paths in capacitors C_{AZ} due to mismatch. Capacitors C_{AZ} were designed as ~ 1 pF metal–oxide–metal (MOM) capacitors in the selected CMOS technology. Using this simple configuration, the residual offset is below 100 nV. Both our theoretical analysis in Section III and extensive electrical simulations show that this residual offset does not have a significant effect on the resolution of the stepwise ramp generator prototype.

C. Capacitors

The sizing of the sampling and feedback capacitors, C_{i1}, C_{i2}, and C_F, respectively, is a key point in the design of the generator given that it defines the nominal size of the step in the generated stepwise ramp signal. According to the design goals in Table I, achieving the target resolution in the desired output swing requires to set the step of the ramp to ~ 100 μV. In order to realize this design goal for the stepwise ramp generator prototype, we propose to make

$$\frac{C_{i2} - C_{i1}}{C_F} V_{\text{ref}} = 100\,\mu\text{V}. \tag{27}$$

This capacitance ratio is feasible in the selected 65-nm CMOS technology by making $C_F = 10$ pF and $C_{i2} - C_{i1} = 1$ fF. Then, according to the choice of design parameters in Table II, we can size the input capacitors C_{i1} and C_{i2} to comply with the mismatch requirement $\Delta C_i \lesssim 0.1$ fF. According to the mismatch model provided in the Process Design Kit of the selected technology, if we implement the input capacitors as ∼1 pF MOM capacitors (i.e., $C_{i1} \sim 1$ pF and $C_{i2} = C_{i1} + 1$ fF), with a geometry of about 100×100 metal 2 to metal 5 fingers, the capacitance value of the input capacitors will vary with a standard deviation $\sigma_C = 0.04$ fF, which, considering a $\pm 3\sigma$ variation, would limit the resolution of the stepwise ramp generator in the range from $N = 14.8$ bits to $N = 15.7$ bits. This is an acceptable tradeoff between the area of the capacitors and the expected variation of the generator resolution for our design goals. In addition, this implementation allows for an easy realization of the desired capacitance difference between C_{i1} and C_{i2} simply by adjusting properly the number

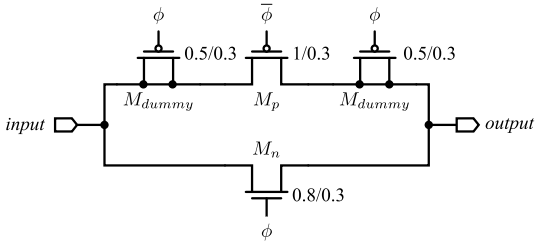


Fig. 8. Transistor-level schematic of the designed CMOS switches.

of fingers. Electrical simulations also show that other second-order effects in the selected MOM capacitors, such as capacitance nonlinearity, do not have a significant contribution to the linearity and resolution of the generated stepwise ramp in the proposed implementation. In addition, the effect of parasitic capacitances due to interconnections and switches in the SC network is minimized by a careful symmetrical layout of the proposed fully differential architecture.

D. Switches

Switches in the integrator were designed as CMOS switches to reduce its equivalent ON resistance along the complete signal range considered. Charge injection due to the switches turning OFF may degrade the performance of the proposed stepwise ramp generator strategy. Indeed, in a single-ended implementation such as the simplified generator in Fig. 1, the effect of charge injection in the sampling capacitors would appear as an uncompensated signal-dependent offset that would be integrated together with the desired ramp steps limiting the resolution and linearity of the ramp generator. In a fully differential implementation, such as the proposed stepwise ramp generator prototype, the effect of charge injection is greatly reduced since the charge injection in the positive and negative paths tend to compensate. To further reduce the effect of charge injection in the input sampling switches, they are designed with two added dummy pMOS transistors as shown in Fig. 8. These dummy transistors are intended to acquire the charge stored in the channel of the pMOS transistor in the switch when it turns OFF when sampling the reference voltage. In addition, two advanced phases ϕ_{1a} and ϕ_{2a} [see Fig. 5(b)] have been introduced to enable bottom plate sampling. The switch at the bottom plate of the capacitor opens before the top plate switch does. When the top plate switch opens, the bottom plate is floating and no charge is injected on the capacitor, further reducing charge injection issues.

An additional concern in the design of the switches is the eventual discharge of the capacitors through its equivalent OFF resistance. Given that the ramp signal generator is aimed at static test applications, this effect has to be carefully considered to ensure a correct charge transfer in the SC integrator at the desired clock frequency. Transistors in the CMOS switch were sized to ensure a correct operation for clock frequencies above 10 kHz.

V. Experimental Results

The described stepwise ramp generator prototype was fabricated in the selected STMicroelectronics 2.5-V 65-nm CMOS technology. Fig. 9(a) shows the layout and floorplan of the

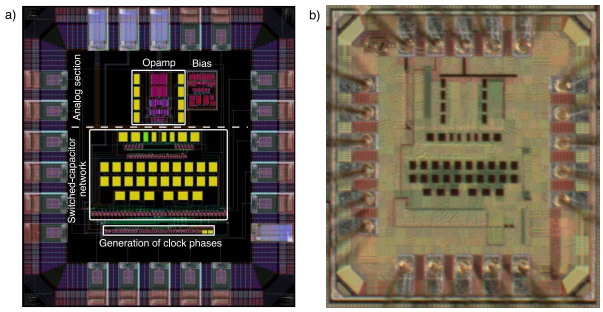


Fig. 9. (a) Layout and floorplan of the stepwise ramp signal generator prototype. (b) Microphotograph of one of the fabricated samples.

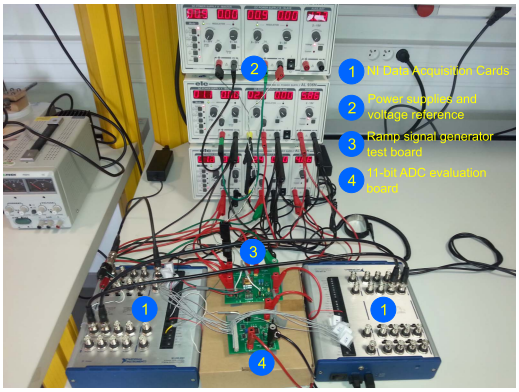


Fig. 10. Photograph of the test setup for the stepwise ramp signal generator prototype.

ramp signal generator prototype. Positive and negative signal paths have been carefully drawn to respect the symmetry of the fully differential architecture, while the analog section is separated from the SC network and digital clock generation circuitry to minimize noise injection due to the switching activity. Fig. 9(b) shows a microphotograph of one of the fabricated chip samples. It occupies an active area of 0.06 mm^2, including the dedicated bias and clock phase generation circuitry. A total of 15 samples were fabricated, packaged, and fully characterized in the laboratory in order to validate the feasibility and performance of the developed ramp signal generator prototype.

Our test setup is depicted in Fig. 10. It makes use of two National Instrument USB-6361 data acquisition cards (DAQs) controlled by a conventional computer. Two sets of experiments are carried out to validate the functionality and performance of the fabricated ramp generator. The first set of experiments is aimed at characterizing the linearity performance of the fabricated ramp generator as a stand-alone circuit. The second set of experiments is aimed at validating the functionality of the fabricated ramp generator in a proof-of-concept static test scenario. In this proof-of-concept, we characterize the linearity of an 11-bit ADC by using the proposed stepwise ramp generator and the static linearity measurement strategy described in Section III-B.

A. Performance of the On-Chip Stepwise Ramp Generator

Our first set of experiments is focused on validating the performance of the proposed ramp signal generator as a

TABLE V
COMPARISON OF THE MEASURED SIGNAL GENERATOR PERFORMANCE WITH PREVIOUS WORK ON ON-CHIP RAMP STIMULUS GENERATION

Reference	Generation technique	Linearity (bits)	Output swing (V)	Area (mm^2)	Technology
This work	Step-wise ramp generation	14.5	–2/2	0.06	65nm CMOS
[4]	Automatic slope adjustment ramp generation	8	–2/2	N/A	N/A
[5]	Current source integration	14*	0.1/0.9	0.11	2.0μm CMOS
[5]	Relaxation oscillator	12*	0.2/1.4	0.51	1.2μm CMOS
[6]	Adaptive triangle-wave generation	14*	–1/1	0.05	0.6μm CMOS
[9]	Error-cancellation Least-Mean-Square integrator	10	N/A	N/A	N/A
[9]	SC fully-differential Least-Mean-Square integrator	11	0.7/1.3	0.18	180nm CMOS
[17]	$\Sigma\Delta$ modulation-based generation	12*	0.4/1.4	0.02	250nm CMOS
[8]	Integration of voltage controlled current source	15*	0/1	0.9	0.5μm CMOS
[10]	Bootstrap integrator-based generator	> 8*	N/A	N/A	180nm CMOS
[15]	Segmented resistor-string DAC	9	0/1.8	0.91	180nm CMOS

* Electrical simulation results.

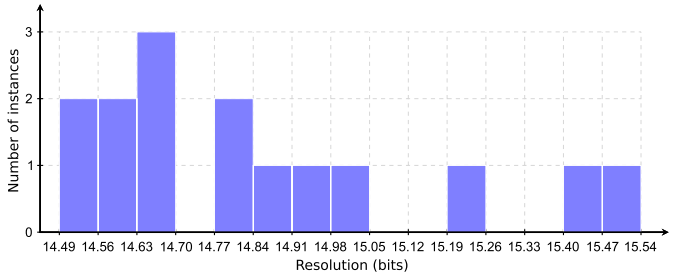


Fig. 11. Histogram of the measured resolution of the generated stepwise ramp signal for the 15 fabricated generator samples.

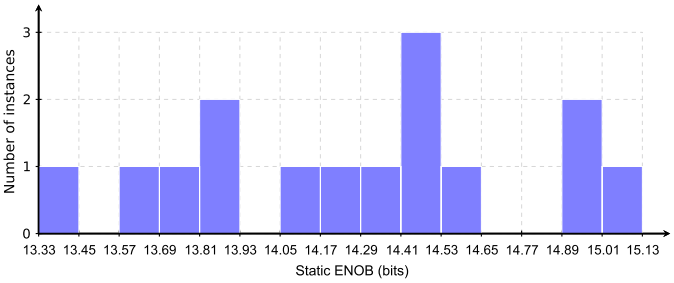


Fig. 12. Histogram of the measured static ENOB of the generated stepwise ramp signal for the 15 fabricated generator samples.

stand-alone device, for the 15 fabricated samples. The instrumentation cards provide the master clock signal for the generator and capture the generated differential analog ramp at the output of the generator with a 16-bit quantizer. The captured signals are then processed in MATLAB to evaluate the resolution and linearity of the generated stepwise ramp signals.

Figs. 11 and 12 show the histograms of the measured resolution and static ENOB, respectively, for the 15 fabricated ramp signal generator samples. These performance metrics were evaluated considering a $\pm$2-V differential output range for the generated ramp signal, while the generator operates at a clock frequency $f_{\text{clk}} = 200$ kHz and with a reference input voltage $V_{\text{ref}} = 1$ V. As can be observed in Fig. 11, the histogram of the measured resolution of the generated ramp signal across the 15 fabricated samples is contained in the range of $N = 14.5$ bits to $N = 15.5$ bits, which matches very well with the predicted resolution range, i.e., $N = 14.8$ bits to $N = 15.7$ bits, due to capacitor mismatch limitations discussed in Section IV-C. The measured linearity of the generated ramp signal is contained in the range of $\text{ENOB}_{\text{static}} = 13.3$ bits to $\text{ENOB}_{\text{static}} = 15.1$ bits, as can be observed in Fig. 12, with an average static ENOB of 14.5 bits, in agreement with our target design specifications. The measured nonlinearity of the fabricated ramp generators can be explained by uncompensated second-order effects such as the nonlinearity of the amplifier gain and the nonlinear behavior of capacitors for large signal values.

Table V compares the measured performance of the proposed stepwise ramp signal generator with other state-of-the-art on-chip ramp generators published in the literature. As can be observed, the proposed stepwise ramp generator compares very well to the state-of-the-art. The proposed ramp signal generator yields one of the highest linearity and output swing figures among the considered references.

B. Static Linearity Measurements Using Stepwise Ramp Stimuli

Our second set of experiments is focused on validating the functionality of the generator in a static test scenario, using the proposed static linearity measurement strategy described in Section III-B. For that purpose, we employ the fabricated stepwise ramp generator to provide the test stimulus for characterizing the static linearity of an off-the-shelf 11-bit ADC. The selected ADC under test is a 10 MSamples/s 11-bit ADC with a differential input range of $\pm$1 V. In this set of experiments, the generated ramp stimulus is fed to an evaluation board containing the ADC under test, while the output codes generated by the ADC are captured by a DAQ. The ramp stimulus generator works in the same operating conditions as in the previous set of experiments. The captured output codes are then processed in MATLAB using the classical histogram test algorithm to extract the INL of the ADC under test [3]. For validating the obtained results, the ADC is also characterized by using the arbitrary waveform generator in one DAQ to excite the ADC with a slow 16-bit analog ramp as a test stimulus. The INL is then extracted for each ADC output code using the histogram test algorithm and the obtained values are stored as a reference for comparison. It is important to remark that this is a proof-of-concept experiment devised to show the equivalence between the proposed on-chip ramp stimulus generator and dedicated external test equipment. In an actual on-chip test application,

TABLE VI
COMPARISON OF THE OBTAINED MEASUREMENT ACCURACY WITH PREVIOUS WORK ON STATIC LINEARITY TESTING

Reference	Brief description of key features	Nature of validation	ADC under test	Accuracy (INL measurement)
This work	On-chip step-wise ramp signal generator	Experimental	11 bit	±0.3 LSB
[5]	On-chip signal generator based on current source integration	Simulation	10 bit	±0.03 LSB (DNL)
[5]	On-chip signal generator based on relaxation oscillator	Simulation	10 bit	±0.15 LSB (DNL)
[11]	On-chip signal generator based on low-resolution DAC with DDEM	Experimental	11 bit	±0.5 LSB
[11]	On-chip signal generator based on low-resolution DAC with DDEM	Experimental	12 bit	±1 LSB
[13]	ADC/DAC loopback test	Experimental	10 bit	±0.4 LSB
[14]	DAC-ADC co-testing	Simulation	12 bit	±0.5 LSB
[20]	Low resolution DAC with polynomial fitting algorithm	Experimental	12 bit	±0.6 LSB
[18]	Stimulus error identification and removal	Experimental	16 bit	±2 LSB
[27]	Error identification and segmented model identification	Simulation	16 bit	±0.8 LSB
[19]	Double histogram strategy	Simulation	16 bit	±1 LSB
[21]	Reduced code linearity testing of pipeline ADCs	Experimental	11 bit	±0.2 LSB
[25]	Transition-code linearity test of pipeline ADCs	Experimental	12 bit	±1.1 LSB
[24]	Code-density testing with non-linearity identification and removal	Experimental	16 bit	±1 LSB

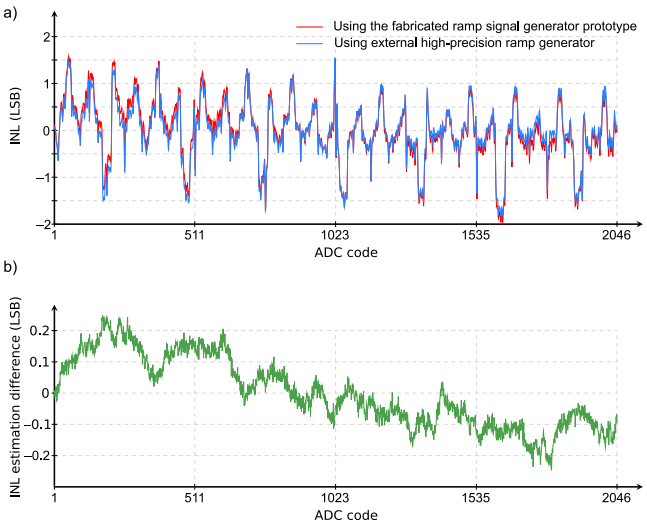


Fig. 13. (a) INL measurements across the complete signal range of the ADC under test using the NI DAQ to provide a high-resolution ramp stimulus, and using the fabricated ramp signal generator. (b) INL estimation difference.

both the ramp stimulus generator and the ADC under test would be integrated into the same die.

Fig. 13 shows the obtained INL per code across the complete output range of the ADC, obtained by exciting the ADC under test with one of the samples of the fabricated ramp signal generator. In this experiment, we selected one representative sample of the generator with $N = 14.5$ bits and $\text{ENOB}_{\text{static}} = 14.1$ bits. Results are compared to the measurements obtained by using the high-precision ramp generated by the instrumentation card. As can be seen, differences in the estimation of INL are well contained in the ±0.25 LSB band. It is interesting to note that, as predicted by (10), the magnitude of the observed INL estimation error agrees very well with the stepwise nature of the generated ramp stimulus, which, for the selected ramp generator sample, has a step size of ∼ 0.2 LSB.

In order to further show the equivalence between our ramp signal generator and the external high-precision test equipment, we measured the maximum INL, INL_{max}, of the ADC under test using the 15 fabricated ramp generator samples. Fig. 14 shows the histogram of the INL_{max} estimation

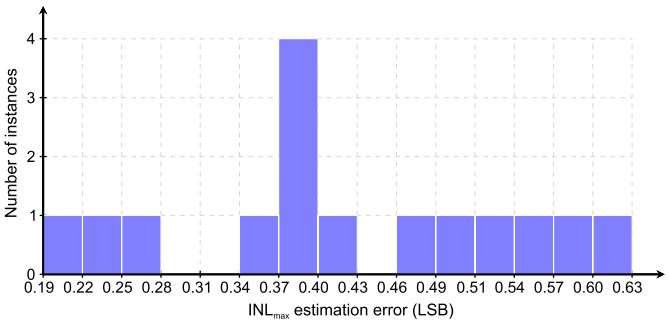


Fig. 14. Histogram of the INL estimation error for the 15 fabricated generator samples.

error in the characterization of the ADC static linearity, for the 15 fabricated ramp generator samples. This INL_{max} estimation error is defined as the difference between the INL_{max} estimation obtained by using the fabricated ramp signal generator, and the INL_{max} measurement obtained by using the high-precision 16-bit ramp provided by the external equipment. As it can be observed, for the 15 fabricated samples, the measured INL_{max} estimation error is contained between 0.2 and 0.6 LSB, with an average INL estimation error of 0.33 LSB, again in agreement with the expected error due to the discrete nature of the stepwise ramp stimulus.

To put the obtained results into perspective, Table VI illustrates a comparison between different static linearity measurement techniques recently presented in the literature. For a fair comparison, it has to be noted that each of the measurement techniques in Table VI is aimed at a different target application. Thus, the studies in [5], [11], and [13] are aimed at static linearity BIST applications of ADCs using embedded signal generators, while the measurement strategies in [18]-[21], [24], and [25] rely on external equipment and dedicated postprocessing to either relax the linearity requirement of the signal generator [14], [18]–[20], reduce the number of necessary measurements [21], [25], or both [24], [27]. The work presented in this paper is aimed at BIST applications, and, as it is given in Table VI, the obtained experimental results compare very well to the state of the art.

VI. Applications

In the view of the obtained experimental results, the proposed on-chip ramp stimulus generator may be employed for the on-chip characterization of the static nonlinearity of moderate-resolution ADCs, in the range up to 11–12 bits. The developed on-chip ramp generator may enable a full-BIST implementation of classic static test techniques, such as the standard static tests in [3], and may be also a key building block for moving advanced reduced-code algorithms on-chip, as discussed in [21]–[27] for the particular case of pipeline, cyclic, and SAR ADCs.

Regarding the practical implementation of static linearity test as a full-BIST, the proposed generator reuses the FS reference voltage of the ADC under test, which simplifies the cointegration of the generator together with the ADC under test, within the tradeoffs discussed in Section III-B. In terms of area overhead, compared to the area of reported state-of-the-art ADCs [36], [37], the proposed generator represents, in average, less than a 10% area overhead. Moreover, the current trends in VLSI design propose the use of system-level test buses for the hierarchical control of embedded mixed-signal test instruments within a complex system [38], [39]. Indeed, this system-level approach may enable sharing the on-chip ramp generator between different ADCs in a VLSI system, which further reduces the overhead. For instance, if an on-chip ramp generator could be shared for the test of the column read-out ADCs in a consumer CMOS imager sensor, the area overhead could be below 0.1% of the total system area. In the future applications, this system-level approach may also allow a complete ADC characterization combining on-chip static and dynamic tests in the same VLSI system by integrating also dynamic stimulus generators, such as the one presented in [40] for $\Sigma\Delta$ ADCs. In this line, the target application defines the type of tests required for the ADCs in the system. Thus, as it is described in [3], static performance is critical for applications such as automatic control, while dynamic performance is critical for audio applications. Imaging applications, on the other hand, demand both static and dynamic tests for an appropriate characterization.

VII. Conclusion

We have presented an on-chip stepwise ramp generator architecture and a discrete-time measurement strategy for a static test of ADCs. The proposed ramp generator is based on a discrete-time SC integrator whose input stage has been modified to produce a very small integration gain. The main nonidealities affecting the performance of the ramp generator and the accuracy of the proposed static linearity measurements have been comprehensively explored, and the analytical design equations for a practical implementation have been provided.

The proposed discrete-time ramp generator has been designed in a 65-nm CMOS technology and its performance has been experimentally validated in the laboratory. Obtained measurements on 15 fabricated samples show an average static ENOB of 14.5 bit, in a ± 2 V differential output range. The feasibility and performance of the proposed static linearity measurement strategy has been verified in an ADC static test scenario with experimental measurements.The fabricated ramp stimulus generator has been employed for characterizing the INL of an off-the-shelf 11-bit ADC. Experimental results show an error in the estimation of the INL of $\sim \pm 0.3$ LSB, compared to reference measurements performed with external high-precision equipment.

References

[1] M. J. Barragán, G. Huertas, A. Rueda, and J. L. Huertas, "(Some) open problems to incorporate BIST in complex heterogeneous integrated systems," in *Proc. 5th IEEE Int. Symp. Electron. Design, Test Appl. (DELTA)*, Jan. 2010, pp. 8–13.

[2] F. Poehl, F. Demmerle, J. Alt, and H. Obermeir, "Production test challenges for highly integrated mobile phone SOCs—A case study," in *Proc. 15th IEEE Eur. Test Symp. (ETS)*, May 2010, pp. 17–22.

[3] *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters*, IEEE Standard 1241-2010 (Revision of IEEE Standard 1241-2000), 2011, pp. 1–139.

[4] C. Jansson, K. Chen, and C. Svensson, "Linear, polynomial and exponential ramp generators with automatic slope adjustment," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 41, no. 2, pp. 181–185, Feb. 1994.

[5] J. Wang, E. Sanchez-Sinencio, and F. Maloberti, "Very linear ramp-generators for high resolution ADC BIST and calibration," in *Proc. 43rd IEEE Midwest Symp. Circuits Syst.*, vol. 2, Aug. 2000, pp. 908–911.

[6] F. Azaïs, S. Bernard, Y. Bertrand, X. Michel, and M. Renovell, "A low-cost adaptive ramp generator for analog BIST applications," in *Proc. 19th IEEE VLSI Test Symp. (VTS)*, Apr./May 2001, pp. 266–271.

[7] S. Bernard, F. Azaïs, Y. Bertrand, and M. Renovell, "A high accuracy triangle-wave signal generator for on-chip ADC testing," in *Proc. 7th IEEE Eur. Test Workshop*, May 2002, pp. 89–94.

[8] E. S. Erdogan and S. Ozev, "An ADC-BiST scheme using sequential code analysis," in *Proc. Design, Autom. Test Eur. Conf. Exhibit.*, 2007, pp. 1–6.

[9] B. Provost and E. Sanchez-Sinencio, "On-chip ramp generators for mixed-signal BIST and ADC self-test," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 263–273, Feb. 2003.

[10] S. Ashwini, M. S. Sivakumar, and S. P. J. V. Rani, "Design of linear ramp generator for ADC," in *Proc. 4th Int. Conf. Signal Process., Commun. Netw. (ICSCN)*, Mar. 2017, pp. 1–5.

[11] H. Jiang, B. Olleta, D. Chen, and R. L. Geiger, "Testing high-resolution ADCs with low-resolution/accuracy deterministic dynamic element matched DACs," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 5, pp. 1753–1762, Oct. 2007.

[12] H. Xing, H. Jiang, D. Chen, and R. L. Geiger, "High-resolution ADC linearity testing using a fully digital-compatible BIST strategy," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 8, pp. 2697–2705, Aug. 2009.

[13] X.-L. Huang and J.-L. Huang, "ADC/DAC loopback linearity testing by DAC output offsetting and scaling," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 10, pp. 1765–1774, Oct. 2011.

[14] Y. Zhuang and D. Chen, "Cost-effective accurate DAC-ADC co-testing and DAC linearization," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (I2MTC)*, May 2018, pp. 1–6.

[15] H.-W. Ting, Z.-T. Wu, J.-Z. Yan, and H.-Y. Wu, "A segmented resistor-string DAC based stimulus generator for ADC linearity testing," in *Proc. 7th Int. Symp. Next Gener. Electron. (ISNE)*, May 2018, pp. 1–4.

[16] B. Dufort and G. W. Roberts, "On-chip analog signal generation for mixed-signal built-in self-test," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 318–330, Mar. 1999.

[17] W. Yong-Sheng, W. Jin-Xiang, L. Feng-Chang, and Y. Yi-Zheng, "A low-cost BIST scheme for ADC testing," in *Proc. 6th Int. Conf. ASIC*, vol. 2, Oct. 2005, pp. 694–698.

[18] L. Jin, K. Parthasarathy, T. Kuyel, D. Chen, and R. L. Geiger, "Accurate testing of analog-to-digital converters using low linearity signals with stimulus error identification and removal," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 3, pp. 1188–1199, Jun. 2005.

[19] M. A. Jalón, A. Rueda, and E. Peralías, "Enhanced double-histogram test," *Electron. Lett.*, vol. 45, no. 7, pp. 349–351, Mar. 2009.

[20] S. Kook, H. W. Choi, and A. Chatterjee, "Low-resolution DAC-driven linearity testing of higher resolution ADCs using polynomial fitting measurements," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 3, pp. 454–464, Mar. 2013.

[21] A. Laraba, H.-G. Stratigopoulos, S. Mir, and H. Naudet, "Exploiting pipeline ADC properties for a reduced-code linearity test technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2391–2400, Oct. 2015.

[22] Z. Yu, D. Chen, R. Geiger, and Y. Papantonopoulos, "Pipeline ADC linearity testing with dramatically reduced data capture time," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, May 2005, pp. 792–795.

[23] E. Peralías, A. Ginés, and A. Rueda, "INL systematic reduced-test technique for pipeline ADCs," in *Proc. 19th IEEE Eur. Test Symp. (ETS)*, May 2014, pp. 1–6.

[24] L. Jin, D. Chen, and R. L. Geiger, "Code-density test of analog-to-digital converters using single low-linearity stimulus signal," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 8, pp. 2679–2685, Aug. 2009.

[25] J.-F. Lin, S.-J. Chang, T.-C. Kung, H.-W. Ting, and C.-H. Huang, "Transition-code based linearity test method for pipelined ADCs with digital error correction," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 12, pp. 2158–2169, Dec. 2011.

[26] N. Jain, N. Agarwal, R. Thinakaran, and R. Parekhji, "Low cost dynamic error detection in linearity testing of SAR ADCs," in *Proc. IEEE Int. Test Conf. (ITC)*, Oct./Nov. 2017, pp. 1–8.

[27] T. Chen, X. Jin, R. L. Geiger, and D. Chen, "USER-SMILE: Ultrafast stimulus error removal and segmented model identification of linearity errors for ADC built-in self-test," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 7, pp. 2059–2069, Jul. 2018.

[28] G. Renaud, M. J. Barragan, and S. Mir, "Design of an on-chip stepwise ramp generator for ADC static BIST applications," in *Proc. 20th Int. Mixed-Signal Test. Workshop (IMSTW)*, Jun. 2015, pp. 1–6.

[29] G. Renaud *et al.*, "A 65 nm CMOS ramp generator design and its application towards a BIST implementation of the reduced-code static linearity test technique for pipeline ADCs," *J. Electron. Test.*, vol. 32, no. 4, pp. 407–421, 2016.

[30] M. Mahoney, *DSP-Based Testing of Analog and Mixed-Signal Circuits*. Los Alamitos, CA, USA: IEEE Computer Society Press, 1987.

[31] L. Toth, I. Yusim, and K. Suyama, "Noise analysis of ideal switched-capacitor networks," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 46, no. 3, pp. 349–363, Mar. 1999.

[32] O. Oliaei, "Thermal noise analysis of multi-input SC-integrators for delta-sigma modulator design," in *Proc. IEEE Int. Symp. Circuits Syst. Emerg. Technol. 21st Century*, vol. 4, May 2000, pp. 425–428.

[33] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[34] O. Choksi and R. Carley, "Analysis of switched-capacitor common-mode feedback circuit," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 12, pp. 906–917, Dec. 2003.

[35] P. Jespers, *The g_m/I_D Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits*. Boston, MA, USA: Springer, 2010.

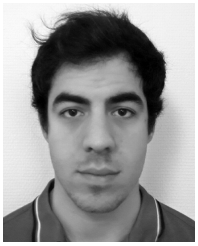
[36] R. Sehgal, F. van der Goes, and K. Bult, "A 12 b 53 mW 195 MS/s pipeline ADC with 82 dB SFDR using split-ADC calibration," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1592–1603, Jul. 2015.

[37] C. Briseno-Vidrios *et al.*, "A 44-fJ/conversion step 200-MS/s pipeline ADC employing current-mode MDACs," *IEEE J. Solid-State Circuits*, to be published, doi: 10.1109/JSSC.2018.2863959.

[38] H. G. Kerkhoff, G. Ali, J. Wan, A. Ibrahim, and J. Pathrose, "Applying IJTAG-compatible embedded instruments for lifetime enhancement of analog front-ends of cyber-physical systems," in *Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr. (VLSI-SoC)*, Oct. 2017, pp. 1–6.

[39] P. Sarson and J. Rearick, "Use models for extending IEEE 1687 to analog test," in *Proc. IEEE Int. Test Conf. (ITC)*, Oct./Nov. 2017, pp. 1–8.

[40] M. J. Barragan *et al.*, "A fully-digital BIST wrapper based on ternary test stimuli for the dynamic test of a 40 nm CMOS 18-bit stereo audio $\Sigma\Delta$ ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 11, pp. 1876–1888, Nov. 2016.



Guillaume Renaud received the M.S. degree in electrical engineering from the Ecole Nationale Supérieure d'Électronique, Informatique, Télécommunications, Mathématique et Mécanique de Bordeaux, Bordeaux, France, in 2012 and the Ph.D. degree in microelectronics from the Université Grenoble-Alpes, Grenoble, France, in 2016, with a focus on the built-in-self-test of pipeline ADCs.

He is currently at the Commissariat à l'Energie Atomique-Leti Minatec, Grenoble, France. His current research interests include design and test of high-performance imagers.

Mamadou Diallo received the M.S. degree in electronic from Montpellier 2 University, Montpellier, France.

From 2007 to 2010, he was at the Engineering School-Microelectronic Department, Polytech Montpellier, Montpellier, France. He was an IC Design Engineer at the LPP Laboratory, Paris, France, where he was involved in the Solar Orbiter project. Since 2014, he has been a Microelectronic Engineer at the French National Research Council, TIMA Laboratory, Grenoble, France. His current research interests include design, layout, and test of IC for supporting research activities at TIMA Laboratory.

Manuel J. Barragan (M'14) received the M.Sc. degree in physics and the Ph.D. degree in microelectronics from the University of Seville, Seville, Spain, in 2003 and 2009, respectively.

He is currently a Researcher at the French National Research Council, TIMA Laboratory, Grenoble, France. His current research interests include topics of test and design for testability of analog, mixed-signal, and RF systems.

Dr. Barragan serves as the Technical Program Committee for the Design, Automation, and Test in Europe Conference, the IEEE European Test Symposium, and the IEEE VLSI Test Symposium. He was a recipient of Silver Leaf Award for the Ph.D. research at the IEEE PRIME conference in 2009 and 2011, the Best Special Session Award in the 2015 IEEE VLSI Test Symposium, and the Best Paper Award in the 2018 European Test Symposium. His work was selected for inclusion in the 20th Anniversary Compendium of Most Influential Papers from the IEEE Asian Test Symposium.

Salvador Mir (M'99) received the Industrial Engineering degree in electrical from the Polytechnic University of Catalonia, Barcelona, Spain, in 1987, and the M.Sc. and Ph.D. degrees in computer science from the University of Manchester, Manchester, U.K., in 1989 and 1993, respectively.

He is currently a Research Director at the TIMA Laboratory, Center National de la Recherche Scientifique, Grenoble, France. He is also the Director of TIMA and a member at the Reliable Mixed-Signal Systems Group, TIMA Laboratory. His current research interests include field of mixed-signal/RF/MEMS test.