A 16-bit 2.0-ps Resolution Two-Step TDC in 0.18-μm CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration

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***Abstract*— This paper proposes a time-to-digital converter (TDC) that achieves wide input range and fine time resolution at the same time. The proposed TDC utilizes pulse-shrinking (PS) scheme in the second stage for a fine resolution and two-step (TS) architecture for a wide range. The proposed PS TDC prevents an undesirable nonuniform shrinking rate issue in the conventional PS TDCs by utilizing a built-in offset pulse and an offset pulsewidth detection schemes. With several techniques, including a built-in coarse gain calibration mechanism, the proposed TS architecture overcomes a nonlinearity due to the signal propagation and gain mismatch between coarse and fine stages. The simulation results of the TDC implemented in a 0.18-μm standard CMOS technology demonstrate 2.0-ps resolution and 16-bit range that corresponds to ∼130-ns input time interval with 0.08-mm^2 area. It operates at 3.3 MS/s with 18.0 mW from 1.8-V supply and achieves 1.44-ps single-shot precision.**

***Index Terms*— Built-in calibration, pulse shrinking (PS), time-to-digital conversion, two step (TS).**

I. Introduction

BASED on the recent progress in CMOS process scaling, time resolution is becoming more and more superior to voltage resolution due to the high-speed transistors and the reduced supply voltage [1], [2]. Recently, a time-to-digital converter (TDC) has been used for various applications, e.g., ADPLLs, space science instruments, jitter measurements, and so on. In particular, with the recent improvement in TDC performance, it is often used in high-precision time-of-flight measurement applications, such as laser range finder [3] and mass spectrometry [4]. It is also used in fluorescence lifetime imaging applications [5]. In these applications, which are the main target applications of this paper, fine time resolution and wide dynamic range are demanded at the same time [6]. Since the TDC determines the overall performance of the measurement, a few ps time resolution with low jitter at a sampling rate of several MS/s is often requested.

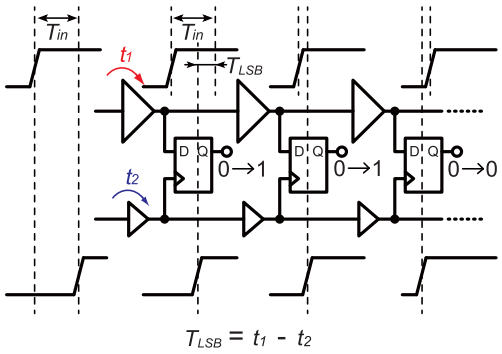

Fig. 1. Simplified schematic of a typical Vernier TDC.

In terms of fine resolution, several time conversion techniques that realize sub-gate-delay resolution have been proposed. A Vernier TDC is widely adopted, thanks to the simplicity of its design concept [6]–[9]. As illustrated in Fig. 1, a typical Vernier TDC needs two independent delay lines that are often implemented as ring delay lines to save area. Two lines have different delay steps, e.g., t_1 and t_2 ($t_2 < t_1$), and thus, the initial time interval T_{in} between two rising transitions gradually shrinks until the moment when the transition in lower delay line catches up with that in the upper one. By tuning the delay difference $T_{\text{LSB}} = t_1 - t_2$, we can realize fine time resolution. However, this architecture requires two independent delay lines, where mismatch between them is inevitable.

On the other hand, a pulse-shrinking (PS) TDC shown in Fig. 2, which is also a type of Vernier TDCs, utilizes the delay difference between rising and falling transitions of a buffer instead of the two independent delay lines [10], [11]. The buffer is intentionally designed to have different rise and fall delays, e.g., t_r and t_f ($t_f < t_r$), and thus, the incoming pulsewidth shrinks $T_{\text{LSB}} = t_r - t_f$ by propagating through each buffer stage until it disappears. Unlike Vernier TDCs,

Manuscript received April 15, 2018; revised July 8, 2018; accepted August 21, 2018. This work was supported in part by JSPS KAKENHI Grant Numbers 26820125 and 17H03244, and in part by the VLSI Design and Education Center, the University of Tokyo in collaboration with ROHM Corporation, Cadence Design Systems, Inc., Synopsys, Inc., and Mentor Graphics, Inc. *(Corresponding author: Tetsuya Iizuka.)*

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Digital Object Identifier 10.1109/TVLSI.2018.2867505

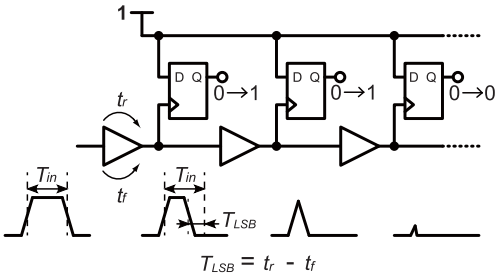

Fig. 2. Simplified schematic of a typical PS TDC.

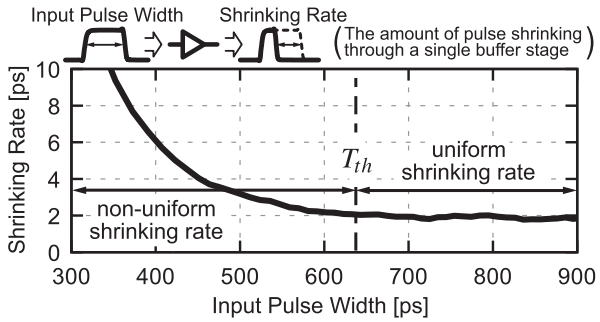

Fig. 3. Simulated PS rate versus input pulsewidth.

PS TDC is realized with a single delay line that amounts to less area and power. It also alleviates the mismatch issue because both rising and falling transitions propagate the same way on the layout. The typical PS TDC, however, has to treat the input time interval as a pulse, which could be impossible for a few ps time interval input [12]. It also has difficulty in resolving the narrow input pulse with fine resolution because the PS rate becomes nonuniform, as shown in Fig. 3, when its width shrinks narrower than a certain threshold T_{th}, which is roughly equal to the sum of signal transition times for the buffer output to fully swing from low to high and from high to low [11]. Though the conventional PS TDC can be used with a fixed offset pulsewidth to keep the input pulse sufficiently wide to accept the fine time difference, it wastes time and power to wait for the conversion of the offset part and it also integrates extra jitter. Due to these drawbacks, the PS TDCs have been used only for limited applications that request a coarse time resolution, i.e., several tens of ps [10].

The architecture of the TDCs discussed so far focused on fine time resolution. However, for a wide dynamic range, it may become unattractive. For example, a Vernier TDC that has an N-bit and τ time resolution uses 2^N delay elements and has $\tau \times 2^N$ dynamic range. If the time resolution τ is reduced by half, the dynamic range is also halved. Then, to keep the same dynamic range, the TDC requires additional 2^N delay elements that increase area occupation, slow down conversion rate, and increase jitter accumulation as N becomes larger. A looped TDC architecture is one of the simplest ideas to extend the dynamic range while preventing area increase [13]. A loop counter determines how many times the start signal rotates on the loop until the stop signal catches up. The overall conversion result can be calculated from the counter output and the thermometer code provided by the DFFs. In an ideal situation the input range can be expanded infinitely just by adding more bits in the counter. However, the issues on the conversion rate and jitter accumulation have not been solved.

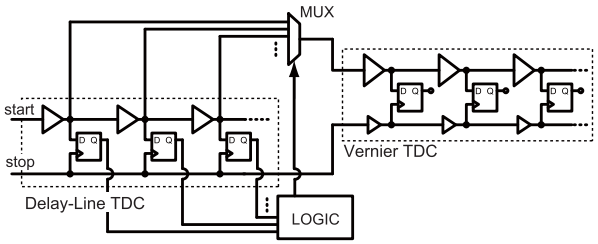

Fig. 4. Schematic of a typical TS TDC [14], [15].

For long time interval measurements, the conversion time and jitter accumulation can be reduced by a two-step (TS) approach depicted in Fig. 4. The TS TDC is composed of two TDCs: one has a coarse time resolution and wide range (a coarse TDC) and the other has a fine resolution and narrow range (a fine TDC). Though the concept of TS architecture is simple, it actually has many possible difficulties in practice [15]. First, the multiplexer between two stages introduces unwanted delay in the signal propagation path. To compensate this delay, a replica delay has to be inserted in the stop signal path and has to be carefully tuned to match with the delay of the multiplexers. These additional delay elements lead to difficulty in delay tuning and also cause jitter accumulation. Second, transferring the time residue to the fine TDC itself is challenging because the layout of the propagation paths between two TDCs has to be symmetric for any input time interval to avoid nonlinearity caused by difference in propagation delays. Thus, the conventional TS TDC has an inevitable nonlinearity caused by this inter-stage signal propagation, which is not perfectly symmetric in reality. Moreover, the TS architecture requires the ratio between the time resolutions of the two TDCs to combine the quantization results. Although this ratio can be determined to some extent at the design stage, it is not actually the same as that in the fabricated design due to process, voltage, and temperature variations. Therefore, some techniques to calibrate this mismatch are needed.

In this paper, in order to achieve a fine resolution and wide range at the same time, we employ a sub-gate-delay resolution PS architecture as the fine TDC of the TS architecture and propose several techniques to overcome the issues in the conventional PS and TS TDCs discussed so far. The proposed PS TDC incorporates a novel pulse injection with a built-in offset pulse and always keeps the propagating pulse wider than the offset one. Then, the PS TDC finishes the conversion process when it detects the original offset pulsewidth that is set wider than the threshold T_{th} to avoid the nonuniform PS rate issue, as shown in Fig. 3 [11]. Based on this scheme, the PS TDC realizes a fine time resolution, avoids unneeded jitter accumulation, and saves conversion time and power consumption, while it inherits the advantages of the conventional PS TDC architecture. The proposed TS TDC avoids the use of the inter-stage multiplexer and overcomes the resolution mismatch issue with a built-in coarse gain calibration mechanism so that the proposed TS TDC realizes a wide dynamic range and a fine time resolution at the same time.

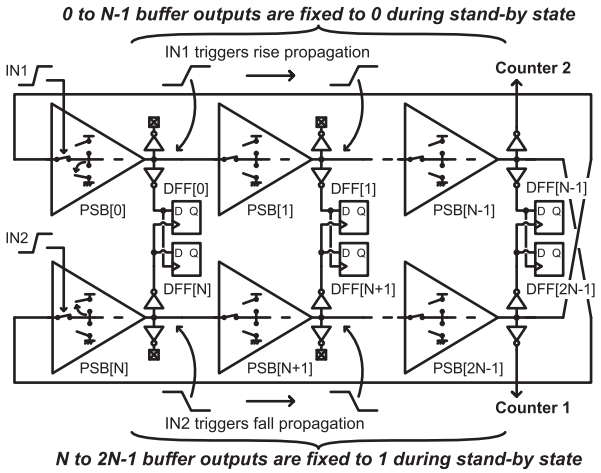

Fig. 5. Block diagram of the proposed fine TDC based on the PSBR.

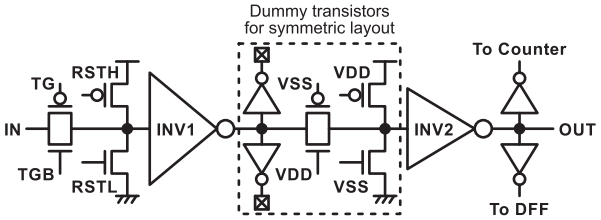

Fig. 6. Detailed schematic of the PSB.

The rest of this paper is organized as follows. In Section II, the architecture and conversion principle of the proposed TDC are described. Section III presents the circuit implementation and post-layout simulation results of the proposed TDC. Then, Section IV concludes this paper.

II. Proposed Two-Step TDC Architecture

A. Pulse-Shrinking Fine-Stage TDC

The block diagram of the fine-stage TDC based on PS buffer ring (PSBR) is illustrated in Fig. 5. It is mainly composed of $2N$-stage PS buffers (PSBs). The output of kth PSB ($k = 0, \ldots, N-1$) is connected to both a data input of kth DFF and a clock input of $(N+k)$th DFF, while the output of $(N+k)$th PSB on the opposite side of the ring is connected to both a data of $(N+k)$th and a clock of kth DFFs. Besides, the outputs of $(N-1)$th and $(2N-1)$th PSBs are connected to counters outside the PSBR core. The PSB has three functions: suspending the transition of the input signal, forcing the output at low or high level, and shrinking an input pulsewidth; in other words, the falling edge propagates the PSB faster by T_{LSB} than the rising edge. To realize these functions, the PSB circuit in Fig. 6 is used. The leftmost transmission gate is used to suspend a signal propagation when it is OFF, and the neighboring reset transistors force the output of PSB at low or high level. INV1 in the PSB is designed with a wider pMOS than that of INV2 so that the PSB falling transition delay t_f becomes smaller than the rising transition delay t_r, hence an input pulse shrinks its width through these inverters. The ratio of these two pMOS widths determines T_{LSB}. Some dummy transistors are also integrated to keep symmetry of the circuit.

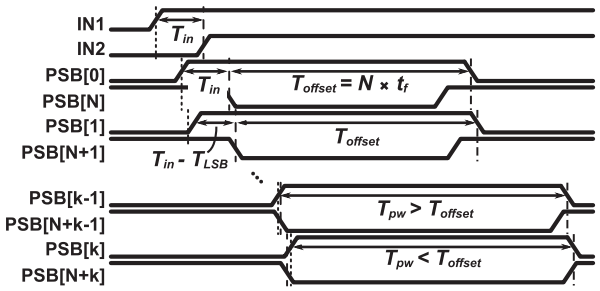

Fig. 7. Timing diagram of the PS TDC.

When the PSBR is in its standby state, zeroth and Nth PSBs suspend the signal propagation and force their outputs at low and high levels, respectively. Other PSBs enable the signal propagation so that the ring keeps the outputs of the zeroth to $(N-1)$th PSBs at low level and those of Nth to $(2N-1)$th PSBs at high level, as indicated in Fig. 5. The rise transition of IN1 input subsequently enables the signal propagation at zeroth PSB, and it triggers the rising edge propagation from $(2N-1)$th to zeroth PSB outputs. After T_{in}, the rise transition of IN2 triggers the falling edge propagation from $(N-1)$th to Nth PSB outputs. Note that the first falling transition arrives at zeroth PSB after propagating N PSBs. Therefore, the time difference between the falling edges at Nth and zeroth PSBs is equal to the total falling propagation delay of N PSBs, which works as a built-in offset pulsewidth and is defined as $T_{\mathrm{offset}} = N \times t_f$. Through this time difference injection scheme, the input T_{in} is fed into the ring in addition to the built-in T_{offset}, as shown in Fig. 7, where the width of the pulse signal in the ring just after IN2 injection is a sum of T_{in} and T_{offset} [16]. Thus, this scheme allows a tiny input time interval injection because it does not directly translate it into a narrow pulse.

Then, the pulse injected to the ring shrinks its width by T_{LSB} when it propagates through a single PSB. Suppose that the pulsewidth becomes almost equal to T_{offset} but still slightly wider than that after the pulse signal propagates $(k-1)$th PSB, as shown in Fig. 7, then the pulse arrives at the next PSB shortly thereafter to shrink its width below T_{offset}. Since the output of the PSB at the opposite side of the ring is supposed to have a signal transition of an opposite polarity when the propagating pulsewidth T_{pw} becomes equal to the original built-in offset pulsewidth T_{offset}, the kth PSB output rises later than the falling edge of the $(N+k)$th PSB output, thus the kth DFF alters its output from 0 to 1, as illustrated in Fig. 8. By identifying this DFF output transition, this TDC detects the original built-in T_{offset} and triggers the completion signal. Therefore, even if T_{offset} fluctuates due to process variation, the absolute value of T_{offset} has no impact on the conversion process. Since T_{offset} is chosen by design to satisfy $T_{\mathrm{offset}} > T_{\mathrm{th}}$ in Fig. 3, the proposed TDC does not suffer from the nonuniform shrinking rate issue.

The number of pulse rotation in the ring R is counted by the counter connected to $(2N-1)$th PSB, whereas the other counter connected to $(N-1)$th PSB is used to fix a false count caused by the delay of the completion detection circuit.

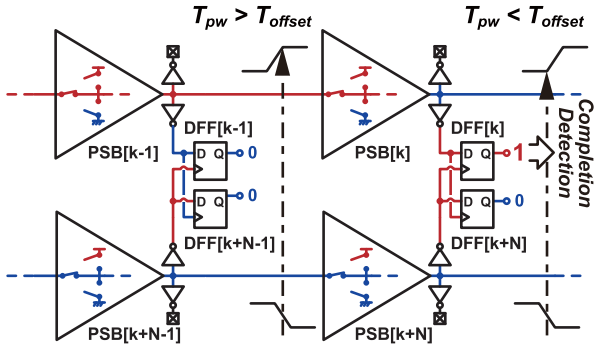

Fig. 8. Detailed PSBR schematic at the moment of the completion of conversion.

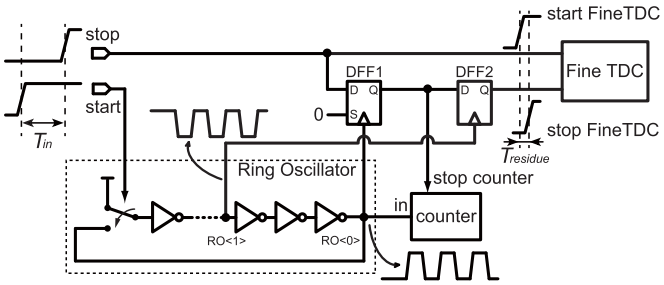

Fig. 9. Block diagram of the proposed TS TDC.

Finally, the input time difference T_{in} is converted to a digital code $R \times 2N + k$ with the resolution of T_{LSB}.

B. Architecture of the Two-Step TDC

The block diagram of the proposed TS TDC architecture is illustrated in Fig. 9. A ring oscillator with a counter works as the coarse TDC, and the PS TDC in Section II-A works as the fine stage. In the proposed TDC, the two TDCs are coupled through two DFFs unlike the conventional TS TDCs to avoid the nonidealities of the inter-stage multiplexers. Though the second DFF, DFF2 in Fig. 9, connected to the fine TDC seems to be redundant, it alleviates a metastability issue in DFF1 due to asynchronous timing between RO⟨0⟩ and the input stop signal. Moreover, the two DFFs have another role for the proposed built-in calibration mechanism, which is mentioned in Section II-C.

Fig. 10 shows the timing diagram of the proposed TDC. At the beginning of the conversion, a start input signal enables the ring oscillator by switching the input of the first-stage inverter from VDD to the feedback path, as illustrated in Fig. 9. After the input time interval T_{in}, the stop signal serves as an internal start signal for the fine TDC and enables it. Note that the coarse TDC is not stopped directly by the stop signal. The coarse TDC stops the measurement when the RO⟨0⟩ rises for the first time after the arrival of the rise transition of the stop signal. This timing is detected by DFF1, and then, the internal stop signal for the coarse TDC (stop counter signal) goes high. As a result, the coarse TDC rounds up the input T_{in} and quantizes the time interval T_{coarse}, as shown in Fig. 10. On the other hand, the fine TDC stops the measurement when the RO⟨1⟩ rises for the first time after the internal stop signal for the coarse TDC goes high. The time interval between rising edges of RO⟨0⟩ and RO⟨1⟩

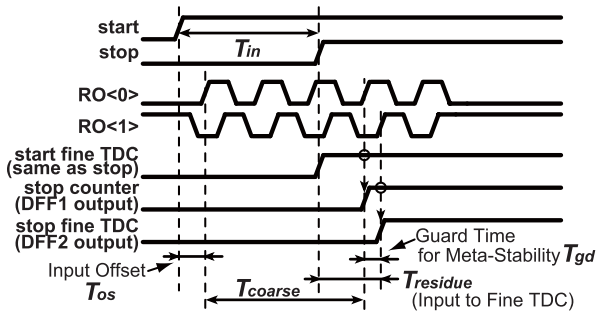

Fig. 10. Timing diagram of the proposed TS TDC.

works as guard time to suppress the metastability. Through the above-mentioned procedure, the time residue caused by this roundup, T_{residue}, in Fig. 10, is injected into the second-stage TDC for a fine conversion. Eventually, the overall input time interval is resolved according to

$$T_{\text{in}} = T_{\text{os}} + T_{\text{coarse}} + T_{\text{gd}} - T_{\text{residue}} \tag{1}$$

where T_{os} and T_{gd} are, respectively, the input offset time and the guard time for the metastability prevention. Though the sum of these fixed times $T_{\text{os}} + T_{\text{gd}}$ is tuned by design to be equal to one period of the coarse ring oscillator so that it can be calibrated out by simple calculation, in practice, these fixed times will be calibrated by using the conversion result with $T_{\text{in}} = 0$. Although (1) is correct in the time domain, the overall result is calculated with the binary output of each conversion. Thus, the ratio between the time resolutions of the two TDCs is essential.

C. Built-In Coarse Gain Calibration

The proposed calibration scheme is based on the built-in measurement mechanism. The required ratio of the resolutions can be obtained by measuring a time interval that corresponds to the 1 LSB of the coarse TDC with the fine TDC. In the calibration process, two different paths are switched by utilizing S (Set) input of DFF1 that is used to fix its output Q to high, as illustrated in Figs. 11 and 12. First of all, during the calibration mode, the input of the first-stage inverter is fixed to GND before the process starts. When DFF1 is in normal operation with 0 input to the S-port, as illustrated in Fig. 11(a), given $T_{\text{in}} = 0$, the fine TDC is stopped after one period of coarse oscillation T_{period} plus the input offset time T'_{os}, as summarized by the timing diagram in Fig. 11(b). On the other hand, when DFF1 output is fixed high with 1 input to the S-port, the timing signal injected into the oscillator passes through it without turning around the ring, as illustrated in Fig. 12(a), thus only the time that corresponds to the offset T'_{os} is fed into the fine TDC for conversion, as summarized by the timing diagram in Fig. 12(b). The time resolution of the coarse TDC is equal to the oscillation period of the ring oscillator T_{period} in Fig. 11(b), which can be calculated as the propagation delay of two laps through the inverter ring. Thus, the required coefficient, which is equal to the ratio of the time resolutions of the coarse and fine stages, is calculated just by subtracting the conversion result of Fig. 12 from that of Fig. 11, which cancels out the contribution of T'_{os}.

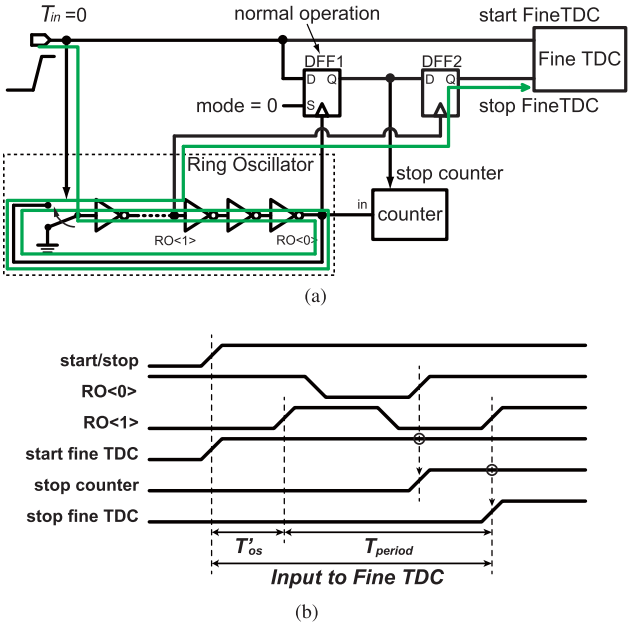

Fig. 11. (a) Signal propagation path for the coarse gain calibration mode 0 and (b) its timing diagram.

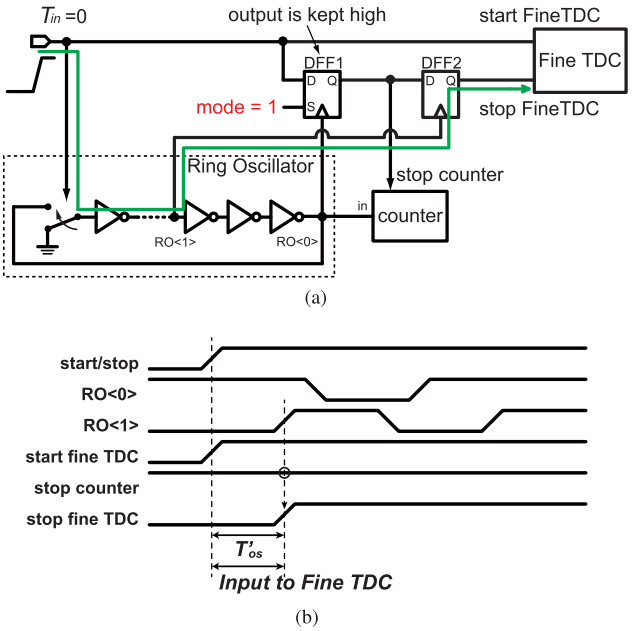

Fig. 12. (a) Signal propagation path for the coarse gain calibration mode 1 and (b) its timing diagram.

This subtraction also cancels the contributions of the signal path delay from the input port of T_{in} to the coarse ring oscillator and that from the ring to the fine TDC through DFF2, which are not explicitly shown in these timing diagrams for simplicity.

As a result, assuming that the fixed time $T_{\text{os}} + T_{\text{gd}}$ is calibrated out with the result of $T_{\text{in}} = 0$, the overall conversion result is given by

$$B_{\text{out}} = B_{\text{coarse}} \times N_{\text{cnt}} - B_{\text{fine}} \tag{2}$$

where B_{coarse} is the result of the calibration that corresponds to the binary output of the coarse time resolution quantized with the fine resolution, N_{cnt} is the value of the loop counter

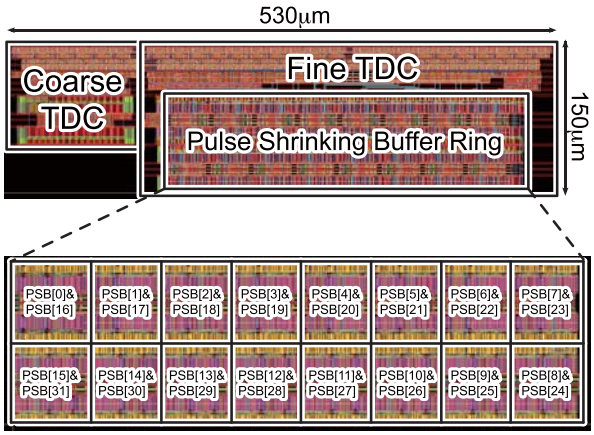

Fig. 13. Layout of the proposed TS TDC and PSBR.

in the coarse stage, and B_{fine} is the quantization result of the fine TDC. As the coarse stage utilizes a period of the ring oscillator as its time resolution, it typically has good linearity because the transition edge propagates exactly the same path at every one more coarse code output. Thus, the nonuniformity of the circuit, e.g., layout parasitics and process variation, does not impact its linearity. Therefore, we will utilize the result of the above-mentioned calibration procedure with the first oscillation cycle throughout the TDC input range.

Jitter during these procedures may impact the calibration results. In the calibration mode 0 in Fig. 11, the fine TDC has to convert $T_{\text{period}} + T_{\text{gd}}$, which is the maximum time interval input for the fine stage when it is used within the TS TDC. Thus, this procedure leads to the maximum jitter accumulation by the signal propagation through the PSBs in the fine stage, whereas in the coarse stage, the signal propagates just three laps through the inverter ring. As will be detailed in Section III, the inverters and buffers in both coarse and fine stages are carefully designed so that even with the maximum time interval input, the accumulated jitter is $\sim$0.5 LSB. Thus, also in the calibration procedure, the jitter does not have significant impact with the proposed design. If the jitter is of concern, we can perform an averaging over the multiple results of repeated calibrations to improve the accuracy.

III. Prototype Implementation and Simulation

The proposed TS TDC is implemented in a 0.18-μm standard CMOS technology, as shown in Fig. 13, and its performance is verified with post-layout simulation.

A. Fine-Stage TDC

The lower part of Fig. 13 shows PSB placement of the PSBR core in the fine TDC, which has 32 PSB stages. kth and $(k + 16)$th PSBs ($k = 0, \ldots, 15$) are laid next to each other to relax DFF connections shown in Fig. 5, and PSBs are arranged so that the wire lengths of inter-PSB connections are equal. The transistor size and the current consumption of the inverters in PSB have to be carefully chosen because the impact of jitter accumulation and process variation needs to be considered. We determined the transistor sizes of the PSB based on the jitter analysis in [17, eq. (29)]. Supposing that the uncertainty in propagation delay is dominant rather than

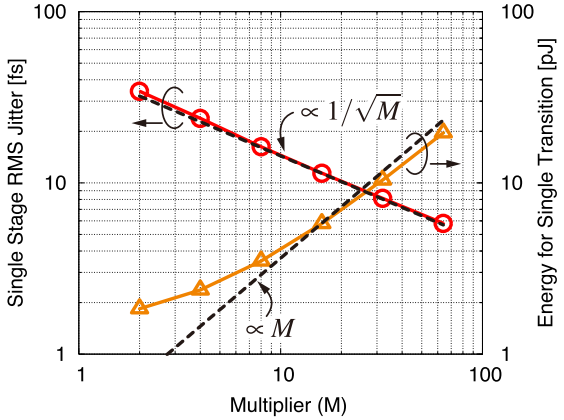

Fig. 14. Schematic-level simulation results of jitter and energy of a single-stage PSB for a single rise transition depending on the transistor width. For INV1 in PSB, $W_{\mathrm{pMOS}} = 8.32 \times M$ μm and $W_{\mathrm{nMOS}} = 4.00 \times M$ μm. For INV2, $W_{\mathrm{pMOS}} = 8.00 \times M$ μm and $W_{\mathrm{nMOS}} = 4.00 \times M$ μm. The rms jitter is calculated with 1024 times Monte Carlo simulations with thermal noise.

the initial noise on the output capacitor [17], the jitter due to the white noise caused by channel resistance is given by

$$\sigma_{t_{\mathrm{dP}}} \approx \sqrt{\frac{4kT\gamma_P t_{\mathrm{dP}}}{I_P(V_{\mathrm{DD}} - V_{\mathrm{tP}})}} \tag{3}$$

where t_{dP} is a delay of rise transition and $\sigma_{t_{\mathrm{dP}}}$ is its standard deviation. Here, we assume the rise transition and, thus, the parameters I_P, V_{tP}, and γ_P are saturation current, threshold voltage, and noise coefficient of pMOS FET, respectively. k and T are Boltzmann's constant and absolute temperature, respectively. Note that if the same inverters are used in the PSBs to compose the ring, by increasing the FET width W, I_P increases in proportion, while t_{dP} is almost constant, because the load capacitance, which is the gate capacitance of the next stage PSB, increases accordingly. Thus, from (3), we expect that the jitter of the PSB decreases in proportion to $\sqrt{W}$, while its power consumption increases in proportion to W, which is proven by schematic-level simulation results shown in Fig. 14. This graph shows the trends of rms jitter and energy consumption for a rise output transition in the single-stage PSB by sweeping the transistor width. The black dashed lines, respectively, show $\propto 1/\sqrt{M}$ and $\propto M$ trends that are both normalized with the simulation results at $M = 16$, where M is a multiplier of the transistors. Since we have miscellaneous switches and buffers in the PSB, the power is not exactly in proportion to W, while the jitter clearly shows $1/\sqrt{W}$ trends. The fine-stage TDC covers up to 10-bit range, and thus, with the maximum time interval input, the transition edge propagates 1024 stages of PSB until the end of the conversion. Since the proposed fine-stage TDC utilizes two transition edges propagating on the opposite side of the ring as explained in Section II-A, supposing that both rise and fall transitions have equal jitter $\sigma_{t_{\mathrm{dP}}}$, the accumulated jitter with the maximum time interval input is given by

$$\sigma_{t_{\mathrm{dP}}} \times \sqrt{1024} \times \sqrt{2}. \tag{4}$$

Here, we decided to make this accumulated jitter lower than 1/2 LSB that corresponds to ~1.0 ps. Thus, $\sigma_{t_{\mathrm{dP}}} < 22.1$ fs. As a result, we chose $M = 4$ to use $W_{\mathrm{pMOS}} = 8.32 \times 4$ μm and

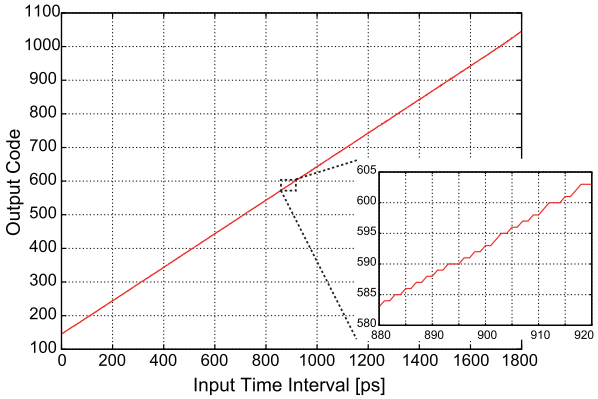

Fig. 15. Simulation result of the 2.0-ps resolution fine-stage PS TDC transfer characteristic in 10-bit range.

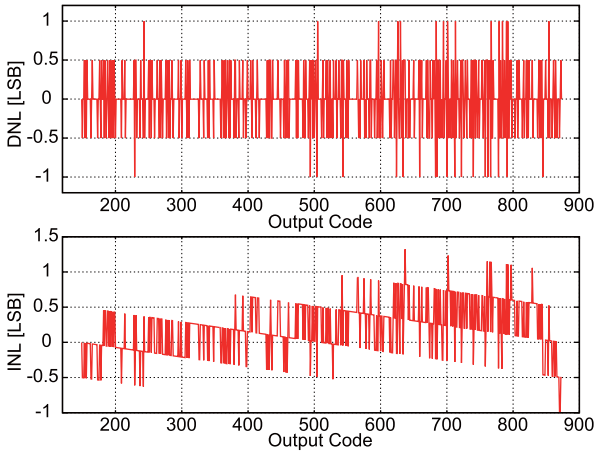

Fig. 16. Simulation results of DNL and INL of the fine-stage PS TDC.

$W_{\mathrm{nMOS}} = 4.00 \times 4$ μm for INV1 and $W_{\mathrm{pMOS}} = 8.00 \times 4$ μm and $W_{\mathrm{nMOS}} = 4.00 \times 4$ μm for INV2. The transmission gates are designed with $W_{\mathrm{pMOS}} = 12.0$ μm and $W_{\mathrm{nMOS}} = 6.0$ μm. Fig. 15 shows the simulated transfer characteristic of the PS TDC for the fine stage. The PS TDC realizes $T_{\mathrm{LSB}} = 2.0$ ps with 10-bit range that corresponds to 0–2-ns input time interval range. Simulated differential non-linearity (DNL) and integral non-linearity (INL) are plotted in Fig. 16. The simulation range is 150–850 output code that corresponds to 300–1700-ps input time interval range, which is used in the TS conversion. The TDC achieves the DNL and INL of +1.0/−1.0 LSB and +1.3/−1.0 LSB in post-layout simulation.

B. Two-Step TDC

The transistor sizes of the ring oscillator in the coarse TDC, which has 15 stages of inverters, are also determined based on the jitter analysis in [17]. As shown in Fig. 17, for the coarse stage ring oscillator, we have verified the trends of jitter and energy for a single rise transition with schematic-level simulation by sweeping the transistor width. The black dashed lines are normalized with the simulation results at $M = 16$. As expected, the jitter and energy are clearly in proportion to $1/\sqrt{M}$ and M, respectively, because the coarse stage ring oscillator uses simple inverters. Since, in our TS TDC, the coarse stage covers up to 7-bit range, with the maximum

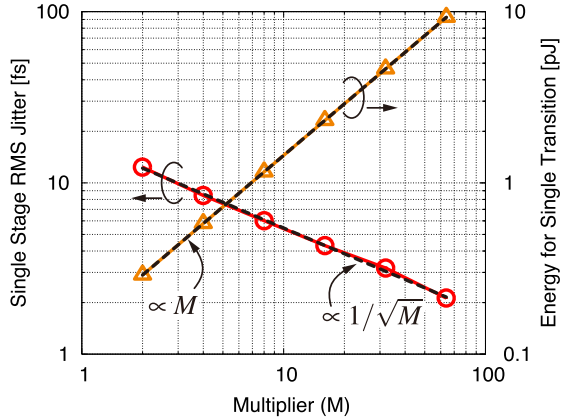

Fig. 17. Schematic-level simulation results of jitter and energy of a single-stage inverter in the coarse stage ring oscillator for a single rise transition depending on the transistor width. $W_{\mathrm{pMOS}} = 8.0 \times M$ μm and $W_{\mathrm{nMOS}} = 4.0 \times M$ μm are used. The rms jitter is calculated with 1024 times Monte Carlo simulations with thermal noise.

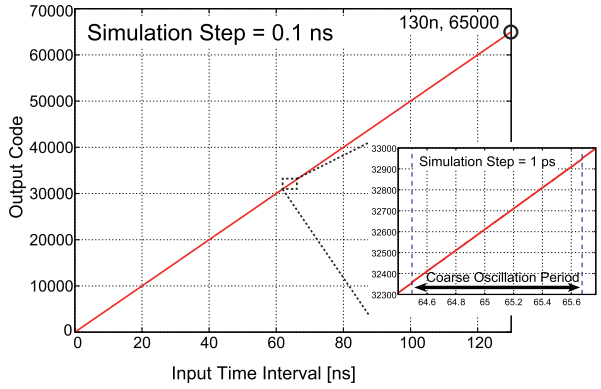

Fig. 18. Simulation result of 2.0-ps resolution TS TDC transfer characteristic in 16-bit range.

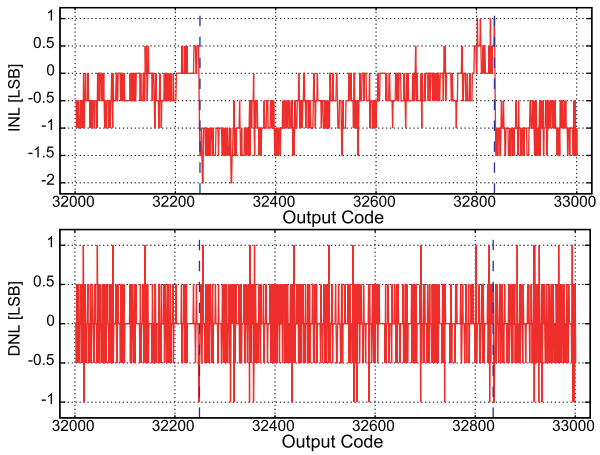

Fig. 19. Simulation results of DNL and INL of the TS TDC.

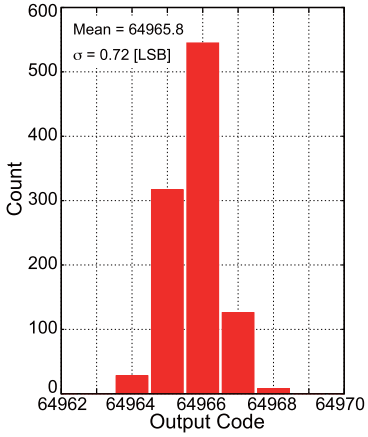

Fig. 20. Post-layout simulation result of single-shot code distribution of the TS TDC.

time interval input, the accumulated jitter is given by

$$\sigma_{t_{\mathrm{dP}}} \times \sqrt{15 \times 2} \times \sqrt{128}. \tag{5}$$

Considering the power budget, here, we assign 1/8 LSB that corresponds to ~0.25-ps jitter contribution for the coarse stage that results in $M = 16$, thus $W_{\mathrm{pMOS}} = 8.0 \times 16$ μm and $W_{\mathrm{nMOS}} = 4.0 \times 16$ μm. Since the fine-stage PSB is designed to have ~0.5 LSB jitter with its maximum time interval input, in total of the TS operation, the maximum accumulated jitter is expected to be $(0.5^2 + 0.125^2)^{1/2} \approx 0.52$ LSB.

Fig. 18 shows the simulated transfer characteristic of the proposed TS TDC. Although the input time interval range can be expanded infinitely long by extra counter bits, in reality, the jitter accumulation through the signal propagation causes a conversion error at longer time interval input. The maximum time interval input for this prototype is ~130 ns based on the above-mentioned calculation, where the accumulated jitter in the proposed TS TDC is roughly 0.5 LSB. As a result, the prototype TDC realizes 16-bit range that corresponds to 0–130 ns with $T_{\mathrm{LSB}} = 2.0$ ps. It consumes 18.0 mW from a 1.8-V power supply on an average throughout the input range while operating at 3.3 MS/s. The maximum power consumption is 26.8 mW at the input time interval of $T_{\mathrm{in}} = 129.5$ ns, where both the coarse and fine TDCs need longest time to finish the conversion. In this case, 47.8% of the total power is consumed in the fine stage, while the rest is in the coarse stage.

Simulated DNL and INL are plotted in Fig. 19. The range of the simulation is at the middle of the input time interval range, where the INL becomes its maximum because the transfer characteristic of the TDC has slightly arcuate shape caused by the calibration error. The detailed transfer characteristic of this range is also shown in Fig. 18. The TDC achieves the maximum DNL and INL of $-1.0/+1.0$ and $-2.0/+1.0$ LSB, respectively.

In 1024 times of simulations with thermal noise, as shown in Fig. 20, the maximum standard deviation of the TDC output code distribution is 0.72 LSB for this input range that corresponds to 1.44-ps single-shot precision, which agrees well with the predicted value with the schematic-level simulation though with the layout parasitics, the number becomes slightly larger.

The Monte Carlo simulation with process variation is carried out to evaluate its impact on the TDC performance. Fig. 21 summarizes DNLs and INLs for three different process variations simulated within the same range, as shown in Fig. 19. Due to the process variation, the coarse and fine resolutions fluctuate within the range of 1.90–2.04 and 1182.47–1183.16 ps, respectively. Through the proposed coarse gain calibration procedure using the built-in measurement mechanism, the proposed TS-TDC keeps its linearity even

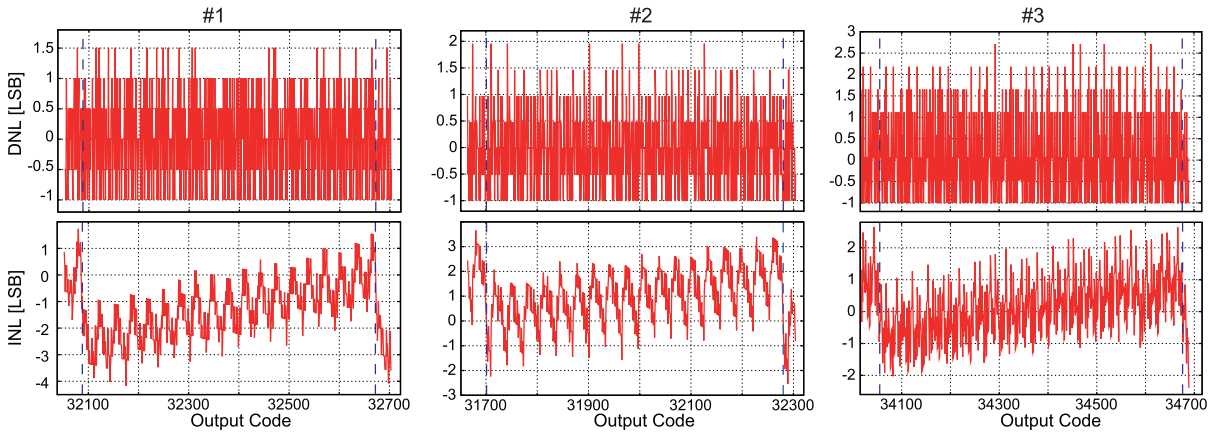

Fig. 21. Monte Carlo simulation results of DNLs and INLs with three different process variations.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON

Ref.	TCAS'14 [6]	JSSC'10 [7]	MEJ'15 [9]	JSSC'12 [18]	JSSC'13 [19]	JSSC'14 [20]	ASSCC'16 [11]	This work
Architecture	3D Vernier	2D Vernier	Vernier Sub-Ranging	Cyclic	Two-Step (Time Amp.)	Pipeline	Pulse Shrinking (PS)	Two-Step PS
Tech. [nm] (Meas. / Sim.)	130 Meas.	65 Meas.	130 Meas.	130 Meas.	65 Meas.	65 Meas.	180 Meas.	180 Sim.**
Resol. [ps]	7	4.8	5	1.25	3.75	1.12	1.8	2.00
Precision rms [ps] (T_{in} at the meas. or sim.)	20.8 (@1.4 ns)	–	2.05 (0∼300 ps)	∼1.25* (@40 ps)	–	0.77 (@∼348 ps*)	2.16 (@860 ps)	1.44 (@129.5 ns)
Rate [MS/s]	25	50	20	50	200	250	4.4	3.3
Range [bit]	11	7	6	8	7	9	9	16
DNL [LSB]	0.8	1	0.63	0.7	0.9	0.6	1.2	1.5
INL [LSB]	1.5	3.3	1.47	3.0	2.3	1.7	8.7	4.2
Power [mW]	0.33(@1MHz)	1.7	1.15	4.3	3.6	15.4	3.4	18.0
Area [mm^2]	0.28	0.02	0.7	0.07	0.02	0.14	0.07	0.08
FoM [pJ/conv.-step]	0.40	1.14	1.96	1.34	0.46	0.32	14.6	0.43

* calculated from the figure of the measurement result. ** Monte-Carlo simulation result that leads to the worst FoM.

with these fluctuations. With the built-in measurement, the coarse gain ratio B_{coarse} in (2) for these three cases are 587, 580, and 623, respectively. With these numbers, the proposed TS TDC achieves the maximum DNL of 2.7 LSB and INL of 4.2 LSB in the worst case among the three results.

The performance of the proposed TS TDC is compared with several recently reported sub-gate-delay resolution TDCs in Table I. To make a fair comparison, the figure of merit (FoM), which is widely used for TDC comparison, is adopted [6], [19], [20]. The FoM is defined as

$$\text{FoM} = \frac{\text{Power}}{(2^{N_{\text{linear}}} \times f_s)} \tag{6}$$

where the effective number of linear bits (N_{linear}) is given by

$$N_{\text{linear}} = \text{Range [bit]} - \log_2(\text{INL} + 1). \tag{7}$$

The Monte Carlo simulation results with the worst FoM case are listed for the proposed TDC. The proposed TDC realizes ultrawide range and fine time resolution at the same time while achieving competitive FoM using mature 0.18-μm CMOS technology.

IV. CONCLUSION

This paper presented a wide input range and fine-time resolution TDC that combines PS and TS architectures. In the fine-stage PS TDC, an undesirable nonuniformity of pulse shrinking rate in the conventional PS TDCs is avoided by a novel pulse injection with a built-in offset pulse and an offset pulsewidth detection schemes. This contributes to fine-resolution and low-jitter time-to-digital conversion, while it inherits the advantages of the PS TDC architecture, such as small-area implementation. The proposed TS architecture is applied to the PS TDC in order to expand the input range. The proposed TS TDC that incorporates a built-in coarse gain calibration mechanism overcomes the practical difficulty due to the nonideality of the inter-stage signal propagation path and the gain mismatch between the two stages. The detailed simulation results demonstrated that the proposed TDC realizes 16-bit wide dynamic range and 2.0-ps fine resolution at the same time. It achieves a competitive FoM using mature 0.18-μm technology in comparison with the recently reported sub-gate-delay resolution TDCs.

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