A 12-bit, 2.5-bit/Phase Column-Parallel Cyclic ADC

Amandeep Kaur, Deepak Mishra, and Mukul Sarkar

***Abstract*— A 12-bit, 1.67-MS/s, two-stage cyclic ADC, using a 1.5-bit algorithm in a 2.5-bit framework is proposed in this brief. The number of accurate comparators is reduced to half as compared with the conventional 2.5-bit stage, which reduces the power consumption. Furthermore, the pipelined operation of the two stages reduces the total number of clock-cycles, which improves the conversion rate. The proposed ADC is designed and fabricated in a standard 180-nm CMOS technology. The obtained differential nonlinearity and integral nonlinearity are +0.5/−0.5 LSB and +0.8/−0.9 LSB, respectively. The ADC consumes 435-μW of power and occupies an area of 0.045 mm^2. The postlayout simulations of ADC designed in a column-pitch of 5.6 μm show that it is suitable for column-parallel readout in CMOS image sensors.**

***Index Terms*— 2.5-bit cyclic ADC, CMOS image sensor (CIS).**

I. Introduction

High-resolution and high-speed CMOS image sensors (CIS) need high-bandwidth analog readout, which increases power consumption and makes the camera system difficult to handle. For high-speed readout and optimum power consumption, column-parallel ADCs are preferred in the state-of-the-art CIS. Medium-to-high-speed ADCs available in the literature include flash, successive approximation register (SAR), and pipeline. Flash ADCs require 2^{N-1} comparators for N-bit conversion, and therefore not preferred for high-resolution and low-power applications. SAR ADCs use N clock-cycles for N-bit conversion. However, the digital-to-analog converter (DAC) occupies a large area; therefore, these ADCs are limited to column-shared architectures of CIS [1], [2]. In addition, the multiplexing reduces the effective readout speed of the CIS. Similarly, fully pipelined ADCs with N-stages for N-bit resolution increase the chip area and power consumption. In cyclic ADCs, a single stage is recycled N times to achieve N-bit conversion. The moderate speed and small chip area make the cyclic ADC best suitable for high-resolution and high-speed CIS.

The conversion rate of the cyclic ADC is limited by the speed of a multiplying digital-to-analog converter (MDAC). An MDAC with an improved clocking scheme is proposed in [3], where the conversion rate of the ADC is improved at the cost of large power consumption. Two-stage ADCs are the alternate choice to achieve high speed. In two-stage architectures, the power and settling constraints of the second stage are relaxed, which results in low power consumption [4]. The ADCs reported in [3] and [4] internally use 1.5-bit/cycle algorithm. In a 1.5-bit stage, effectively, 1 bit is obtained per cycle. Therefore, the single stage is recycled N times for N-bit resolution. A multibit/cycle is used to reduce the ADC power as the number of cycles for N-bit conversion is reduced by the factor of the number of bits processed in the first cycle. Furthermore, the multibit stage has the higher gain, which reduces the noise, matching, and settling requirements for the later stages [5]. The conventional 2.5-bit stage consists of six comparators and an MDAC [6].

Manuscript received May 24, 2018; revised August 20, 2018; accepted September 15, 2018. *(Corresponding author: Amandeep Kaur.)*

The authors are with the Electrical Engineering Department, IIT Delhi, New Delhi 110016, India (e-mail: eez138241@ee.iitd.ac.in; eez138244@ee.iitd.ac.in; msarkar@ee.iitd.ac.in).

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Digital Object Identifier 10.1109/TVLSI.2018.2871341

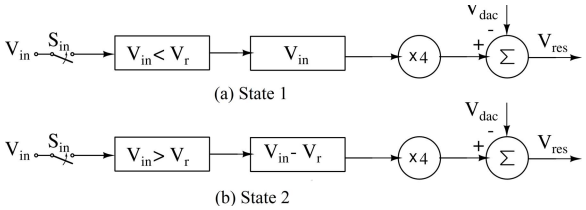

Fig. 1. Equivalent circuits representing two states when (a) $V_{\text{in}} < V_r$ (State 1) and (b) $V_{\text{in}} > V_r$ (State 2).

Decreasing the number of comparators reduces the parallel switching and also improves the input signal bandwidth.

In this brief, a 12-bit, 2.5-bit/phase two-stage cyclic ADC, containing half the number of comparators as compared with the conventional 2.5-bit stage is proposed. The reduction in the number of comparators should ideally result in 50% power saving in terms of comparator power. However, a subtractor used for input subrange mapping requires additional power; therefore, effective power saving is 25%. This power saving is achieved by using only one MDAC at a time, which results in a sampling rate of 1 MS/s [7]. In general, the 2.5-bit stage has lower speed than the 1.5-bit stage due to a lower feedback factor and the higher settling time. This reduction in speed is compensated by the increased number of bits per cycle. In the proposed ADC, an additional improvement in speed is obtained by using two MDACs in a pipelined fashion. The ADC results in a sampling rate of 1.67 MS/s while consuming the same power as the conventional 2.5-bit stage. The multibit stage along with the pipelined operation shows more than three-time and five-time improvement in the conversion rate than the cyclic ADCs in [4] and [8], respectively.

The ADC is designed and fabricated in the UMC 180-nm CMOS technology. It operates at a sampling rate of 1.67 MS/s and consumes 435 μW of effective power. The area occupied by the ADC is 0.045 mm^2, which includes the reference circuits, clock generators, and buffers. Since the proposed ADC is targeted for CIS applications, the postlayout simulations of the column ADC occupying an area of 5.6 μm $\times$ 1350 μm are also presented. The rest of this paper is organized as follows. Section II describes the proposed ADC. Section III presents the measurement results. Section IV concludes this paper.

II. Proposed Two-Stage Cyclic ADC

The fundamental idea and the block diagram of the proposed ADC are shown in Figs. 1 and 2(a), respectively. In the first step, the sampled signal (sample and hold circuit are not shown for simplicity) V_{in} is compared with the reference signal V_r (mid-voltage of the input range), using the MSB comparator to determine the subrange. For the inputs lying in the lower subrange ($V_{\text{in}} < V_r$), comparator returns logic low and high otherwise. The bit D_2 of the ADC is determined by the MSB comparator. The higher subrange inputs are mapped to the lower subrange using a subtractor. The signal or the subtracted value is thus resolved using the standard 1.5-bit algorithm. The signal flow for the two states $V_{\text{in}} < V_r$ and $V_{\text{in}} > V_r$ are also shown in Fig. 1(a) and (b), respectively. Fig. 2(b) shows the subranges for the proposed 2.5-bit stage. The timing diagram of the ADC is shown in Fig 1(c).

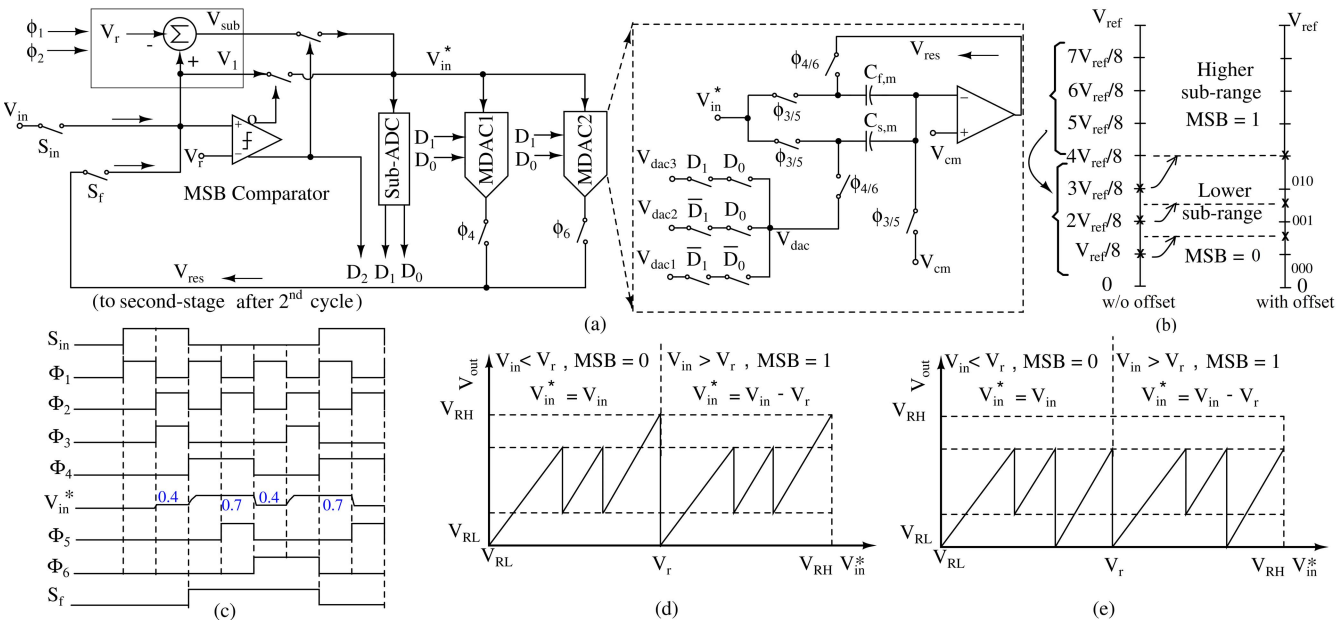

Fig. 2. (a) Single-stage block diagram. (b) Subrange algorithm. (c) Timing diagram with V_{in}^{*} as the residue voltage of MDAC, for an ADC input of 0.4 V, assuming V_{RL} and V_{RH} of 0.3 and 1.5 V, respectively. (d) Residue plot of the MDAC. (e) Proposed residue plot with a tolerable positive offset.

The proposed ADC uses a capacitor flip-over MDAC, shown in Fig. 2(a) to generate the residue voltage V_{res}, given by

$$V_{\text{res}} = \left(1 + \frac{C_{s,m}}{C_{f,m}}\right) V_{\text{in}}^{*} - \frac{C_{s,m}}{C_{f,m}} V_{\text{dac}}. \tag{1}$$

The ratio of the capacitors $C_{s,m}$ and $C_{f,m}$ is chosen to be three to obtain an interstage gain of four. This improves the linearity of the ADC with respect to the 1.5-bit stage as

$$\text{DNL} = k.\frac{2^{N-N_1/2}}{C_{\text{total}}} \tag{2}$$

where k is a proportionality constant, N_1 is the number of bits resolved in the first cycle, C_{total} corresponds to the total stage capacitance, and N is the ADC resolution [5]. Thus, the matching requirement of a 2.5-bit stage is 3 dB lower than the 1.5-bit stage. The residue plot of MDAC is shown in Fig. 2(d). The proposed ADC uses two MDACs to alternately sample and hold the residue. When MDAC1 is holding the residue voltage, MDAC2 starts sampling the new residue, which effectively improves the conversion rate by 40%. Furthermore, the residue generated at the end of the second clock phase is simultaneously sampled on the second stage. When the second stage is resolving the residue of the first stage, the first stage starts sampling new data. Therefore, the conversion rate of the ADC is increased both due to the multibit architecture and the pipelined operation.

The ADC uses a double-tail comparator, where the preamplifier is biased with a constant current source for high gain and low offset [9]. The tail of regenerative latch is dynamically controlled for high speed. The conventional 2.5-bit stage has inherent redundancy; therefore, the offset requirements of the comparators are relaxed. However, the design requirements of the comparators become critical when placed in the column pitch of high-resolution CIS. Due to narrow pixel-pitch, it is difficult to isolate the sensitive analog signals from the digital feedback signals of the DAC [8]. The single-stage comparator without the preamplifier results in large kick-back noise and the capacitive coupling from the digital signals will significantly degrade the ADC resolution. Therefore, the comparators are usually designed with preamplifier as the first stage followed by the regenerative latch [4], [8]. The energy consumed by the comparator is 220 fJ/decision for an input resolution of 1 mV (power $= 55\mu$W at $f_{\text{Clk}} = 250$ MHz) which drops to 112 fJ/decision for a full swing input.

Furthermore, the offset introduced by the MSB comparator is not corrected using conventional digital error correction (DEC). To take the advantage of digital redundancy, the reference voltages of the DAC are modified as

$$\begin{aligned} V_{\text{dac}} &= V_{\text{dac1}} = V_{\text{RL}} \quad \text{when } D_1 D_0 = 00 \\ &= V_{\text{dac2}} = (V_{\text{RH}} + 5\ V_{\text{RL}})/6 \quad \text{when } D_1 D_0 = 01 \\ &= V_{\text{dac3}} = (7\ V_{\text{RL}} + 5\ V_{\text{RH}})/12 \quad \text{when } D_1 D_0 = 11 \end{aligned}$$

where $V_{\text{RH}} - V_{\text{RL}}$ represents the input range of the ADC. Based on these reference voltages, the residue plot of the MDAC is modified and is shown in Fig. 2(e). The modified residue plot shows that the positive offset of all the three comparators can be tolerated. Since the residue generated at the MDAC output is not mapped to the complete input range [Fig. 2(e)], therefore to correct the bits, a modified digital error correction (MDEC) is proposed. According to MDEC, if digital code "010" or "110" is obtained in the current clock phase, and then, "010" is added to the code of the next phase. The MDEC is implemented with an additional XOR gate, two AND gates, and an inverter as compared with conventional DEC.

In the proposed ADC, the main source of nonlinearities is the capacitive mismatch, offset, and the gain error of the subtractor and MDAC. The ADC uses the similar subtractor circuit as used in [7]. The transfer of residue voltage from one stage to the another led to incomplete settling of the MDAC, which also adds to the nonlinearity. To improve the ADC resolution, a digital calibration is applied to the cyclic ADC. As shown in Fig. 1, the ADC operates in two states, where $V_{\text{in}}^{*} = V_{\text{in}} - SV_r$ with $S = 0$ for $V_{\text{in}} < V_r$ and $S = 1$ for the other case. Assume that the mismatch between the capacitors of the subtractor and MDAC is represented by ΔC_{sub} and ΔC_{mdac}, respectively. The error coefficients e_s and e_m defined as $(\Delta C_{\text{sub}}/C_{f,\text{sub}})$ and $(\Delta C_{\text{mdac}}/C_{f,m})$ result in

$$V_{\text{in,mis}}^{*} = V_{\text{in}} - SV_r(1 + e_s) \tag{3}$$

$$V_{\text{res,mis}} = V_{\text{in,mis}}^{*}(4 + e_m) - DV_{\text{RH}}(3 + e_m) \tag{4}$$

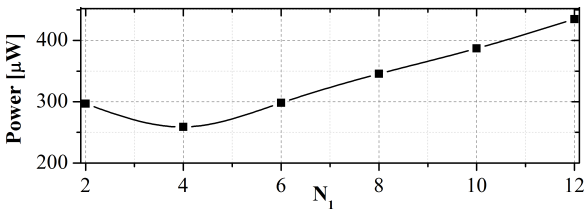

Fig. 3. ADC power as a function of first-stage bits.

where $DV_{\mathrm{RH}} = V_{\mathrm{dac}}$, and D takes a value among 0, 1/6, and 5/12. For simplicity, assume $V_{\mathrm{RL}} = 0$ and $V_{\mathrm{RH}} = 2V_r$, on dividing (4) by $2V_r$ and replacing (3) in (4), the quantized value $(V_{\mathrm{res,mis}}/2V_r)$ and $(V_{\mathrm{in}}/2V_r)$ represented by X_{out} and X_{in}, respectively, is rewritten as

$$X_{\mathrm{out}} = (4 + e_m)\left[X_{\mathrm{in}} - \frac{S}{2}(1 + e_s)\right] - D(3 + e_m). \tag{5}$$

The proposed ADC effectively results in 2-bit per clock phase, and the mismatch error coefficient E_{cm} calculated using (5) for the ith phase is

$$E_{\mathrm{cm}} = e_m\left[(X_{\mathrm{in}}(2i-1)) - D(2i-1) - \frac{S}{2}\right] - 2S(1 + e_s). \tag{6}$$

In two-stage cyclic ADC, the mismatch introduced by the two stages is different. To differentiate the two stages, variables $e_{s,A}$, $e_{m,A}$ and $e_{s,B}$, $e_{m,B}$ are used. In the proposed 2.5-bit algorithm, first stage operates for two clock-phases and second-stage operates for four clock-phases. Using the similar expression for $X_{\mathrm{in}}(j)$ as in [10], the total error due to capacitive mismatch $E_{\mathrm{cm},t}$ is given as

$$\begin{aligned} E_{\mathrm{cm},t} &= 2^{-3}[-D(1) + 2^{-1}D(2)] - 4S(1 + e_{s,A}) + e_{m,A}2^{-1} \\ &\quad \times \sum_{j=4}^{12}\left[D(j)2^{-j} - \frac{5S}{32}\right] + \frac{1}{4^3}\left[-\frac{D(5)}{2} + \frac{D(9)}{2^5} + \frac{D(11)}{2^6}\right] \\ &\quad + \frac{1}{4^3}\sum_{j=3}^{6} e_{m,B}\left[\frac{(j-2)D(2j)}{2^{2j-4}} - \frac{85S}{128}\right] - 8S(1 + e_{s,B}). \end{aligned} \tag{7}$$

Similarly, the coefficients for incomplete settling time $E_{\mathrm{st},t}$ and gain error $E_{\mathrm{ge},t}$ are calculated. The resultant error is therefore the summation of these errors as

$$\mathrm{Error}_{\mathrm{total}} = E_{\mathrm{cm},t} + E_{\mathrm{st},t} + E_{\mathrm{ge},t}. \tag{8}$$

The calibrated output is thus obtained by subtracting the total error $\mathrm{Error}_{\mathrm{total}}$ from the raw digitized output as

$$D_{\mathrm{cal}} = \sum_{j=1}^{12} D_{(j-1)}2^{-j} - \mathrm{Error}_{\mathrm{total}}. \tag{9}$$

In each clock phase, the bit (D_2) is obtained from the MSB comparator and the three-state redundant binary codes expressed with two decision levels (D_1, D_0) are obtained from the sub-ADC. The first and second stages generate 18-bit raw ADC output. These bits are then digitally corrected to obtain the effective 12-bits. The power of the two-stage ADC as a function of processed first stage bits (N_1) is shown in Fig. 3. The bit optimization in the two-stage ADC is determined by optimizing thermal noise and total power consumption. Thus, 4 bits obtained from the first stage and 8 bits from the second stage result in minimum power consumption. The power consumption as a function of bit resolution (N) for the single-stage and two-stage ADCs is shown in Fig. 4. The two-stage ADC consumes approximately 40% less power as compared with the single-stage ADC.

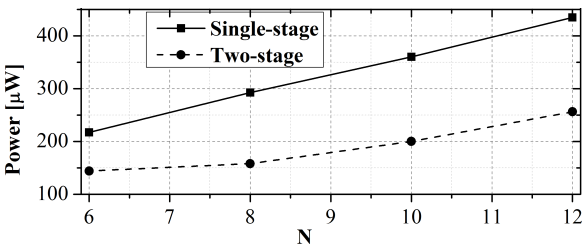

Fig. 4. Power consumed by single-stage and two-stage cyclic ADCs as a function of the total number of bits N.

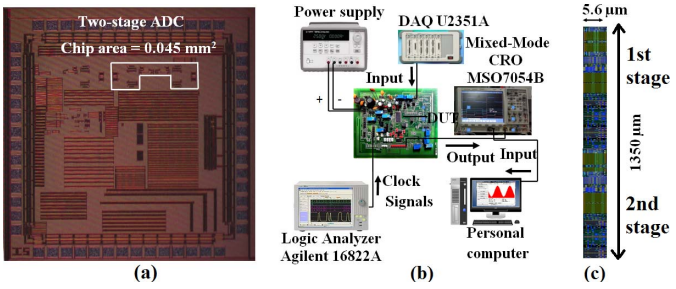

Fig. 5. (a) Chip micrograph of a two-stage cyclic ADC. (b) Experimental setup. (c) Layout of two-stage ADC designed with 5.6-μm pixel pitch.

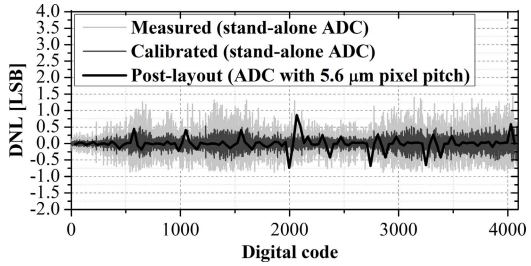

Fig. 6. Differential nonlinearity.

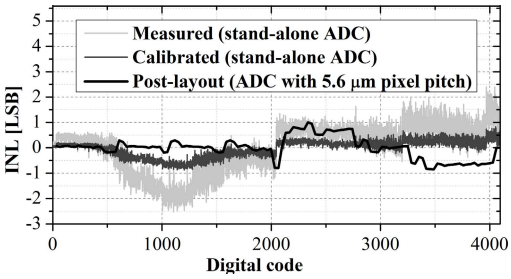

Fig. 7. Integral nonlinearity.

III. Measurement Results and Analysis

A 12-bit, 1.67-MS/s two-stage cyclic ADC has been designed and fabricated in the 180-nm CMOS technology. The microchip photograph is shown in Fig. 5(a). The ADC occupies an area of 0.045 mm^2. The analog input of the ADC is generated through Agilent U2351A and digitized data are captured by the oscilloscope Agilent MSO7054B, as shown in Fig. 5(b). The measurement results show a worst case differential nonlinearity (DNL) and integral nonlinearity (INL) of +1.4/−0.8 LSB and +2.4/−2.5 LSB, as shown in Figs. 6 and 7, respectively. The calibrated values of DNL and INL are +0.5/−0.5 LSB and +0.8/−0.9 LSB, respectively, also shown in the same figures. The dynamic performance of the proposed ADC is evaluated by applying an input sinusoidal signal of frequency 200 kHz. The obtained output frequency spectrum is shown in Fig. 8. The measured signal-to-noise ratio is 63.15 dB. The obtained signal-to-noise and distortion ratio is 60.11 dB. The total power consumed

TABLE I
PERFORMANCE COMPARISON

Parameters	[1]	[4]	[8]	[11]	[12]	[13]	[14]	**This work (stand-alone)**	**This work (in column)**
Technology [nm]	130	180	180	90	180	90/65	45/65	180	180
Samp. rate [MS/s]	30	0.5	0.3	1	3.4	0.54	1.08	1.67	1.67
Resolution [bits]	14	12	13	12	12	14	12	12	12
DNL [LSB]	-	+0.5/-0.7	< 0.5	+0.9/-0.7	0.7/-0.4	+0.95/-0.8	+0.82/-0.88	+0.5 /-0.5	+0.8/-0.7
INL [LSB]	-	-	< 3.2	+1.9/-1.2	+1.0/-0.6	+2.57/-28.27	+1.04/-11.75	+0.8/-0.9	+0.9/-0.8
Supply [V]	1.2	1.8	1.8/3.3	1.4	1.8	-	-	1.8/3.3	1.8/3.3
Power [mW]	2.54	0.101†	0.3†	0.49	3/2.9	0.12†	0.12†	0.435	0.256†
Chip area [mm^2]	0.24	0.00991	-	0.037	0.61	6.4 $\times$ 1892.6	4.4 $\times$ 920	0.045	5.6 $\times$ 1350
FOM [pJ/conv-step]	0.031	0.045 *	0.122*	0.37	0.66/1.15	0.014	0.027	0.31	0.037*

† Column-ADC power (excluding chip-level circuits), * FoM = $\frac{Power}{f_s \times 2^{ENoB}}$ or FoM = $\frac{Power}{f_s \times \frac{2^N}{Noise}}$ at DC [15].

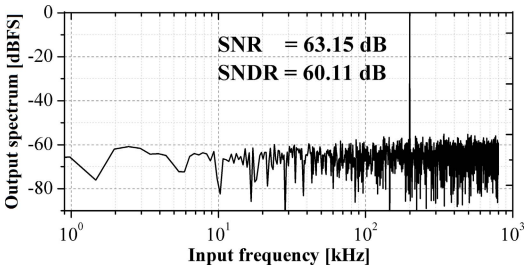

Fig. 8. FFT spectrum for an input sinusoid of 200 kHz.

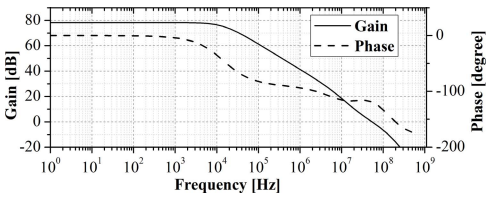

Fig. 9. AC response of an amplifier for a load capacitance of 300 fF.

by the ADC is 0.8 mW, including bias generators, clock generators, and buffers. However, the effective power of column ADC is 435 μW. The obtained figure of merit (FoM) (Walden) of the stand-alone ADC is 0.31 pJ/conversion-step.

In the stand-alone design, the associated circuitries like a bias generator, a clock generator, and buffers are placed on the same chip, resulting in an area of 0.045 mm^2. The area of ADC (excluding the bias generator, clock generator, and buffers) is 0.015 mm^2, which when converted into a 5.6-μm column pitch of CIS will occupy an area of 5.6 μm $\times$ 2670 μm. In the stand-alone ADC, the two stages are identical to save the design time. In actual practice, the second-stage design requirements are relaxed. In the column design, the second-stage MDAC and the subtractor are relaxed and a lower value of capacitances (100 fF, 300 fF) and (150 fF, 150 fF), respectively, are used. The total area occupied by the column ADC is 5.6 μm $\times$ 1350 μm, as shown in Fig. 5(c). The area reduction is due to the relaxed second-stage design and optimal routing. The worst case DNL and INL obtained after postlayout simulations is $+0.8/-0.7$ LSB and $+0.9/-0.8$ LSB, also shown in Figs. 6 and 7, respectively.

The proposed design uses a p-input folded cascode amplifier to meet the design requirements of 12-bit ADC. The dc gain of the amplifier is 79–84 dB, phase margin is 51–54°, and a unity gain bandwidth is 54–56 MHz throughout the process corners. The gain and phase plot of the amplifier is shown in Fig. 9. Furthermore,

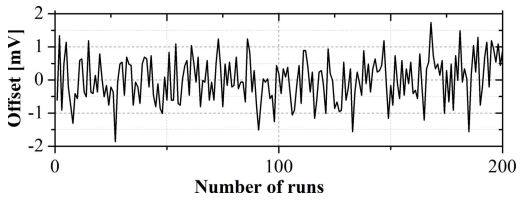

Fig. 10. Op-amp offset plotted for 200 Monte Carlo runs.

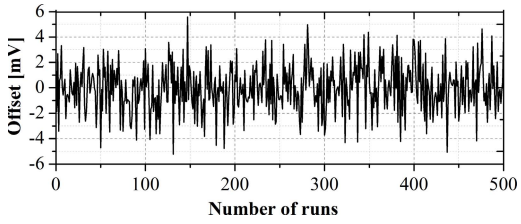

Fig. 11. Comparator offset plotted for 500 Monte Carlo runs.

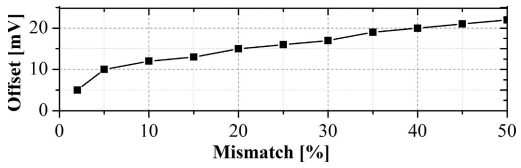

Fig. 12. Offset introduced due to the addition of mismatch.

the op-amp offset is plotted for 200 Monte Carlo runs in Fig. 10. The figure shows the worst case offset of $+1.8/-1.9$ mV.

The layout shown in Fig. 5(c) uses two stages where the design constraints on the second stage are relaxed. The residue at the output of the first stage is multiplied by the factor 2^{N_1-1}, increasing the noise and mismatch tolerance band of the second stage. This helps in reducing the sizes of the capacitors of the second stage. The measured offset of the comparator is 1.2 mV. To take the advantage of redundancy algorithm, the positive offset is added intentionally to the MSB comparator and a sub-ADC comparator of the column ADC. The required amount of mismatch depends on the offset introduced by the comparators. Monte Carlo simulations are performed to identify the amount of mismatch, as shown in Fig. 11. The simulated worst-case offset of the comparator is -5.2 mV. To compensate this offset, an intentional mismatch of 2.5% is desired as shown in Fig. 12. The reported postlayout results of the column ADC are calculated with an additional mismatch of 5% between the transistors.

The column ADC with the relaxed second stage consumes 256 μW of power, resulting in an FoM [15] of 0.037 pJ/conversion-step. Performance of the two-stage cyclic ADC is compared with the literature in Table I. The ADC in [1] has better FoM than the proposed ADC. However, [1] internally uses an SAR architecture, which is difficult to implement in a pixel pitch of 5.6 μm due to a large DAC area. Furthermore, [13] and [14] are implemented in the 65-nm technology. The performance of the proposed ADC is thus comparable with the state-of-the-art column ADCs and is therefore suitable for high-resolution and high-speed CIS.

IV. Conclusion

A 12-bit, 1.67-MS/s two-stage cyclic ADC is designed and fabricated in a standard UMC 180-nm CMOS technology. A two-stage architecture with the 1.5-bit algorithm implemented in a 2.5-bit framework increases the conversion rate by more than three times as compared with the existing two-stage cyclic ADCs. The power consumed by the ADC is 435 μW, resulting in the FoM of 0.31 pJ/conversion-step. In addition, the postlayout results of the ADC designed in 5.6-μm pitch are presented with an FoM of 0.037 pJ/conversion-step. The designed ADC will result in a frame-rate of greater than 1600 frames/s for a 1-Mpixel array.

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