Design and Characterization of SEU Hardened Circuits for SRAM-Based FPGA

Tianwen Li, Hongjin Liu, and Haigang Yang

***Abstract*— The mitigation of single-event upset (SEU) in SRAM-based field-programmable gate array (FPGA) is increasingly important as utilization and demand for SRAM-based FPGA dramatically increased in radiation environments such as space. As D flip-flop (DFF) and memory [including block random-access memory (BRAM) and configuration random-access memory (CRAM)] are constituted as the key elements in an FPGA, it is fundamentally necessary to develop radiation hardening techniques targeted for enhanced reliability of DFF and memory. A novel SEU hardened memory design for FPGA is proposed with capabilities of multibit upset protection. We further developed two prototype FPGA chips, one with SEU and the other without SEU hardening for comparison. The FPGA chips are fabricated in a standard 0.13-μm CMOS process and have a volume of three million equivalent logic gates. In terms of SEU cross section, CRAM in the hardened FPGA design is about four orders of magnitude lower than in the unhardened FPGA design, while BRAM demonstrates a reduction by three orders of magnitude. On the conditions of linear energy transfer being up to 14 MeV$\cdot$cm^2/mg, no SEU errors were observed from DFF in the hardened FPGA design.**

***Index Terms*— Error correction code (ECC), memory, multibit upset (MBU), radiation hardened by design, single-event upset (SEU), SRAM-based field-programmable gate array (FPGA), triple interlocked latch (TILL).**

I. Introduction

As A circuit function of SRAM-based field-programmable gate arrays (FPGAs) is mainly defined by the content of the configuration memory [e.g., configuration random-access memory (CRAM)], they are considered as more vulnerable to single-event upsets (SEUs) than application-specific integrated circuit (ASIC) devices, where all the logic functions and interconnections are determined. With continued scaling of the integrated circuit feature size, the node capacitance and the supply voltage decrease altogether. Hence, the amount of charges stored on a node capacitor to hold a certain logic state are getting less, more prone to influences from cosmic ray, or α-particles originated by the decay of uranium and thorium impurities presented within packages [1]–[3], [17], [18]. These energetic particles will ionize a mass of electron–hole pairs in the semiconductor substrate, which may be collected by source/drain diffusions and hence possibly alter the existing logic state dedicated to a storage cell. This phenomenon is so-called SEU. When SEUs occur in whichever of the CRAM, the block random-access memory (BRAM), or the D flip-flop (DFF) presented in an FPGA [19]–[21], the implemented functional design is impaired for its original behavior. SEU has long been known as a cumbersome problem for SRAMs because of their dense geometries organized in a highly compact fashion [4], [5]. Specifically, in those high reliability required applications such as space missions, military equipments, and avionics systems, an SEU impacted FPGA could result in a catastrophic operation failure.

The issue of making SRAM-based FPGAs resilient to SEUs has been tackled mainly in two ways. One avenue of endeavors is to build some sort of redundancy in circuit implementations. Triple modular redundancy (TMR) with majority voters is commonly used to mask errors, combined with dynamic reconfiguration [8]. Unfortunately, the TMR is usually realized at a high cost in terms of area, speed, and power consumption. The other avenue of endeavors is to have an FPGA intrinsically designed with the SEU hardened storage element and circuitry. Toward this end, some intensive studies have been devoted to SEU hardened design of the memory, and the DFF being fit into FPGA. The DFF hardening methods can also be classified into two categories [6]. The first is to design a hardened DFF based on a special state locking mechanism. The second is to design a hardened DFF by enlarging node capacitance and driving strength. One example of the first category is the dual interlocked cell element (DICE) cell [7], which tolerates SEU without increasing the transistor size and the node capacitance. Error correction code (ECC) is typically used for hardening the memory in FPGA to detect the soft errors and recover the corrupt state. In this paper, we combine the extended hamming coding technique with the physical bit location interleaved to enhance the memory reliability. Moreover, a so-called autochecking controller (ACC) is proposed to constantly scan and correct bit errors accumulated in CRAM and SRAM. For DFF, the triple interlocked latch (TILL) structure previously published in [9] is applied, proven to have a higher SEU threshold than the conventional DICE structure.

The rest of this paper is organized as follows. Section II analyzes the SEU sensitivity characteristics arising from the SRAM-based FPGA. Section III discusses a comprehensive

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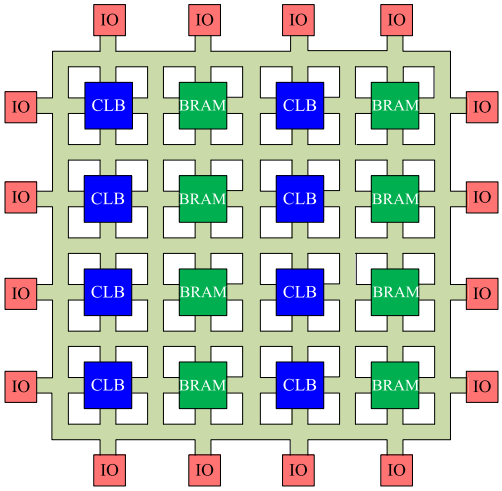

Fig. 1. Generic view of FPGA architecture.

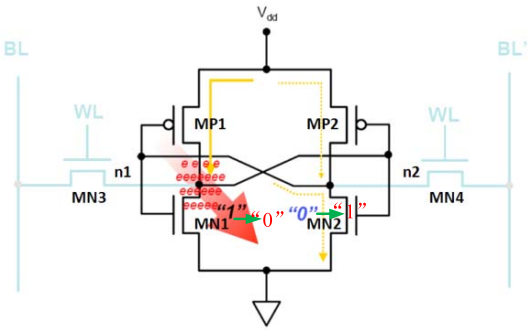

Fig. 2. Bit-flip occurrence in a memory cell.

design method proposed for SEU hardened FPGA. Section IV evaluates the effective performance of the proposed SEU hardened FPGA design. Irradiation test results are given in Section V. Finally, Section VI provides the conclusion.

II. SEU Sensitivity Issues

A generic diagram of an FPGA is shown in Fig. 1, where clustered logic blocks (CLBs) and BRAMs are arranged in a 2-D grid and are interconnected by programmable routing channels. I/O blocks are arranged at the periphery of the grid, and they are also connected to the programmable routing interconnect.

An SRAM-based FPGA employs the static memory cells which are distributed throughout the entire chip to provide configurability. Example of such a memory cell is shown in Fig. 2. Those SRAM cells in FPGA are mainly served for the following purposes: 1) to program the routing interconnect which are generally steered by groups of the individual multiplexors and 2) to program CLBs that are used to implement logic functions.

Fig. 2 illustrates one bit memory cell impacted by an SEU, known as bit-flip. The circuit is desired to maintain state "1." For each state, a pair of p-n transistors is activated while the other pair of p-n transistors should be put OFF. A bit-flip happens when an energetic particle provokes the inversion of the cell state. The similar effect could also happen to a DFF.

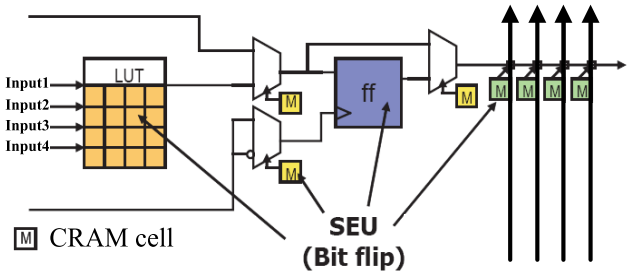

Fig. 3. SEU sensitivity due to CRAM cells.

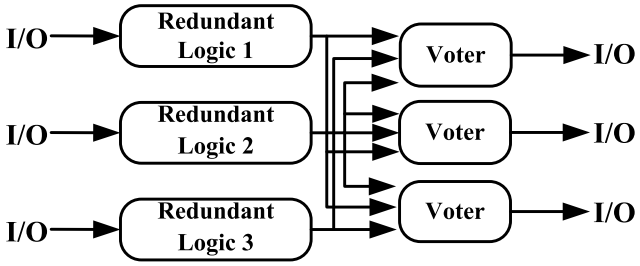

Fig. 4. TMR implementation architecture [8].

In FPGA, an upset in CRAM will impact the combinational or sequential logic circuits mapped onto the programmable architecture. Typically, compared with antifuse- and flash-based FPGA, SRAM-based FPGA can be quickly programed by loading a configuration bitstream (a series of binary codes) into the device. Such a bitstream is normally partitioned in frames and contains all the information necessary to configure the CRAM cells located around the look-up tables (LUTs), flip-flops, CLB control circuits, and interconnections, as shown in Fig. 3. All these configuration bits are extremely sensitive to SEU.

III. FPGA Hardening Techniques

As mentioned earlier, there are generally two ways to reduce the SEU sensitivity for SRAM-based FPGA, i.e., TMR or embedding SEU hardened data storage elements. Those two approaches will be discussed in the following.

A. TMR-Based Techniques

The basic concept of the TMR implementation architecture is to have three identical circuits designed with a majority voter that makes decisions on the three output results. In the case of ASIC, TMR just needs to be applied to the embedded memory, exclusive of those determined logic functions, and interconnections. However, in the case of FPGA, TMR is required for all the CRAM cells besides the embedded memories, since all the logic functions, interconnections, and I/O interfaces are programed by CRAMs. Thus, a large amount of area overheads will be taken [8], as illustrated in Fig. 4.

B. SEU Hardened Elements

The SEU sensitivity of SRAM-based FPGA is essentially decided by DFF and memory (both CRAM and BRAM). Apparently, when those elements are replaced by

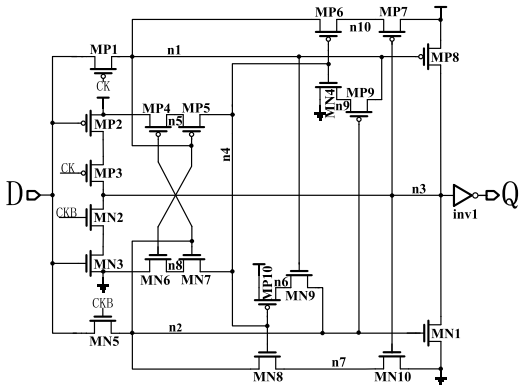

Fig. 5. TILL circuit proposed in [9].

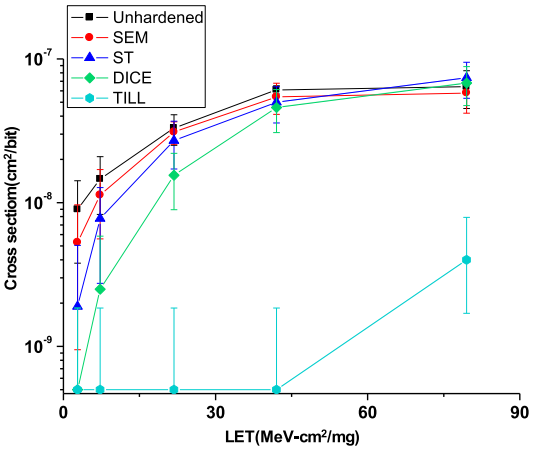

Fig. 6. SEU CS for each type of the latch tested in [9].

SEU hardened designs, the FPGA reliability shall be greatly improved.

1) SEU Hardened DFF: There are two aspects that should be considered in strengthening latch design for even higher SEU tolerant capability. Apart from employing additional locking loops to restore the original state for a transient fault (TF) impacted node, reducing the number of sensitive node pairs (i.e., a single or more particles strike at the latch and cause TFs to simultaneously happen at two nodes (hence corrupting a correct stored state) should be further beneficial.

As shown in Figs. 5 and 6, from four SEU hardened forms, namely, soft error masking, Schmidt trigger, DICE, and TILL proposed in [9], TILL has achieved its SEU threshold of above 42 MeV $\cdot$ cm^2/mg, the highest among the compared designs. SEU radiation hardening efficiency factor (SRHEF) is a metric to take into account the overall performance evaluation for a latch, not only on radiation hardening effect but also on the area and power-delay product (PDP). SRHEF can be used as a guideline for design optimization. Assume that ε, ξ, and γ represent the normalized weight factors for SER, area, and PDP, respectively,

$$\varepsilon + \xi + \gamma = 1. \tag{3.1}$$

Then, we have

$$\text{SRHEF} = \frac{(\text{SER}_{\text{Un}}/\text{SER})^{\varepsilon}}{(\text{Area}/\text{Area}_{\text{Un}})^{\xi} \times (\text{PDP}/\text{PDP}_{\text{Un}})^{\gamma}} \tag{3.2}$$

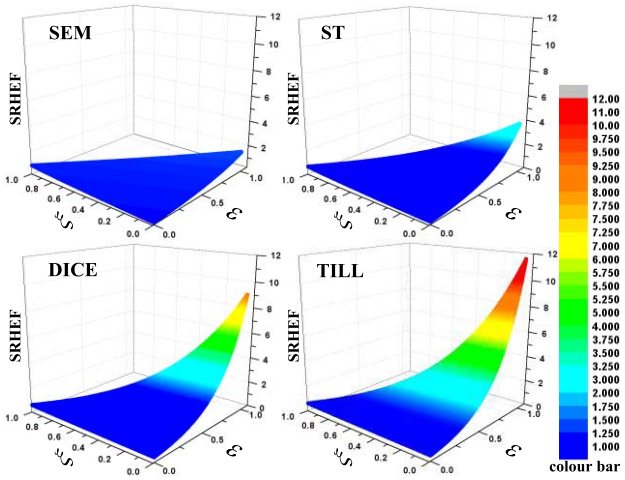

Fig. 7. SEU radiation hardening efficiency factor for each latch analyzed in [9].

where SER_{Un}, Area_{Un}, and PDP_{Un} correspond to the unhardened latch. As the unhardened latch is regarded as a reference design, SRHEF of the unhardened latch should always be 1.

TILL has higher SRHE than the previously hardened latches as shown in Fig. 7. There are about 35 840 DFFs in our FPGA. When all the conventional DFFs were replaced by the TILL DFFs, the area merely increases by about 0.31% in our FPGA design.

2) SEU Hardened Memory: In order to mitigate the soft errors occurred in CRAMs and BRAMS of FPGA, a systematical approach is attempted at both the circuit and the architectural level for the combined effect of improved SEU hardening performance. Several coding schemes for single-error correction (SEC) or double-adjacent error correction have recently been proposed to tackle the SEU problem in memories [10]–[13]. A more robust coding design is presented in [14], combining both double error and burst error correction capabilities for a data word of up to 24 bits, but at a high cost in redundancy. Regarding CRAM or BRAM in FPGA, the SEC coding may be preferable due to its lower area overhead. Hence, the SEC and double error detection (SEC–DED) coding are used. In a way, the SEC–DED coding requires storing seven check bits for a 32-bit data, increasing the memory array size approximately just by 22%. This is compared to the case where the DICE storage cell is implemented, resulting in the memory array size being increased by 100%.

As shown in Fig. 8, the memory structure (either CRAM or BRAM) mainly consists of three parts, namely, memory core, ECC block, and ACC. The process where the data are written to or read from the SRAM array is through the memory core. The ECC block encodes the input data from I/O when in write process and decodes the data from the memory core when in read process. The ACC block is used to examine the content readback from the SRAM cells and further to correct the error bits by writing into the SRAM cells with the recovered code. Such a "identify and repair" operation is carried out in background without any interruptions to the functionality of the whole device. ACC will look through each

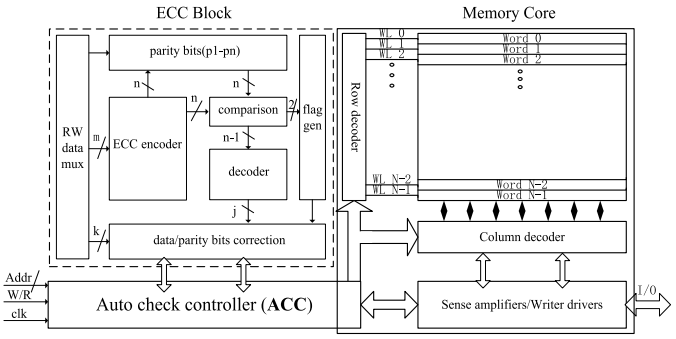

Fig. 8. Architecture diagram of SEU hardened memory.

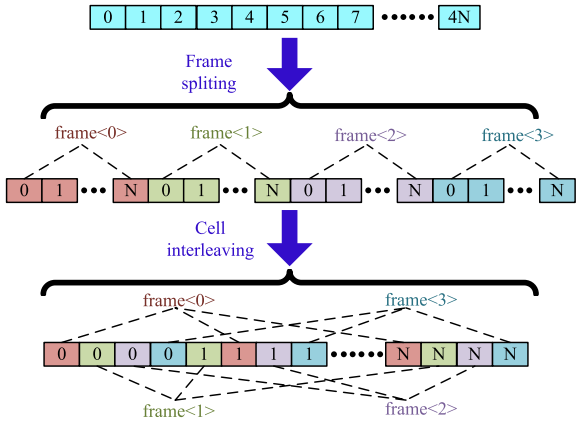

Fig. 9. Fundamental of bit location interleaving in memory.

row of the memory at frequency "clk." Accordingly, failure in ACC becomes then critical for FPGA, TILL has been used to enhance the SEU tolerant capability of ACC.

According to the reliability model for SEC/DED memories with "identify and repair" operation [16], the mean time to failure for embedded FPGA memories can be calculated in the following equation:

$$\text{MTTF} = \frac{2 \times \nu}{M \times \lambda^2 \times N \times (N-1)} \tag{3.3}$$

where ν is the correction rate, λ is the bit failure rate, N is the number of bits in a single word, and M is the number of words in the memory. Thus, MTTF is proportional to ACC frequency.

In order to achieve multibit upset (MBU) mitigations with minimum area overhead of the added-in circuit, the combination measures are taken, as listed below.

a) Scattered locations of the bit cells in the same frame for nonadjacency: The configuration data stream can be split into some smaller frames, and all the bit cells of a frame are scattered over a distance. In [14], a minimum interleaving distance of four to eight is recommended for 150-nm SRAMs. It should, therefore, be larger than four for 130-nm SRAM, say, of 7 bits as shown in Fig. 9 to prevent MBU from happening to the same frame.

b) Built-In single-bit error correction and double-bit error detection: Thus, for scattered cells of a frame, an extended Hamming coding scheme is sufficiently applied

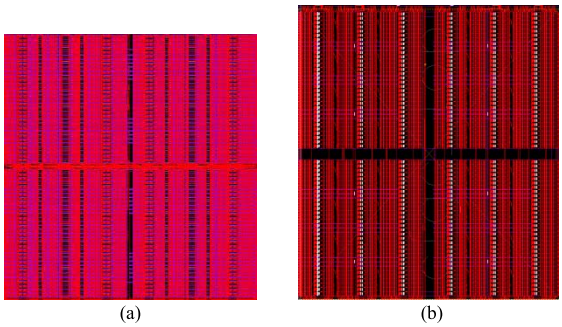

Fig. 10. (a) Layout of the base FPGA design (area = 1.92 cm × 2.04 cm). (b) Layout of the SEU hardened FPGA design (area = 1.98 cm × 2.08 cm).

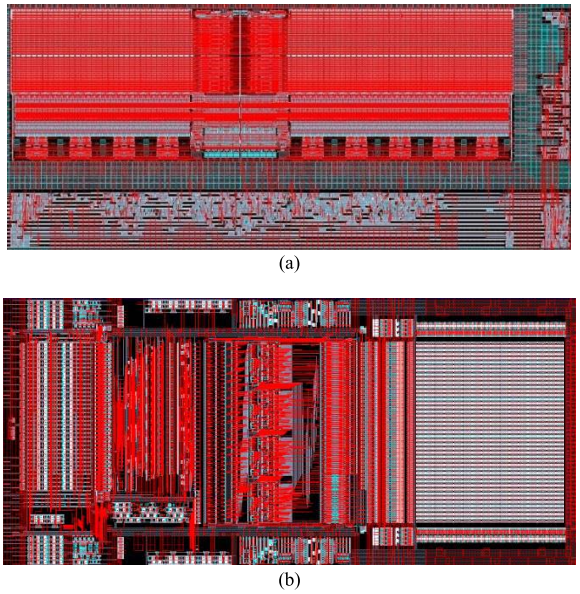

Fig. 11. (a) Layout of the base BRAM design (area = 580 μm × 300 μm). (b) Layout of the SEU hardened BRAM design (area = 646 μm × 300 μm).

to correct any single bit error and detect possible double bit errors.

c) Self-Checking: ACC is designed to run in the background and without any disturbance to normal executions of the circuit function. If an error is detected in a configuration frame or in a memory word, it shall be immediately remedied. For the self-checking operation, CRAM is designed to support the four levels of the running frequency, giving some balanced choices between the SEU hardening performance, and power consumption considerations. BRAM is designed to have the self-checking frequency to be decided by the user clock.

IV. Evaluation

The layout diagrams, respectively, for the base FPGA (without hardening measures included) and for the hardened FPGA designs are shown in Fig. 10. The area overhead arising from added circuitry is estimated as 20.16 mm^2, an increase of merely 5.15%. To further characterize, the layout diagrams, respectively, for the base BRAM design and for the hardened BRAM design are also given in Fig. 11. Floorplan optimization of hardened BRAM has been made to keep shape and data

TABLE I
RESOURCE OF THE FPGA

Logic		I/O		MEMORY	
LUT	DFF	USER I/O	LVDS	BRAM	CRAM
35840	35840	512	256	1728Kbits	4Mbits

TABLE II
ACC_{CRAM} CAN WORK AT FOUR LEVELS OF THE FREQUENCY

Frequency(MHz)	60.00	7.50	0.47	0.06
Increased FPGA current (mA)	38.6	2.9	0.8	0.5
Increased by percent	193.0%	14.5%	4.0%	2.5%

flow consistency. It can be seen that adding of the ACC and the ECC circuitry leads to increasing of the area by 11.42%. In a similar way, the layout area for the CRAM array is also increased for adding the ACC and the ECC circuitries and it is about 3.8%. The test chips for the base FPGA and the SEU hardened FPGA designs have been fabricated on a commercial 0.13-μm bulk CMOS process. Both FPGA designs contain the same programmable resource, 35 840 LUTs, 512 I/Os, 1728-kbits BRAM, and 4-Mbits CRAM in both FPGAs, as shown in Table I.

They were tested at a supply voltage of 1.5 V and at room temperature. The static current of both FPGAs is about 20 mA, and the increased current consumption of the SEU hardened CRAM at different ACC_{CRAM} frequencies is shown in Table II. Taking power consumption and circuit limitations into account, four levels of frequency are designed in ACC_{CRAM}. If the user clock is 10 MHz, ACC_{BRAM} would work at the same frequency, and the increased supply current is 1.5 mA for all BRAMs in FPGA. According to the radiation test results, when ACC circuit works at high frequency, the current would increase accordingly. Also, the SEU tolerant capability is hence greatly improved. Consequently, there should be a compromise between reliability and power consumption.

V. RADIATION EXPERIMENT

Before the radiation tests, the relationship between ACC frequency and flux rate of ion beam had been evaluated to guide the radiation experiment. With fixed ACC frequency, the decreasing of ion flux rate may lead to the decreasing of upsets in the memory. Maximum ion flux rate could be calculated by the evaluation model given in Section V-A. Then, the irradiation environment and test results will be illustrated and analyzed.

A. ACC-Frequency Estimation

As a rule of thumb, the speed for scanning and refreshing the entire CRAM and BRAM arrays should be ten times higher than the flux rate of ions, allowing sufficient time for a bit-flip error to be corrected before the next possible SEU. For around four million CRAM cells and two million BRAM cells existing in our FPGA design, it typically requires about one second to accomplish a checking and correction run at 60 and 10 MHz, respectively. Concerning the radiation process, the flux indicates heavy ions incident in waves into the chip. For convenience of calculation, we assume that the total influx of irons is equally divided and modeled in two consecutive waves.

At the time of impacting by the first wave, the CRAM and BRAM arrays are going through the checking phase. Then, at the next time of impacting by the second wave, the CRAM and BRAM arrays are going through the correction phase. Note that both CRAM and BRAM could correct one bit error in a word. Suppose the flux rate of irons F is taken in ions/(μm$^2 \times 0.5$ S). In order to find the maximum flux rate of irons at which any bit-flip error can be recovered, the following equations are derived:

$$M_{\text{upsets}} = F \times 0.5 \times T \times A_{\text{SRAM}} \tag{5.1}$$

$$A_{\text{affacted}} = M_{\text{upsets}} \times (W_{\text{word}} - 1) \times A_{\text{SRAM}} \tag{5.2}$$

$$N_{\text{upsets}} = F \times 0.5 \times A_{\text{affacted}} < \text{one upset} \tag{5.3}$$

$$F^2 \times 0.25 \times A_{\text{SRAM}}^2 \times (W_{\text{word}} - 1) \times T < \text{one upset} \tag{5.4}$$

$$F < \frac{1}{0.5 \times A_{\text{SRAM}} \times \sqrt{(W_{\text{word}} - 1) \times \text{T}}}. \tag{5.5}$$

A_{SRAM} denotes the area of the SRAM cell, T denotes the total number of the SRAM cells, and W_{word} denotes the word width. M_{upset} is the upset number in first wave (5.1), and A_{affacted} is the area SRAM that is affected by M_{upset} (5.2). If another ion is falling into this area in the same W_{word}, which already has an error, ACC cannot deal with it in this case. So, the upset number N_{upset} in second wave should be no more than 1 (5.4). The maximum flux rate is given in (5.5).

After calculation, the ion flux rate F_{CRAM} for the CRAM array must be less than 416 ions/(cm$^2 \cdot$ S), while the ion flux rate F_{BRAM} for BRAM must be less than 5945 ions/(cm$^2 \cdot$ S). The above-mentioned model is based on the assumptions listed as follows.

1) The incident irons are uniformly distributed across the whole chip.
2) Each ion stands for the same chance to cause an upset.
3) Upsets happening to any pair of the cells within a single word would not occur during the impact by a single wave of ions.

B. Radiation Test

The test chips for both the base FPGA and the hardened FPGA were designed to determine the effectiveness of the SEU hardening measures mentioned above. Furthermore, those FPGA designs were tested at the China Institute of Atomic Energy (CIAE) and the Institute of Heavy Ion Physics of Peking University, Beijing, China, respectively. The irradiation environment and test setup are illustrated in Figs. 12 and 13.

The onsite test system is mainly made up of three parts: the test chip, an SEU detecting board, and an upper stream computer. The storage data from DFF, BRAM, and CRAM were sent in and readback by a commercial FPGA device

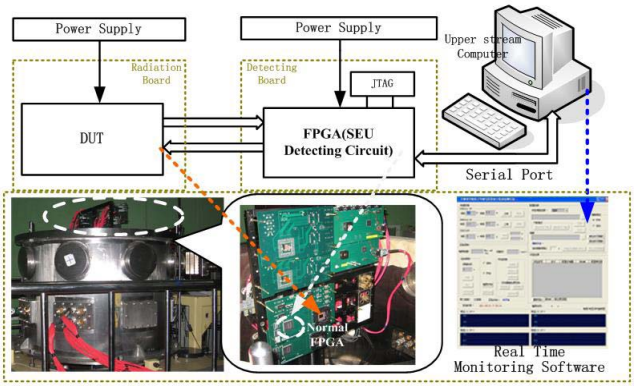

Fig. 12. SEU detecting system and irradiation environmentfor the base FPGA design at CIAE.

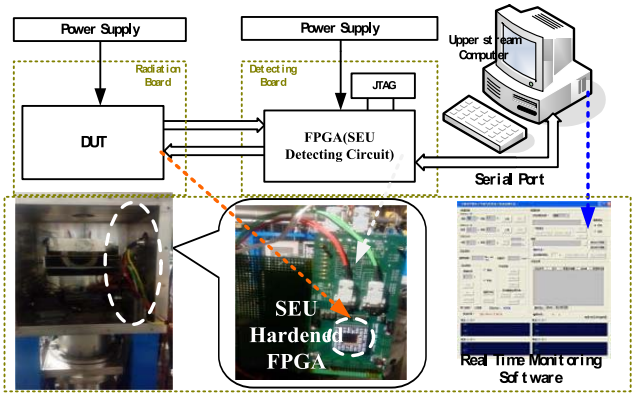

Fig. 13. SEU detecting system and irradiation environment for the SEU hardened FPGA design at Peking University.

TABLE III
CHARACTERISTICS OF ION BEAMS USED AT CIAE

Ion	C	O	Ti
Energy (MeV)	79	100	180
LET (MeV-cm^2/mg)	1.63	3.1	21.8
Range in target (μm)	14	11	34.7
Flux(ions/cm^2*S)	5000		
Fluence(ions)	1E+7		

TABLE IV
CHARACTERISTICS OF ION BEAMS USED AT PEKING UNIVERSITY

Ion	C	F	Si
Energy (MeV)	25	35	40
LET (MeV-cm^2/mg)	3.53	6.78	13.65
Range in target (μm)	25.7	21	14.2
Flux (ions/cm^2*S)	500		
Fluence (ions)	1E+6		

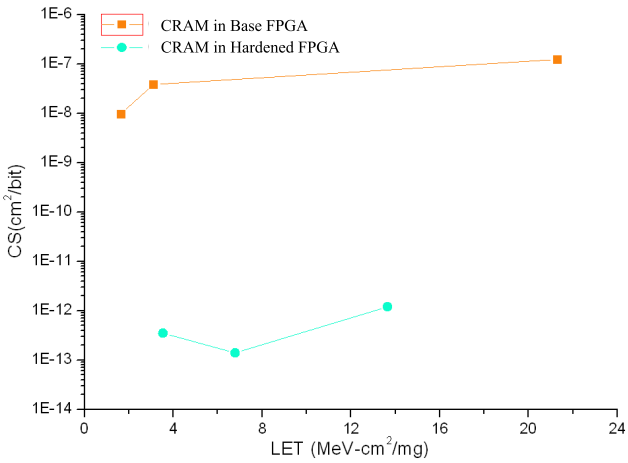

Fig. 14. SEU CS of CRAM.

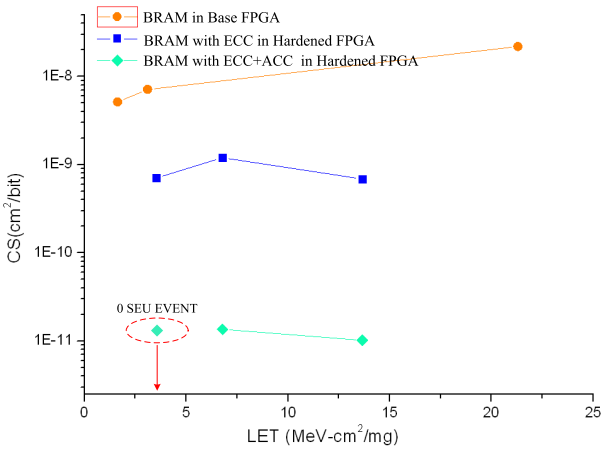

Fig. 15. SEU CS of BRAM.

on the detecting board. When a mismatch is detected, the data are stored and at intervals transported via a cable to the serial port of the upper stream computer for analysis. The test chips together with the SEU detecting boards were placed in the vacuum chamber to minimize the energy loss of incident ions. Three types of heavy ions (e.g., C, F, and Ti) were used in the experiment for the base FPGA design, when the irons C, F, and Si were chosen for test of the SEU hardened FPGA design. Under the irradiation, each chain of memory cells was tested with three different linear energy transfer (LET) levels. The energy, range in target, LET, flux, and fluence of those ions used are listed in Tables III and IV. The chips were tested at a supply voltage of 1.5 V. The ACC operations of CRAM and BRAM in the hardened FPGA design are clocked at 60 and 10 MHz, respectively. The measured SEU cross sections (CSs) of CRAM are given in Fig. 14. It can be seen that, at LET from 3.53 to 13.65 MeV $\cdot$ cm^2/mg, the SEU CS of the hardened CRAM was about 1E$-$12 cm^2/bit, which is at least two orders of magnitude lower compared to the base CRAM. Radiation test results for BRAMs are given in Fig. 15. When only ECC was enabled in the hardened BRAM, its SEU CS was 1 order of magnitude lower than the base BRAM. Especially, when ECC and ACC were both

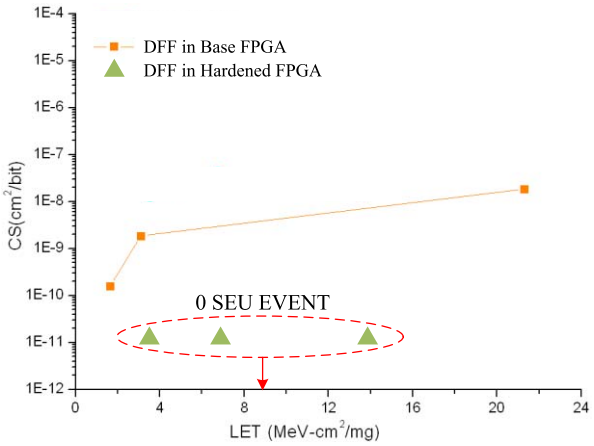

Fig. 16. SEU CS of DFF.

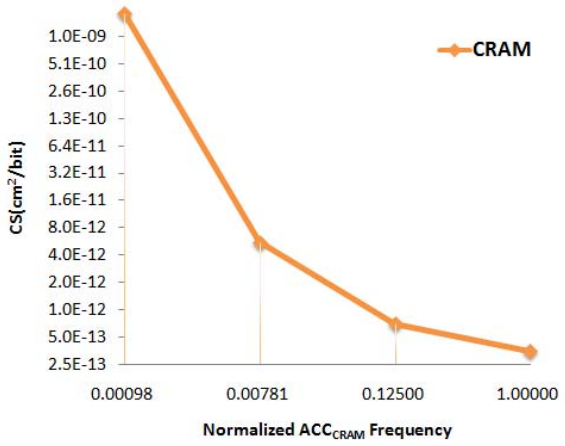

Fig. 17. SEU CS of the CRAM in the hardened FPGA design obtained at different ACC frequencies and with C ion flux rate of 500 ions/(cm^2 · S).

enabled, there was no upset observed under the irradiation by iron C, and the SEU CS of the hardened design is reduced to 1E−11 cm^2/bit, about three orders of magnitude lower compared to the base BRAM. Apparently, at LET from 3.53 to 13.65 MeV · cm^2/mg, there was no SEU happened to the DFFs in the SEU hardened FPGA, as shown in Fig. 16. This is owing to the sufficiently high-LET threshold of the TILL structure used in the design, which is consistency with the observation in [9].

When the ion strikes at a shallow angle, it is expected that the SEU CSs of both the base FPGA and the hardened FPGA gets worse. However, as there is lower percentage of the sensitive node pairs existing in the TILL than in unhardened DFF, superiority of the TILL in terms of the SEU CS should still be valid in the circumstances just mentioned. Similarly, the bit interleaving techniques used in the CRAM and the BRAM designs could also mitigate MBU sufficiently when the ion strikes at a shallow angle. According to (5.5), if the flux is below 416 ions/(cm^2·S), both CRAM and BRAM could efficiently correct the bit error. As shown in Figs. 14 and 15, with LET ranging from 3.53 to 13.65 MeV · cm^2/mg, few upsets happen in both the BRAM and the CRAM memories. Fig. 17 shows as expected that if the flux rate of ion C is 500 ions/(cm^2 · S), SEU CS of CRAM is significantly reduced with the increase of ACC_{CRAM} frequency. More single errors in a word can be corrected at higher ACC frequency as the number of accumulated errors is reduced.

C. Comparison

Comparison between the existing commercial radiation hardened FPGA devices and proposed design will be made in this section. The susceptibility of the previous SEU hardened FPGAs, such as UltraScale, which is Xilinx's first product offering built using TSMC's 20-nm, 20-SoC process, had been previously tested for the purpose of estimating terrestrial upset rates [22]–[26], the radiation test results for Virtex II, Virtex-4, Kintex-7, and Ultrascale are given in Table V. In the same LET range, radiation test results of CRAM, BRAM, and DFF are concluded in Table V. Obviously, the SEU tolerant capacity of the proposed FPGA is better than the previous designs,

TABLE V
SEU TOLERANT CAPABILITY FOR DIFFERENT HARDENED FPGAS

Type	Virtex II	Virtex-4	Kintex-7	Ultrascale	Proposed
Node	130nm	90nm	28nm	20nm	130nm
CRAM (cm^2/bit)	2E-8	8E-9	2E-9	8E-10	1E-12
BRAM (cm^2/bit)	5E-8	1E-8	8E-9	1.5E-9	1E-11
DFF SEU threshold (MeV-cm^2/mg)	<7	<7	<7	<7	>42

which is mainly due to the two following facts: 1) larger device feature size effect, which means when the same charge cloud caused by energetic ions, fewer storage cells may be affected, and 2) combinational measures are used to enhance the SEU tolerant capability of the proposed FPGA, which could dramatically reduce its upset CSs.

VI. CONCLUSION

In this paper, we propose an SEU hardened FPGA design involving high reliability storage cells and error correction mechanism. In comparison to the base (unhardened) FPGA, the area of the hardened FPGA increases just about 5.15%. An ACC_{CRAM} is implemented in the hardened FPGA for background error correction, and it supports four levels of the checking frequency all generated on chip. The frequency of ACC_{BRAM} is determined by the user clock. According to the irradiation experimental results, when ACC_{CRAM} is clocked at 60 MHz, the SEU CS of the hardened CRAM is at least four orders of magnitude lower compared to the base CRAM. Accordingly, when ACC_{BRAM} is clocked at 10 MHz, the SEU CS of the hardened BRAM is about three orders of magnitude lower compared to the base BRAM. Moreover, at LET level of 3.53–13.65 MeV · cm^2/mg, there was no SEU occurring to the DFFs in the hardened FPGA design. Moreover, compared with the previous hardened FPGAs, proposed FPGA exhibits better SEU tolerant capability, which takes the advantage of technology node and multiple hardening measures.

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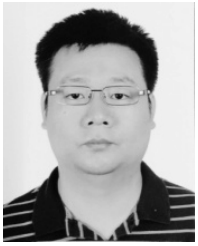

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