A High Performance Gated Voltage Level Translator with Integrated Multiplexer

Dharshak B S and Rahul M. Rao
Email: dharshs1@in.ibm.com
IBM India Private Limited, Bangalore-560045, India

***Abstract*— Multiple supply voltages are commonly used in designs to enable better power performance through dedicated control of the supply voltage of the various functional units. In multiple supply voltage designs, circuits are partitioned into voltage islands that operate at their optimum supply voltages which necessitates the use of voltage level translators between them. This paper presents a high performance voltage level translator design aimed at minimizing insertion penalty by minimizing logic contention and thereby improving latency. In addition, the proposed voltage level translator design has an integrated logic multiplexer function built in through an enable signal. Simulation results of the proposed voltage level translator in comparison with the conventional voltage level translator shows upto 42% delay reduction, combined with a power benefit upto 15%, for supply voltage ranging from near-threshold to above-threshold levels.**

Keywords—Level translator, Near-threshold, Above-threshold, Multiple supply voltages, Logic contention, Latency, Multiplexing.

I. INTRODUCTION

Multiple Supply Voltage Domain (MSVD) is a popular design technique in today's microprocessors and System-on-Chips (SoC) [1]. These designs involve partitioning the microprocessors and SoCs into separate supply voltage domains or voltage islands, wherein each island operates at an optimum supply voltage to meet its timing demands. This enables operation of timing critical regions at higher voltage supply, while running timing non-critical sections at lower supply voltage. Such configurations require a voltage level translator to move signals from the lower supply voltage to the higher voltage supply, without creating excessive shoot through currents. These voltage level translators need to operate over a wide voltage range from near-threshold to nominal or above-threshold depending on the application range and the optimal operating conditions for the various units.

Many voltage level shifters have been discussed in the past, except for the absence of a gated voltage level shifter to control its operation. [2] presents a conventional level shifter using multi-threshold design technique to reduce contention. Unlike the standard level converters based on feedback, the new circuits in [3] avoid feedback and employ multi-threshold transistors in order to reduce contention, which does not fully eliminate standby currents. A subthreshold level converter is demonstrated in [4] by using a cascaded two-stage design to convert signals from subthreshold up to the nominal supply voltage, which while good from a power efficiency point of view, is unsuitable for high performance designs. [5] introduces a combination of NMOS-diode current limiters and multi-threshold CMOS technique to reduce the current contention in the conventional level shifter topology. [6] discusses another multi-threshold CMOS technique for voltage level conversion. The pass-transistor topology described in [7] contains small number of transistors and is a promising level translator to minimize delay and area penalty. However, the existence of pass transistors in [7] causes a reverse current flow originating from the high voltage supply of the level translator and passes through the low voltage supply of the level translator as well as the power supply of the previous logic stage, which is undesirable. Voltage level shifters based on current mirror technique are discussed in [8, 9 and 10]. Some of the above configurations also include some devices that are always *on*, that suffer from device reliability due to aging, especially at higher voltage and temperature operational conditions of high performance designs. A different approach using level translation at flip-flops is presented in [12]. However, this restricts voltage translation to sequential boundaries, thereby restricting design choices.

In this work, a modified voltage level translator that aims to minimize level translator insertion delay, primarily by reducing logic contention is presented. The remainder of the paper is organized as follows: Section II explains the motivation behind the proposed high performance voltage level translator. Section III illustrates the key idea of the proposed voltage level translator to reduce logic contention. Section IV presents the applications of proposed level translator. The simulation results are discussed in section V. Concluding remarks are presented in section VI.

II. PRIOR ART AND MOTIVATION

Fig. 1 shows the conventional voltage level translator which uses cross-coupled PMOS devices to achieve full-swing conversion from input voltage VDIN to output voltage VDOUT. The conventional level translator design shown in Fig.1 is used as a reference for comparison with the proposed level translator design. VDIN and VDOUT are the input and output supply voltages of the level translator respectively, and VSS is the ground connection of the level translator.

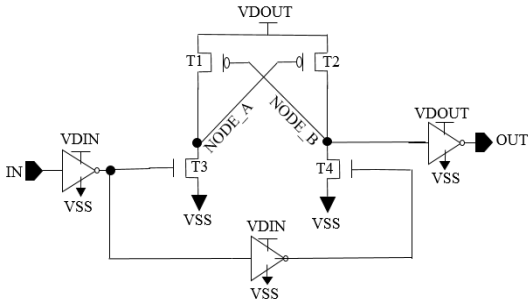

Fig. 1. Conventional Voltage Level Translator

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The PMOS transistors (T1 and T2) act as a cross-coupled load. When the input signal 'IN' is low (logic 0), NMOS transistor T3 is turned *on*, which drives node 'NODE_A' low. Additionally, NMOS transistor T4 is turned *off* and PMOS transistor T2 is turned *on*, due to which node 'NODE_B' is pulled high (logic 1) to VDOUT. Thus, the output signal OUT becomes low. The operation reverses when the input signal 'IN' is switched to high. This conventional voltage level translator has large delay, because it suffers from contention between the pull-down transistors (T3 and T4) and the pull-up transistors (T1 and T2). This paper proposes an approach in which the contention is reduced to gain better performance in delay.

III. PROPOSED VOLTAGE LEVEL TRANSLATOR

The proposed voltage level translator is shown in Fig. 2. The level translator shown has an integrated enable (EN) signal which acts as a control signal with the circuit functioning correctly, when EN='0' and EN_MUX='0'. ENB is the complement of EN. VDIN and VDOUT are the input and output supply voltages of the proposed level translator respectively, and VSS is the ground connection of the proposed level translator.

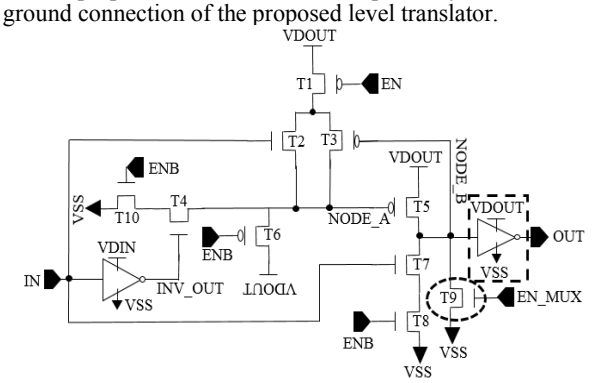

Fig. 2. Proposed Voltage Level Translator

With reference to Fig. 2, assuming that initially the input 'IN' is low, the NMOS transistors T2 and T7 are *off*; the node 'INV_OUT' is high which turns *on* the NMOS transistor T4 and pulls the contention node 'NODE_A' low. Hence, the PMOS transistor T5 is turned *on* and the contention node 'NODE_B' is pulled high to VDOUT voltage, which cuts-off the PMOS transistor T3. Thus the output 'OUT' is low. Now when the input signal 'IN' makes a low to high transition, the NMOS transistors T2 and T7 are turned *on*; the node 'INV_OUT' goes low turning *off* the NMOS transistor T4. Turning *on* the NMOS transistor T2 pulls the contention node 'NODE_A' to VDIN – Vth *(where Vth being the threshold voltage of T2)*. Thus, pulling the contention node 'NODE_A' initially to an intermediate voltage state *(rather than leaving it at its initial VSS, i.e. logic 0 state)* helps the PMOS transistor T3 in pulling 'NODE_A' speedily to VDOUT *(with the assistance of 'NODE_B' going low by the turning 'on' of the NMOS transistor T7)* and turn *off* the PMOS transistor T5 and win the fight against T5. Hence, the 'OUT' node goes high to VDOUT. Subsequently, the contention between the PMOS transistors T3 and T5 during the high to low transition of 'OUT' is overcome by making T3 a little weaker in strength as compared to T5. This facilitates T5 to easily win the fight against T3 *(with the aid of 'NODE_A' going low by turning 'on' of the NMOS transistor T4, driven by 'INV_OUT' going high, along with the NMOS transistor T7 being turned 'off')* and pulls 'NODE_B' to VDOUT; thereby transitioning 'OUT' to VSS. The strength of T3 can slightly be compromised with that of T5, as T3 is being aided by T2 during the low to high transition of 'OUT'.

The Transistors T6 and T9 are sized to be of minimum width as they are functional only while the level translator is turned *off*. Also, these transistors could be of high threshold voltage (HVT) as they do not play a role during the normal operation of the level translator. The rest of the circuit are implemented using regular threshold voltage transistors (RVT) to meet the performance requirements *(though they could be designed with HVT if a different power performance point is desired)*. The transistors T7 and T8 are sized such that the equivalent pull down strength is same as the pull down strength of transistors T4 and T10 together. The input inverter is sized depending on the input slew range to correct the slew of the incoming signal. The pull down to pull up network sizing are in the ratio of approximately 2:1.

IV. APPLICATIONS OF PROPOSED VOLTAGE LEVEL TRANSLATOR

A. Power Gating

The enable signals EN, ENB and EN_MUX in the proposed level translator could effectively be used as fence and partial power gate signals, while the level translator is not being employed for operation.

The normal operation of the proposed level translator requires EN=EN_MUX='0' and ENB='1'; flipping these signals make the level translator non-operational. From Fig. 2, when EN='1' and ENB='0' the transistors T1, T8 and T10 are turned *off* detaching the rest of the circuit from the supplies – VDOUT and VSS. Making EN='1' and ENB='0' turns *on* transistor T6 which in turn shuts *off* transistor T5, thus separating it from the VDOUT supply. The transistor T9 is turned *on* with EN_MUX='1', pulling the 'OUT' to VDOUT. Table I below shows the truth table of the proposed level translator.

TABLE I. TRUTH TABLE OF PROPOSED LEVEL TRANSLATOR

EN *(VDOUT)*	**ENB** *(VDOUT)*	**EN_MUX** *(VDOUT)*	**OUT** *(VDOUT)*
Logic 0	Logic 1	Logic 0	IN
Logic 1	Logic 0	Logic 1	Logic 1
Logic 1	Logic 0	Logic 0	Z

The presence of enable signals in the proposed level translator entitles power saving during non-operating conditions, while the conventional voltage level translator does not support this application.

B. Logic Multiplexing

A pair of proposed voltage level translators can be employed to voltage level translate one of the two signals, originating from different voltage domains VDIN1 and VDIN2, to a common VDOUT voltage domain; by deploying it to function as a multiplexer as shown in Fig. 3. This is enabled through the use of EN in conjunction with the EN_MUX. As shown in Table I, when EN_MUX is a logic low, while EN is logic high, the level trans-

lator output is at a high impedance state. Thus, in Fig. 3, the logic values of the enable signals EN and ENB activates one of the two level translators either to pull up or pull down the 'OUT' node depending on the corresponding input, with the other level translator being in high impedance and low power state as shown in Table II.

TABLE II. TRUTH TABLE OF INTEGRATED MULTIPLEXER

EN_MUX = 0		
EN *(VDOUT)*	**ENB** *(VDOUT)*	**OUT** *(VDOUT)*
Logic 0	Logic 1	IN1
Logic 1	Logic 0	IN2

As shown in Fig. 3, the multiplexing function is implemented at 'NODE_B' of the proposed level translator by excluding the inverter in the dotted box, from Fig. 2, and placing a single inverter of the same drive strength, as in Fig. 2, at the common output.

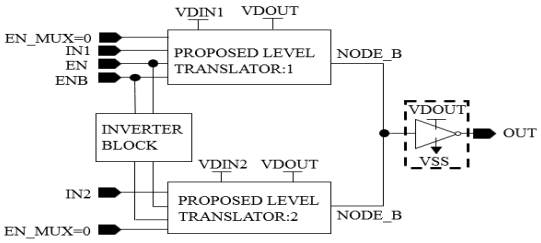

Fig. 3. Multiplexing Application of Proposed Voltage Level Translator

The multiplexing application, using the conventional level translator, could be attained by including a simple 2:1 multiplexer before the level translator. This requires the condition that, both IN1 and IN2 signals are bound to the same voltage domain VDIN. Nevertheless, two signals tied to different voltage domains VDIN1 and VDIN2 can also be multiplexed using the conventional level translator by appending a 2:1 multiplexer after the output of the level translators. However, these two implementations are achieved at the cost of additional delay and power contributed by the extrinsic multiplexer.

V. RESULTS

Simulations are performed for both the discussed level translators in an advanced FinFET Technology at nominal process conditions with input and output voltages (VDIN and VDOUT respectively) ranging from 0.6V to 1.1V using spectre circuit simulator [14]. The simulations are done using identical load FO6 and input slew conditions for both the discussed level translators.

Table III shows the delay improvement (in %) of the proposed level translator as compared to the conventional level translator for their operating voltage range. The "r*ise_delay"* is the delay from rising edge of 'IN' to rising edge of 'OUT', similarly "*fall_delay"* is the delay of the level translator in transitioning a falling edge from 'IN' to 'OUT'. The numbers within '( )' in table III refer to the rise delay improvement, while the numbers within '[ ]' refer to the fall delay improvement. The delays measured are from the 'IN' pin to the 'OUT' pin, in the discussed level translators.

TABLE III. RISE/FALL DELAY IMPROVEMENT OF PROPOSED LEVEL TRANSLATOR (IN % COMPARED TO CONVENTIONAL LEVEL TRANSLATOR)

		VDIN					
		0.6V	**0.7V**	**0.8V**	**0.9V**	**1.0V**	**1.1V**
VDOUT	**0.6V**	(29.34) [12.51]	(26.23) [8.23]	(25.65) [5.79]	(26.15) [3.94]	(27.32) [2.29]	(28.78) [0.71]
	0.7V	(29.91) [18.42]	(25.32) [12.42]	(24.87) [9.11]	(26.20) [6.82]	(28.07) [4.93]	(30.28) [3.20]
	0.8V	(30.92) [24.22]	(24.31) [16.39]	(22.99) [12.12]	(24.29) [9.30]	(26.62) [7.12]	(29.27) [5.25]
	0.9V	(31.93) [30.22]	(23.66) [20.19]	(21.11) [14.98]	(21.79) [11.59]	(24.06) [9.08]	(26.93) [7.02]
	1.0V	(32.42) [36.39]	(23.29) [23.87]	(19.53) [17.74]	(19.36) [13.79]	(21.20) [10.92]	(23.97) [8.64]
	1.1V	(32.17) [42.34]	(22.96) [27.51]	(18.26) [20.40]	(17.22) [15.92]	(18.47) [12.70]	(20.90) [10.19]

The proposed level translator shows a speedup of upto 42% as compared to the conventional level translator; thereby reducing the insertion penalty. This speedup (of > 10%) is fairly consistent across process corners as well, as shown in Fig. 4 which plots the level translator insertion delay of the proposed voltage level translator under different process conditions – TT:nominal, FF:fast-fast, SS:slow-slow, FS:fast-slow and SF:slow-fast. The delays of the proposed level translator are normalized with respect to the conventional level translator. The dotted line represents the delay of the conventional level translator.

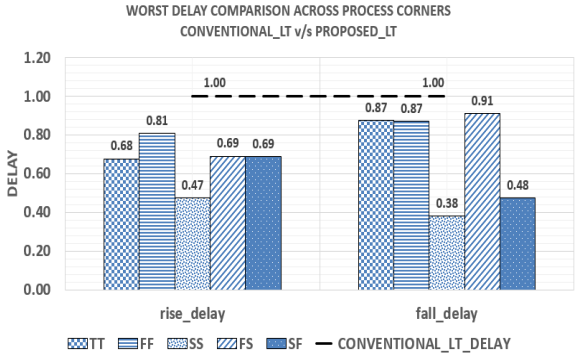

Fig. 4. Worst Delay Comparison across Process Corners

The improved performance also comes with a reduction in the power consumption of the proposed level translator. Table IV shows the percentage reduction in the AC (dynamic) power consumption of the proposed level translator during its operation, as compared to the conventional level translator.

TABLE IV. AC POWER SAVINGS OF PROPOSED LEVEL TRANSLATOR (IN % COMPARED TO CONVENTIONAL LEVEL TRANSLATOR)

		VDIN					
		0.6V	**0.7V**	**0.8V**	**0.9V**	**1.0V**	**1.1V**
VDOUT	**0.6V**	11.74	11.56	11.55	12.12	13.43	15.19
	0.7V	10.36	9.86	9.48	9.32	9.74	10.89
	0.8V	9.39	8.61	8.07	7.54	7.35	7.75
	0.9V	8.74	7.55	7.00	6.31	5.74	5.60
	1.0V	8.37	6.60	6.07	5.39	4.61	4.09
	1.1V	8.22	5.78	5.19	4.60	3.78	3.02

A marginal DC (static) power cost is observed with the proposed level translator as shown in table V. The negative numbers show worse power consumption in the proposed level translator as compared to the conventional level translator.

TABLE V. DC POWER SAVINGS OF PROPOSED LEVEL TRANSLATOR (IN % COMPARED TO CONVENTIONAL LEVEL TRANSLATOR)

		VDIN					
		0.6V	**0.7V**	**0.8V**	**0.9V**	**1.0V**	**1.1V**
VDOUT	**0.6V**	-8.90	-2.29	4.39	10.98	17.36	23.41
	0.7V	-15.05	-9.10	-2.88	3.47	9.82	16.03
	0.8V	-20.12	-14.90	-9.28	-3.36	2.73	8.87
	0.9V	-24.26	-19.76	-14.79	-9.43	-3.76	2.11
	1.0V	-27.64	-23.81	-19.49	-14.72	-9.56	-4.10
	1.1V	-30.38	-27.14	-23.43	-19.26	-14.65	-9.67

In several applications, the voltages at the input and output side of a level translator may vary depending on the performance requirements of the various functional units which may be operated under dynamic voltage and frequency scaling scenarios. Hence, the power consumption of the level translator when going from high to low is as important as when going from low to high, in addition to the scenario where both the input and the output voltage levels are identical.

As discussed in the earlier section, one application of the proposed level translator is that, it effectively can be used to power gate while the level translator is not being employed for operation. Figures 5 and 6 show the power savings obtained by power gating the proposed level translator *(EN='1', ENB='0' and EN_MUX='1')*; for the conditions when 'IN' is switching, and is static respectively. This is done by comparing the power consumption of the proposed level translator, in power gating mode, with that of the un-gated conventional level translator; for the same 'IN' conditions. Power savings in the range of 60 to 95% and 25 to 40%, while 'IN' switching and is static respectively, is benefited while the level translator is non-operational.

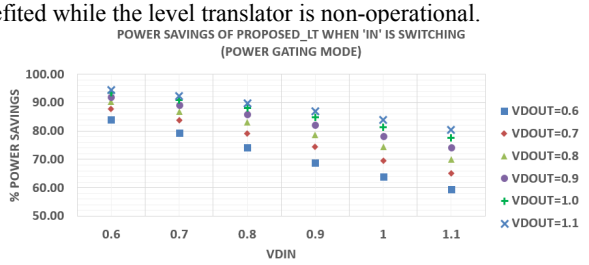

Fig. 5. Power Savings of Proposed Level Translator for 'IN' Switching

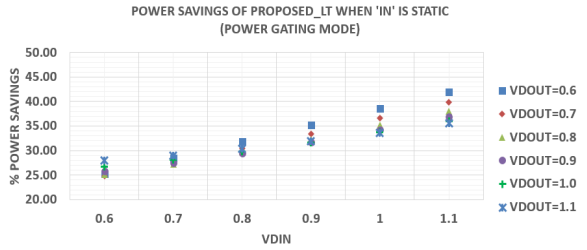

Fig. 6. Power Savings of Proposed Level Translator for 'IN' Static

CONCLUSIONS

This paper proposes a voltage level translator for high speed applications with increased performance by reducing the logic contention which facilitates lower delays in transmitting both rising and falling edges from input to output of the level translator. The integration of enable signal into the level translator allows controlling its functionality and entitles it for power saving and logic multiplexing applications. Around 42% improvement in speed is observed in the proposed voltage level translator, and a minimum of 10% across process corners. In addition, upto 15% reduction in the power consumption of the proposed level translator is noticed. A significant power savings is also observed while the proposed level translator is deployed in power gating mode, as compared to the un-gated conventional level translator.

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