A Very Compact CMOS Analog Multiplier for Application in CNN Synapses

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***Abstract*—This work presents a CMOS analog multiplier architecture for application as the synapse in analog cellular neural networks. The circuit comprises two voltage-mode inputs and a current-mode output. Simulated performance features obtained from a circuit design in CMOS 130 nm technology include: ±100 mV input voltage range, 23 µW static power, -32 dB maximum total harmonic distortion and -3 dB bandwidth of 51.2 kHz. The active area totalizes only 40 µm².**

***Index Terms*—CMOS analog multiplier, analog CNN, synapse.**

I. Introduction

THE last twenty years have witnessed the emergence of a renewed application field for analog electronics: the processing of analog signal generated by ubiquitous micro-sensors [1]. For this purpose, an analog cellular neural network (CNN) is very attractive, thanks to its reconfigurable nature and its high density computing ability, allowing the adaptive processing of signals originated from connected sensor arrays.

An analog CNN cell must comprise weighting synapses, which are usually implemented by analog multipliers. Compact, low-power and low-distortion architectures should be adopted for these multipliers. Besides, a current-mode output is more than welcome, in order to simplify signal summation. In [2], [3] CMOS analog multipliers for the application as CNN synapses are proposed with good performance regarding distortion, power consumption and sensitivity with respect to supply voltage, temperature and technology parameters. However, silicon area has not been optimized and a current-mode input is used to represent each synapses weight. Therefore, for the operators adjustment based on cell stage voltage, a linear voltage-to-current converter is required thus increasing circuit complexity and consumption. Besides, the voltage-mode input of these multipliers is constrained to a small signal range in order to assure the operation of input MOSFET in the linear region. Such limitation can approach signal operation to the noise floor.

In this work, a CMOS analog multiplier with two voltage-mode inputs and a current-mode output is proposed and analyzed through simulation. The input voltage range has been significantly augmented compared to that of [2], [3]. Circuit size reduction is another important aim of this architecture, which is described in Section II. In Section III simulated performance features are assessed and in Section IV the applicability of this multiplier as a CNN synapse is observed.

II. Multiplier Architecture

The CMOS analog voltage-mode multiplier here proposed requires input signal application to the gate and source terminals of input transistors. This input-type approach is also adopted by the multipliers of [4]-[6]. However, the architecture of [4] requires operational amplifiers and resistors to accomplish signal inversion. The multipliers of [5], [6] on the other hand, are quite similar to ours but use slightly different arrangements for signal application and do not include the current subtractor module.

The complete architecture of the proposed multiplier is presented in Fig.1. The blocks for subtraction, level shifting and voltage references generation are detailed in Fig.2.

In Fig.1, transistors M_1 to M_4 compose the multiplier core. Provided operation in strong inversion and saturation, their drain currents are given by [7]:

$$i_{D1,2} = K_1\left(\frac{v_{G1,2}}{n_N} - v_{S1} + \frac{n_N - 1}{n_N}V_{SS} - \frac{V_{T0N}}{n_N}\right)^2 \qquad (1.a)$$

$$i_{D3,4} = K_1\left(\frac{v_{G2,1}}{n_N} - v_{S3} + \frac{n_N - 1}{n_N}V_{SS} - \frac{V_{T0N}}{n_N}\right)^2 \qquad (1.b)$$

where K_1 is a constant proportional to transistor aspect-ratio, supposed equal for transistors M_1 to M_4, and n_N and V_{T0N} are the slope factor and the threshold voltage in equilibrium, respectively, for the n-channel MOS transistors.

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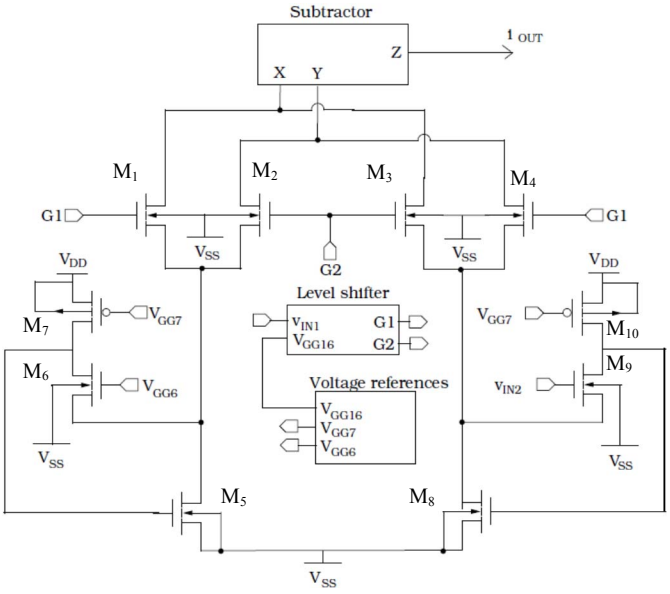


Fig. 1. Proposed CMOS analog multiplier architecture

Since $i_{OUT} = i_{D1} + i_{D3} - (i_{D2} + i_{D4})$, we obtain from (1), after some algebra:

$$i_{OUT} = \frac{2K_1}{n_N}(v_{G1} - v_{G2})(v_{S3} - v_{S1}) \qquad (2)$$

Therefore, this simple principle, also exploited in [4] and [5] gives rise to fully differential four-quadrant multipliers. Nevertheless, for the purpose of this work, which is using the analog multiplier as a CNN synapse, the input signals v_{in1} and v_{in2} are applied to gate and source terminals, respectively, as depicted in Figs.2(a) and 1.

In Fig.1, p-channel MOS transistors M_7 and M_{10} act as current sources, so that the currents of M_6 and M_9 are constant. Thus, the gate voltages of M_6 and M_9 are transferred with a level shift to their source terminals, which are connected to the source terminals of M_1 and M_2 and of M_3 and M_4, respectively. According to most compact MOSFET models, as the one of [7]:

$$v_{S1,3} = \frac{v_{G6,9}}{n_N} - \frac{n_N - 1}{n_N}V_{SS} + \frac{V_{T0N}}{n_N} - \phi_t f\left(\frac{I_{D6,9}}{I_{S6,9}}\right) \qquad (3)$$

where ϕ_t is the thermal voltage, $f(\ )$ is a dimensionless function valid from weak to strong inversion and I_{Sx} is the specific current, proportional to transistor M_x aspect-ratio. Provided equal sizes and biasing currents for M_6 and M_9, the shifted level in (3) is the same for both source voltages.

In Fig.2(a), the drain currents of M_{13} and M_{15} are also made constant by current sources M_{14} and M_{16}. Thus, gate voltages of M_{13} and M_{15} are transferred with a level shift to their sources, which are connected to gate terminals of M_1 and M_4 and of M_2 and M_3, respectively:

$$v_{G1,2} = \frac{v_{G15,13}}{n_P} + \frac{n_P - 1}{n_P}V_{DD} - \frac{V_{T0P}}{n_P} - \phi_t f\left(\frac{I_{D15,13}}{I_{S15,13}}\right) \qquad (4)$$

where n_P and V_{T0P} are the slope factor and threshold voltage in equilibrium, respectively, for p-channel MOS transistors. Provided equal sizes and biasing currents for M_{13} and M_{15}, the level shift in (4) is the same for both source voltages.

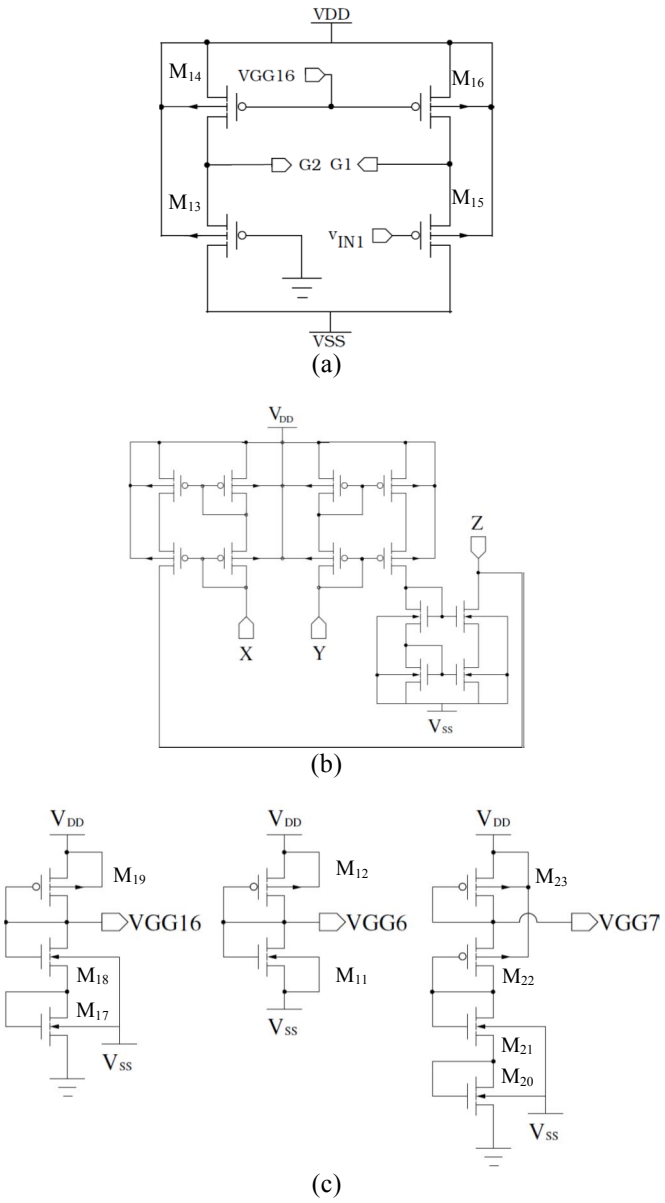


Fig. 2. Detailing of blocks in Fig.1: (a) Level shifter; (b) Current subtractor; (c) Voltage references.

In this multiplier, as depicted in Figs.1 and 2(a), the input voltages v_{in1} and v_{in2} are applied to M_{15} and M_9 gate terminals respectively. The gate terminal of M_{13} is grounded and a constant voltage V_{GG6} is applied to the gate terminal of M_6. Therefore, (2) is rewritten as:

$$i_{OUT} = \frac{2K_1}{n_P n_N^2}v_{in1}(v_{in2} - V_{GG6}) \qquad (5)$$

Fig.2(b) shows that current subtraction is accomplished through three cascoded mirrors, as in [2]. The constant gate voltages of transistors M_6, M_7, M_{10}, M_{14}, and M_{16} are obtained from the active loads voltage dividers of Fig.2(c).

III. Simulation Results

The proposed multiplier has been designed in CMOS 130 nm technology leading to the sizes related in Table I. Bias voltages are presented in Table II. Several simulations through ELDO in Mentor Graphics Tools have been carried out in order to analyze its performance.

TABLE I
TRANSISTOR SIZES

	Transistor	W (μm)	L (μm)
Core	M_1-M_4	0.20	3.00
Source signal application	M_5, M_8	0.50	2.00
	M_6, M_9	0.25	2.00
	M_7, M_{10}	0.50	4.00
Level shifter	M_{13}-M_{16}	0.25	1.00
Voltage references	M_{11}	6.00	0.50
	M_{12}	0.25	3.40
	M_{17}, M_{18}	0.20	5.00
	M_{19}	1.10	1.00
	M_{20}-M_{22}	0.20	0.50
	M_{23}	4.40	1.00
Subtractor	All	5.00	0.25

TABLE II
BIAS VOLTAGES

V_{GG6} (V)	V_{GG7} (V)	V_{GG16} (V)
-0.400	0.550	0.442

A. Standard Operation

The simulation results here presented have been obtained for V_{DD} = -V_{SS} = 0.6 V, temperature of 27 ºC and typical technology parameters. Fig.3 illustrates the multiplier DC transfer characteristics, which reveal that signal excursion can be satisfactorily set to ±100 mV around bias, for both inputs. Fig.4 presents the variation of the simulated total harmonic distortion (THD) with different amplitudes of a sinusoidal signal of 1 kHz applied to one of the inputs, while a constant value is applied to the other input.

Other performance features are summarized in Table III, where a comparison is made with the analog multiplier of [3].

TABLE III
PERFORMANCE FEATURES OF MULTIPLIERS

		Proposed	[3]
input range	x	±100 mV	±20 mV
	y	±100 mV	±200 nA
output range		±100 nA	±150 nA
THD		< -32 dB††	< -32 dB
-3dB bandwidth		51.2 kHz††	4.0 MHz
rms noise current		9.1 nA	5.0 nA
static power		23 □W	15 □W
active area†		40 □m²	703 □m²

† summation of all W-L products
†† regarding input v_{in1}

B. PVT Simulations

The multiplier DC transfer characteristics have also been simulated considering variations in technology parameters, supply voltages and temperature. Figs. 5 to 7 illustrate the results.

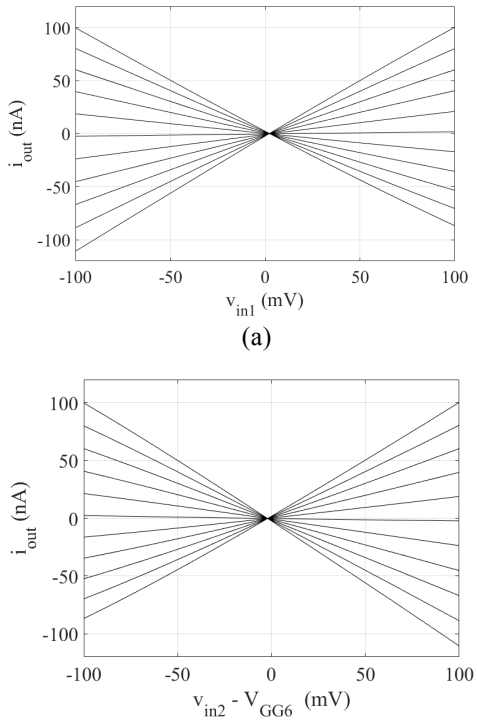


Fig. 3. Multiplier DC transfer characteristics: (a) i_{out} *vs.* v_{in1}, with $v_{in2} - V_{GG6}$ varying from -100 mV to 100 mV with steps of 20 mV; (b) i_{out} *vs.* $v_{in2} - V_{GG6}$, with v_{in1} varying from -100 mV to 100 mV with steps of 20 mV. (V_{GG6} = 400 mV).

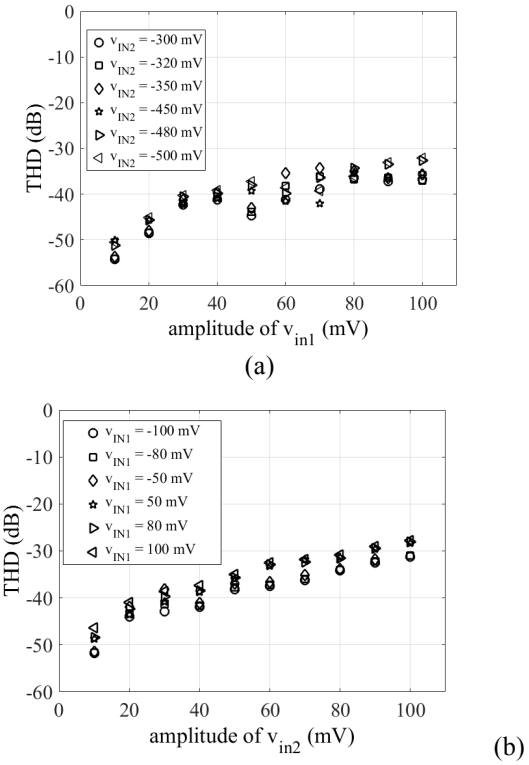
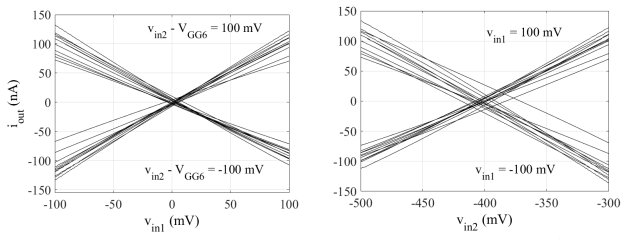
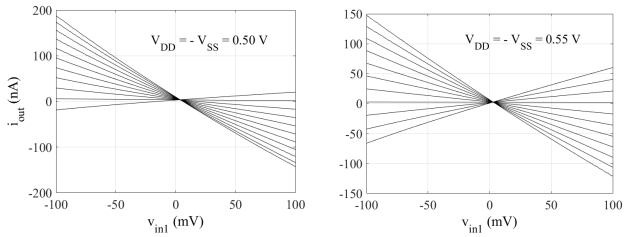


Fig. 4. Multiplier Total Harmonic Distortion: (a) v_{in1} sinusoidal (1 kHz) and constant v_{in2}; (b) $v_{in2} - V_{GG6}$ sinusoidal (1 kHz) and constant v_{in1}. (V_{GG6} = 400 mV).



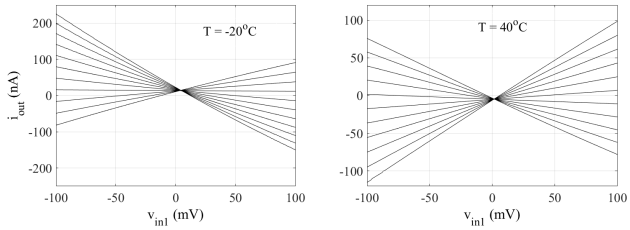
(a) (b)

Fig. 5. Monte Carlo analysis for DC tranfer characteristics: (a) i_{out} *vs.* v_{in1} with $v_{in2} - V_{GG6} = \pm 100$ mV and (b) i_{out} *vs.* v_{in2} with $v_{in1} = \pm 100$ mV.



(a) (b)

Fig. 6. Multiplier DC transfer characteristics i_{out} *vs.* v_{in1}, with $v_{in2} - V_{GG6}$ varying from -100 mV to 100 mV with steps of 20 mV. Supply voltages $V_{DD} = - V_{SS}$ equal to: (a) 0.50 V; (b) 0.55 V.

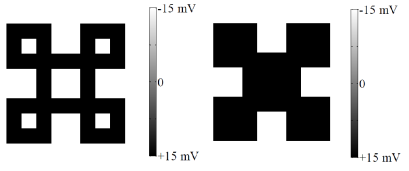


(a) (b)

Fig. 7. Multiplier DC transfer characteristics i_{out} *vs.* v_{in1}, with $v_{in2} - V_{GG6}$ varying from -100 mV to 100 mV with steps of 20 mV: (a) T = -20 ºC; (a) T = 40 ºC.

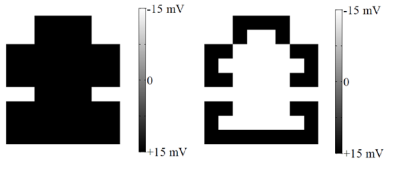
IV. CNN SIMULATION

Preliminary simulations have been accomplished after replacing the synapses by the proposed multiplier in the analog CNN implemented in [2], with 10 x 10 cells of the FSR (Full Signal Range) type. The results for two different binary image processing functions are shown in Figs. 8 and 9.



(a) (b)

Fig. 8. Simulation results for the hole filler image processing function: (a) initial image and (b) final image.



(a) (b)

Fig. 9. Simulation results for the border extractor image processing function: (a) initial image and (b) final image.

The voltage values representing image pixels have been assigned to the input v_{in1} of the proposed multiplier, because the distortion level regarding this input is slightly lower. Since the coefficients values for each image processing function tolerate a small spreading without damage to the implementation, they have been assigned to the input v_{in2}.

V. CONCLUSION

The proposed CMOS voltage-mode analog multiplier, here designed in 130 nm technology and analyzed through simulation, comprises adequate features for its application as synapses: a very compact topology, low power consumption, satisfactory distortion level and input voltage range of $\pm$100 mV. In comparison to the multiplier of [3], this architecture reveals more sensitivity to the variation of technology parameters, supply voltages and temperature. However, since the linearity regarding each input is not dramatically affected by these variations, this problem can be mitigated by replacing the voltage reference generators by high performance structures. This would negligibly impact over circuit power and area of a CNN because the voltage reference generators are unique for all cells. Although significantly reduced with respect to the circuit of [3], the frequency bandwidth is still adequate for the aimed application.

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