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Low Phase Noise Ku-Band VCO With Optimal Switched-Capacitor Bank Design

Peeyoosh Mirajkar, Jagdish Chand, Sankaran Aniruddhan, and Srinivas Theertham

***Abstract*— In this brief, a low phase noise Ku-band voltage-controlled oscillator (VCO) fabricated in a 130-nm BiCMOS process is presented. The phase noise mechanism of the switched-capacitor bank is analyzed, an optimum bank design to reduce phase noise is proposed, and a tradeoff with tuning range is discussed. The prototype 12.2–13.1-GHz VCO achieves a measured phase noise of −120.6 dBc/Hz at 1-MHz offset when running at 12.67 GHz. The VCO core consumes a power of 17.7 mW and attains a figure of merit of 190.**

***Index Terms*— Low phase noise, switched-capacitor bank noise, voltage-controlled oscillator (VCO).**

I. Introduction

Voltage-controlled oscillators (VCOs) are widely used in wireless communication systems as the key component in frequency synthesizers to generate a high-frequency carrier signal. High spectral purity of this signal is important, because reciprocal mixing leads to the degradation of signal-to-noise-ratio. Designing a low phase noise VCO without degrading other performance parameters requires rigorous analysis of phase noise and optimum design of building blocks. In this brief, the phase noise contribution from the coarse-tuning switched-capacitor bank of the VCO is analyzed in detail, and a technique for its optimal design to achieve lower phase noise is proposed.

This brief is organized as follows. Section II analytically describes the phase noise contributed by the switched-capacitor bank and optimum design strategy. Section III discusses the implementation of the proposed VCO along with design choices. Section IV discusses silicon measurement results of the prototype VCOs.

II. Switched-Capacitor Bank: Noise Analysis

A VCO switched-capacitor cell is typically implemented in differential fashion, as shown in Fig. 1. Each capacitance unit is denoted by C_{SW}. M_{SW} connects or disconnects C_{SW} to the tank in a differential manner. MOS transistors M_{B3-4} set the bias voltages of the internal nets int_p and int_m to 0 V when the switched-capacitor cell is turned ON. Transistors M_{B1-2} set the bias voltages of internal nets through bias resistors R_B such that the junctions of M_{SW} do not breakdown in the presence of high voltage swings. The optimum value of R_B is chosen as a tradeoff between quality factor of the switched-capacitor cell in OFF-state and phase noise. The noise of the switched-capacitor cell in ON and OFF-states is discussed below.

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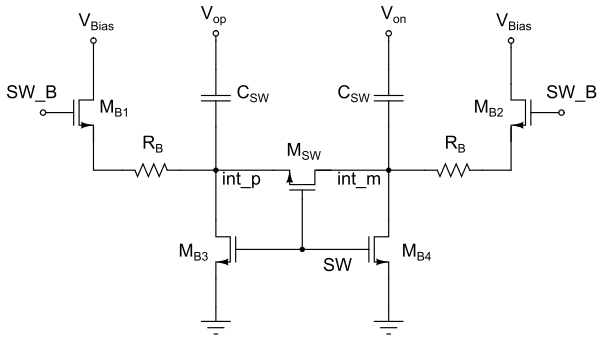

Fig. 1. VCO switched-capacitor cell.

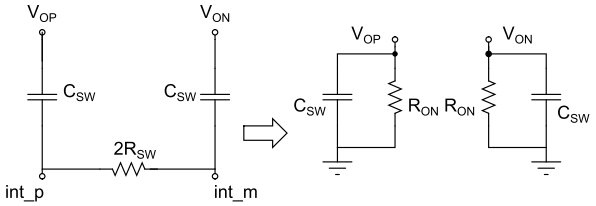

Fig. 2. Equivalent circuit of switched-capacitor cell in ON-state.

A. Noise in ON-State

Fig. 2 shows the equivalent circuit of the switched-capacitor cell in ON-state. The ON-resistance of the switch MOSFET M_{SW} in triode state is denoted by $2 \cdot R_{\mathrm{SW}}$. In the corresponding parallel equivalent circuit shown in Fig. 2, the equivalent resistance is determined to be

$$R_{\mathrm{ON}} = \frac{1}{\omega_0^2 \cdot C_{\mathrm{SW}}^2 \cdot R_{\mathrm{SW}}} \tag{1}$$

where ω_0 is the oscillation frequency of VCO. This resistance R_{ON} is in parallel with the resonant tank and directly contributes a phase noise equal to

$$N\_R_{\mathrm{ON}} = \left(\frac{R_{\mathrm{Tank}}}{R_{\mathrm{ON}}}\right) \cdot N\_R_{\mathrm{Tank}} \tag{2}$$

where N_R_{Tank} is the noise power spectral density (V^2/Hz) of the equivalent parallel resistance of the loaded tank, with all loading except switched-capacitor bank being considered.

B. Noise in OFF-State

Fig. 3 indicates the circuit of the switched-capacitor cell in OFF-state. Capacitance C_{PAR} consists of parasitic diode capacitance and overlap capacitance of M_{SW}, and is inherently nonlinear. For a narrow band of frequencies around the oscillation frequency, the network can be simplified through a parallel-to-series impedance transformation, as shown in Fig. 4. Since V_{Bias} is at ac ground, R_B and C_{PAR} are in parallel for small-signal noise computations.

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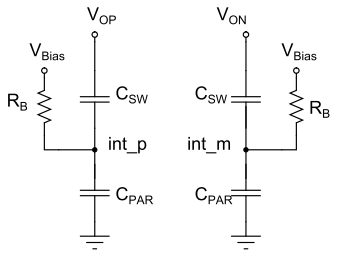

Fig. 3. Switched-capacitor cell in OFF-state.

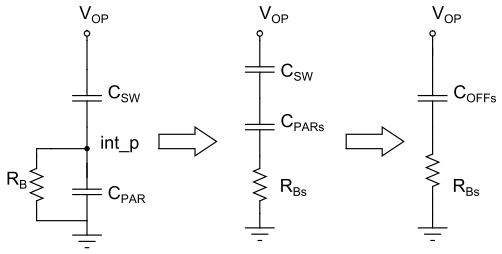

Fig. 4. Narrow-band equivalent circuit of switched-capacitor cell in OFF-state.

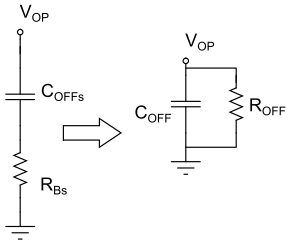

Fig. 5. Simplified parallel equivalent circuit in OFF-state.

Let Q_P be the quality factor of this parallel combination. The equations governing this transformation are as follows:

$$Q_P = \omega_0 \cdot C_{\mathrm{PAR}} \cdot R_B \tag{3}$$

$$R_{\mathrm{Bs}} = \frac{R_B}{(Q_P+1)^2} \simeq \frac{R_B}{Q_P^2} \tag{4}$$

$$C_{\mathrm{PARs}} = C_{\mathrm{PAR}} \cdot \frac{Q_P^2}{(Q_P+1)^2} \simeq C_{\mathrm{PAR}} \tag{5}$$

$$C_{\mathrm{OFFs}} = \frac{C_{\mathrm{SW}} \cdot C_{\mathrm{PAR}}}{C_{\mathrm{SW}} + C_{\mathrm{PAR}}}. \tag{6}$$

Finally, the network can be reduced to the parallel equivalent half circuit in Fig. 5, which is useful for noise derivations. The components of this network, C_{OFF} and R_{OFF}, are given by the following equations:

$$Q_S = \frac{1}{\omega_0 \cdot C_{\mathrm{OFFs}} \cdot \mathrm{Bs}} \tag{7}$$

$$C_{\mathrm{OFF}} = C_{\mathrm{OFFs}} \cdot \frac{Q_S^2}{(Q_S+1)^2} \simeq C_{\mathrm{OFFs}} \tag{8}$$

$$R_{\mathrm{OFF}} = R_{\mathrm{Bs}} \cdot \left(1+Q_S^2\right) \simeq R_{\mathrm{Bs}} \cdot Q_S^2 \tag{9}$$

$$R_{\mathrm{OFF}} = \frac{R_B}{Q_P^2} \cdot Q_S^2 = R_B \cdot \left(\frac{C_{\mathrm{SW}} + C_{\mathrm{PAR}}}{C_{\mathrm{SW}}}\right)^2. \tag{10}$$

Let $\delta C = C_{\mathrm{ON}} - C_{\mathrm{OFF}}$ indicate the single-ended capacitance switched by one cell, and $C_{\mathrm{ON}}/C_{\mathrm{OFF}}$, its efficiency. There exists a tradeoff between quality factor and $C_{\mathrm{ON}}/C_{\mathrm{OFF}}$ [1]. In OFF-state, R_B is the physical element that contributes to noise, and this

	V_{Bias}(V)	R_B(kΩ)	C_{SW}(fF)	M_{SW}(um)
Pt 1	1.60	6	88	160.38
Pt 2	1.60	3	88	160.38
Pt 3	1.15	6	88	160.38
Pt 4	1.60	6	100	160.38
Pt 5	1.60	6	88	320.76

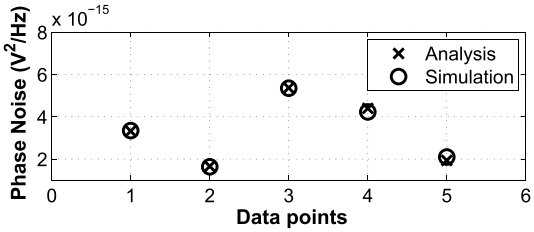

Fig. 6. Phase noise of R_B by indirect mechanism: simulation versus analysis.

happens through two mechanisms: direct and indirect. In the direct mechanism, R_{OFF} is in parallel with the resonant tank and directly adds noise to the output, whose value is

$$N\_R_{\mathrm{OFF}} = \left(\frac{R_{\mathrm{Tank}}}{R_{\mathrm{OFF}}}\right) \cdot N\_R_{\mathrm{Tank}}. \tag{11}$$

In the indirect mechanism, noise of R_B modulates the voltage across nonlinear capacitance C_{PAR}, contributing to phase noise. This can be modeled through a linear gain factor K_{PAR} as

$$\delta C_{\mathrm{PAR}} = K_{\mathrm{PAR}} \cdot \overline{V_{n,R_B}}. \tag{12}$$

A Taylor series approximation for variation in C_{OFF} yields

$$\delta C_{\mathrm{OFF}} \simeq \delta C_{\mathrm{PAR}} \cdot \left(\frac{C_{\mathrm{SW}}}{C_{\mathrm{SW}} + C_{\mathrm{PAR}}}\right)^2. \tag{13}$$

Since this is for the single-ended circuit, the actual change in differential tank capacitance, δC_{Diff}, is equal to $\delta C_{\mathrm{OFF}}/4$. The change in oscillation frequency is

$$\delta\omega \simeq \omega_0 \cdot \left(\frac{\delta C}{C_{\mathrm{ON}}}\right)^2 \cdot \frac{K_{\mathrm{PAR}} \cdot \overline{V_{n,R_B}}}{8 \cdot C_{\mathrm{Tank\_Diff}}}. \tag{14}$$

We now define a quantity $K_{\mathrm{PAR\_unit}}$ that denotes change in unit capacitance for unit change in voltage across it. It is equal to $K_{\mathrm{PAR}}/C_{\mathrm{PAR}}$, is dependent only on process and biasing voltage V_{Bias}, and is independent of switch size. If V_o denotes the VCO output amplitude, the phase noise contributed by R_B through this mechanism at offset frequency $\Delta\omega$ is

$$L\{\Delta\omega\} = 10 \cdot \log\left[\left(\frac{K_{\mathrm{PAR\_unit}}}{4\cdot\sqrt{2}}\right)^2 \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \left(\frac{C_{\mathrm{PAR}}}{C_{\mathrm{Tank\_Diff}}}\right)^2 \cdot \left(\frac{\delta C}{C_{\mathrm{ON}}}\right)^4 \cdot \frac{\overline{V_{n,R_B}^2}}{V_o^2}\right]. \tag{15}$$

Thus, phase noise contributed through the indirect mechanism can be decreased by: 1) reducing $K_{\mathrm{PAR\_unit}}$; 2) reducing R_B; 3) converting fixed capacitance into switched capacitor while keeping δC constant; and 4) reducing $C_{\mathrm{ON}}/C_{\mathrm{OFF}}$. When this noise becomes smaller than that through the direct mechanism, increasing switch size further does not help in reducing overall VCO phase noise. The result of (15) has been compared with SpectreRF simulations on a simplified VCO circuit (without parasitics) to extract the indirect noise contribution for different values of components used in the switched-capacitor cell. The results are plotted in Fig. 6, indicating the correctness of the foregoing analysis.

The basic characteristic of $K_{\mathrm{PAR\_unit}}$ with V_{Bias} is similar for low-voltage and high-voltage MOS transistors in the same process, as

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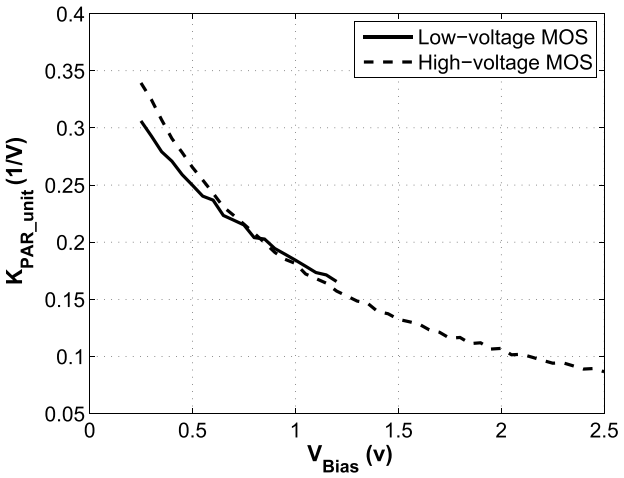

Fig. 7. Simulated behavior of K_{PAR_unit} with V_{Bias}.

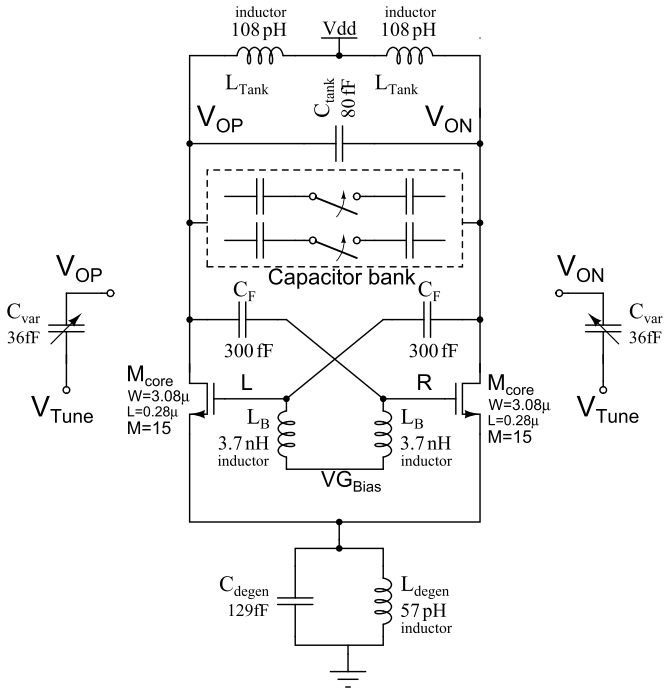

Fig. 8. Ku-band VCO circuit details.

shown in Fig. 7. It is evident that using the high-voltage MOS device allows a larger bias voltage to be applied at its drain (source), thus reducing phase noise contribution through the indirect mechanism in OFF-state. Since the high-voltage MOS device presents larger parasitic capacitance, $(\delta C/C_{ON})$ is smaller, reducing noise even further. Thus, if the VCO is not limited by tuning range, high-voltage MOS devices should be used to realize the capacitor bank switches.

III. VCO Implementation

For a given operating frequency, increasing VCO output power and tank quality factor helps to minimize phase noise. In this brief, the cross-coupled oscillator topology has been selected based on the requirements of ultralow phase noise and comparatively relaxed constraints on power. Fig. 8 indicates the circuit details of the above-mentioned VCO, designed to operate at a center frequency of 13.5 GHz and a differential output voltage swing of 2.6 V. A tail current source is avoided to increase VCO swing, and inductors

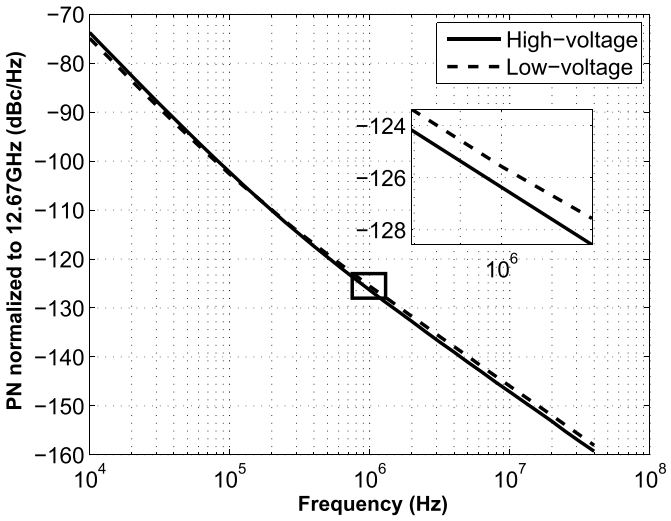

Fig. 9. Simulated phase noise of the two VCOs, normalized to 12.67 GHz.

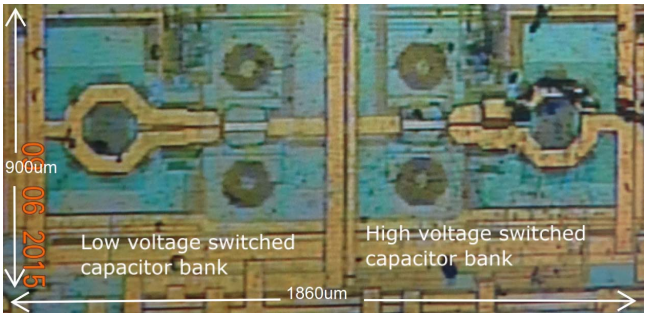

Fig. 10. Die photograph of prototype VCOs.

are used for biasing to avoid bias resistor noise. Additional noise filtering is achieved using a second-harmonic tank at the common source node [2].

A differential center-tapped inductor with an inductance of 216 pH is realized at 13.5 GHz using a parallel stack of the top two thick metal layers available in the process. A floating patterned ground shield is used below the inductor to reduce losses from electrical coupling to the substrate [3]. A switched-capacitor bank with seven coarse-tune bits covers a 1.3-GHz frequency range. The four least significant bits of the switched-capacitor bank are implemented in binary fashion, while the three most significant bits are implemented in thermometric fashion. The fine-tuning varactor is designed for an overall VCO gain K_{VCO} of 35 MHz/V. The second-harmonic noise filter at 27 GHz is achieved by resonating a 57-pH transmission line inductor with a combination of fixed capacitor of 129 fF and parasitic capacitance.

To validate the switched-capacitor noise analysis presented in Section II, two VCOs with high- and low-voltage switched-capacitor banks, but identical otherwise, were designed. On simulation, the VCO with high-voltage switched-capacitor bank exhibited 0.8-dB better phase noise than its counterpart, when all switched-capacitor cells were turned OFF. The simulated phase noise comparison of the two VCOs is plotted in Fig. 9.

IV. Measurement Results

A pair of VCOs, one with a low-voltage switched-capacitor bank and the other with a high-voltage switched-capacitor bank, were fabricated in a 130-nm BiCMOS process, and the die photograph is shown in Fig. 10. Each VCO occupies a die area of approximately

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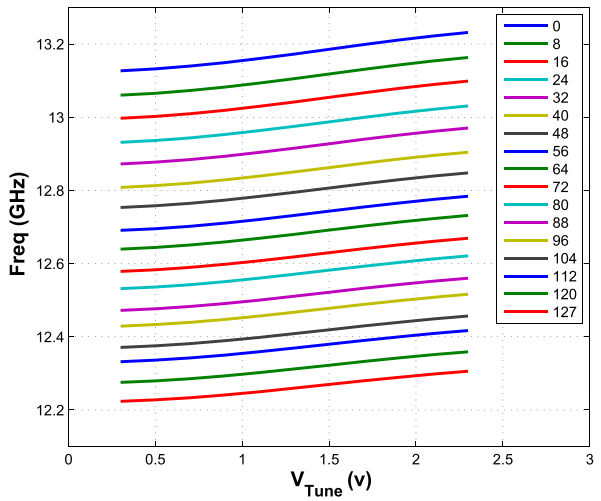

Fig. 11. Measured tuning curve for VCO with high-voltage capacitor bank.

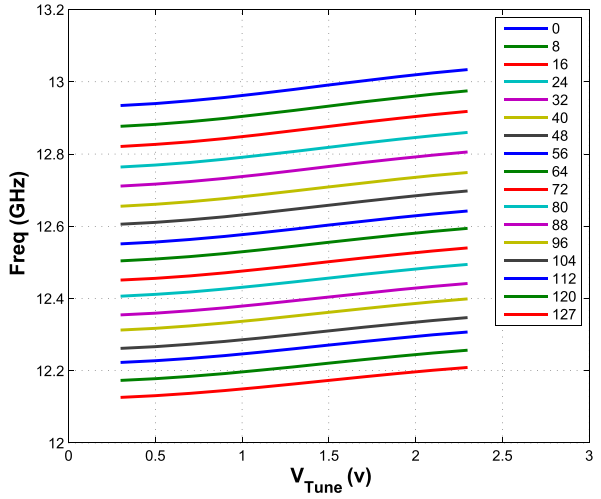

Fig. 12. Measured tuning curve for VCO with low-voltage capacitor bank.

900 μm $\times$ 930 μm. On measurement at room temperature, the VCOs consumed a current of 13 mA from a 1.36-V low dropout regulator supply voltage. The frequency tuning range was approximately 7.3% for both VCOs, as plotted in Figs. 11 and 12.

A Keysight Technologies E5052B 10-MHz to 7-GHz Signal Source Analyzer is used for characterizing VCO phase noise and frequency measurement, through an on-chip divide-by-2 circuit. The measured phase noise of the two VCOs with all switched-capacitor cells in OFF-state, normalized to the same frequency of 12.67 GHz (center frequency of the VCO with high-voltage switched-capacitor bank) and averaged 16 times, is compared in Fig. 13. As expected, the VCO with high-voltage switched-capacitor bank performs around 1 dB better than the low-voltage counterpart at large frequency offsets. This improvement is similar to what was predicted from simulations and has been further confirmed through measurement on multiple device samples to ensure that the improvement is not due to measurement variations. The measured phase noise was found to be higher than expected, which can be traced to two sources: 1) detuning of the second-harmonic tank and 2) lower inductor quality factor than expected, leading to lower output swing. A major portion of the phase noise discrepancy can be replicated in simulation.

It may be seen from Figs. 9 and 13 that the VCO with low-voltage switched-capacitor bank has better phase noise performance

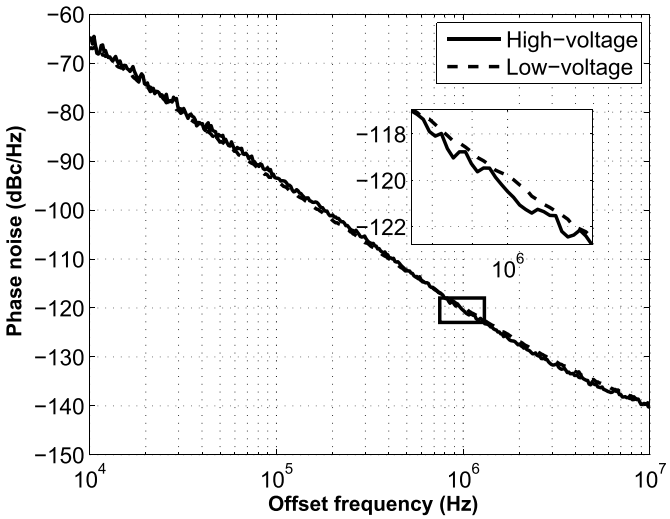

Fig. 13. Measured phase noise of the two VCOs, normalized to 12.67 GHz.

TABLE I
VCO PERFORMANCE COMPARISON

Ref	[4]	[5]	[6]	This work
Process	BiCMOS 180 nm	BiCMOS 180 nm	SiGe:C BiCMOS 250 nm	BiCMOS 130 nm
Freq (GHz)	12.64	13.725	12.74	12.67
VDD (V)	0.7	0.9	3.7	1.36
Idc (mA)	6.15	4.5	25	13
PN @ 1MHz	-117.4	-113.8	-123	-120.6
FTR (%)	3.3	6	5.1	7.34
FOM[a]	193.1	190.2	183	190
FOMT[b]	183.5	185.8	177.2	187.3

[a] $\text{FOM} = 20\cdot\log\left(\frac{f_0}{\Delta f}\right) - PN@\Delta f(dBc/Hz) - 10\cdot\log\left(\frac{P_{DC}}{1mW}\right)$

[b] $\text{FOMT} = \text{FOM} + 20\cdot\log\left(\frac{FTR}{10}\right)$

at smaller offsets. The analysis of Section II is valid not only for thermal noise but also for flicker noise too. It should be noted that all parameters have been kept the same in the two VCOs, including cross-coupled device sizes and the quality factor of the LC tanks, with the only difference being the type of device in the switched-capacitor bank. Moreover, the phase noise has been measured with all switches in the capacitor bank turned OFF. Therefore, the only source of difference in flicker noise is transistors M_{B1} and M_{B2} in Fig. 1. These devices were also chosen to be thin- and thick-oxide devices in the two respective VCOs for reliability reasons. Since flicker noise is known to be dependent on the type of device and process, this is the only possible source for the difference in close-in phase noise.

Table I compares the performance of the VCO with high-voltage switched-capacitor bank in this brief with other Ku-band VCOs reported recently in the literature, showing very competitive performance across several metrics.

V. CONCLUSION

A detailed analysis of phase noise due to VCO switched-capacitor bank was presented in this brief. An optimum capacitor bank design was proposed and validated with a Ku-band VCO implemented in a 130-nm BiCMOS technology. The prototype design covers a 12.2–13.1-GHz frequency range and achieves a phase noise of -120.6 dBc/Hz at 1-MHz offset when running at 12.67 GHz. The VCO core consumes a power of 17.7 mW and attains a figure of merit of 190.

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