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Design of Area-Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications

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***Abstract*— In this brief, based on upset physical mechanism together with reasonable transistor size, a robust 10T memory cell is first proposed to enhance the reliability level in aerospace radiation environment, while keeping the main advantages of small area, low power, and high stability. Using Taiwan Semiconductor Manufacturing Company 65-nm CMOS commercial standard process, simulations performed in Cadence Spectre demonstrate the ability of the proposed radiation-hardened-by-design 10T cell to tolerate both 0 → 1 and 1 → 0 single node upsets, with the increased read/write access time.**

***Index Terms*— Access time, aerospace radiation, memory, reliability.**

I. Introduction

SRAMs have been widely adopted in various aerospace electronic systems, and play a major role in the delay, area, power, and critical reliability [1]. In aerospace applications, SRAMs have a key constrain that makes a challenge in the reliability induced by energetic particles. Therefore, single event upsets (SEUs) are a major reliability failure mechanism that can cause a malfunctioning of an electronic system by altering the stored value temporarily [2]. When the charged particle hits a sensitive node of an integrated circuit, the induced charge along its path can be efficiently collected and accumulated through drift processes. Once a transient voltage pulse generated by the accumulated charge is above the switching threshold of the circuit, the stored value in this sensitive node will be changed [4]. However, it is the fact that the SRAM cell (i.e., 6T) is usually built using two cross-coupled inverters, and the changed value in a stored node can also trigger the positive feedback mechanism to flip the state in another sensitive node so that an error occurs in the memory. Because these corrupted data can be fully recovered by overwriting operations, such a phenomenon is also reported as the soft error [3], [4].

Generally, with CMOS process technology scaling, SRAM cells are more vulnerable to this reliability challenge because of increasing densities, decreasing critical charge, and reducing supply voltage [1]. Hence, soft error robustness with radiation-hardened-by-design (RHBD) techniques is an increasingly important prerequisite in aerospace applications due to the above reasons and more complex cosmic radiation environment, and proposing a novel area-efficient and high-reliability RHBD memory cell is needed [5], [6].

Recently, several remarkable RHBD cell studies have been reported based on circuit-level redundancy or redesigning a memory cell for providing radiation fault-tolerate capability. For example, Jung *et al.* [7] have presented two RHBD memory cells (PS-10T and NS-10T memory cells) by using a stacked structure. However, due to the defect of design, these memory cells can provide only partial SEU robustness, i.e., NS-10T cell can only recover 0 → 1 SEU instead of 1 → 0 SEU. In contrast, PS-10T cell has the capability of tolerating 1 → 0 SEU, and for 0 → 1 SEU, it is incapable of action. Jahinuzzaman *et al.* [8] have proposed an RHBD Quatro-10T memory cell to reduce only 1 → 0 SEU by relying on a negative feedback. In [9], an RHBD 11T memory cell is reported, which remains the stored value by blocking the feedback path to prevent the induced transient pulse affecting the next nodes. However, for this RHBD 11T memory cell, due to the single-ended structure, the differential write and read capabilities are not enabled, which can increase its operation time. In [10], a DICE memory cell is proposed using 12 transistors, which makes use of two interlocked latch pairs to store the complementary values so that an affected value can be recovered to its original value using the positive feedback. In [11], by redesigning a cell structure and using a shallow trench isolation technique, an RHBD 12T memory cell is proposed at the cost of large area overhead. However, the common drawback of 11T, DICE, and 12T cells is that their area overheads are larger. Hence, all of the above RHBD cells are not suitable for aerospace applications in which RHBD memory cells with both area-efficient and high-reliability properties are required in order to offer appropriate design-for-reliability systems.

In order to solve this contradiction, a novel area-efficient, low-power, and high-reliability RHBD 10T memory cell is proposed using a circuit-level hardening technique. According to SEU physical theory together with reasonable transistor size, it can provide high radiation hardening capability at the cost of write and read access times.

Intuitively, this brief is mainly organized as follows. Section II describes the schematic of the proposed RHBD 10T memory cell, and provides the analysis of its timing and fault-tolerate recovery.

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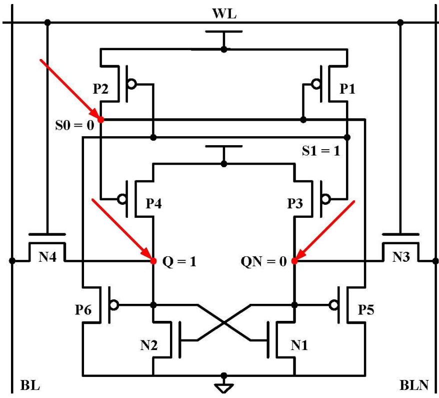

Fig. 1. Schematic of the proposed RHBD 10T memory cell.

In Section III, fault injections are executed, and the detailed comparisons in terms of layout area, power, write/read time, and static noise margins (SNMs) for the above memory cells are given. Finally, the conclusion is provided in Section IV.

II. Proposed Hardened 10T Memory Design

A. Schematic and Normal Operation Analysis

For the proposed RHBD 10T memory cell, Fig. 1 describes its basic schematic structure. From this figure, it can be seen that the proposed RHBD memory cell consists of ten transistors in which PMOS transistors are transistors P1 $\sim$ P6, and the remaining transistors (N1 $\sim$ N4) are NMOS transistors. Both NMOS transistors N4 and N3 are defined as the access transistors, and their gates are connected with a wordline (WL). Hence, when this WL is in high mode (WL = 1), two access transistors are turned ON. At the moment, write/read operation can be implemented. The stored nodes are nodes Q, QN, S1, and S0 in which these four nodes are responsible for keeping the stored value correctly. In order to quickly transmit the digital signal to the output port during a read operation, a differential sense amplifier has to be employed and connected with two bit lines BL and BLN.

Assuming that the stored value of the proposed RHBD 10T memory cell is 1 in digital logic, i.e., $Q = 1$, QN = 0, $S1 = 1$, and $S0 = 0$, as shown in Fig. 1. It is easily concluded that the proposed RHBD 10T memory cell is steadily maintaining the stored value when WL is driven by a low voltage (WL = 0). Before normal read operation, due to precharge circuitry, the voltages of the bit lines BL and BLN will be raised to 1 in digital logic. In read operation, WL is in high mode (WL = 1), and then two access transistors N3 and N4 are turned ON immediately. Nodes Q, QN, S1, and S0 are keeping the stored value, and the voltage of bitline BL is also unchanged. However, the voltage of bitline BLN is decreased due to the discharge operation through ON transistors N1 and N3. Once the voltage difference of bitlines is a constant value which has been confirmed in the differential sense amplifier connecting with two bitlines, the stored digital signal in memory cell will be output as soon as possible. The purpose of write operation is to change the stored logical value correctly. Therefore, before write operation, due to the write circuitry, the voltages of bitline BL will be 0 in digital logic. Contrary to the voltage of bitline BL, the voltage of bitline BLN will be 1. When the voltage of WL is supply voltage VDD (WL = 1), write operation is executed. Transistors N2, P2, P3, and P6 are turned ON. At the moment, the states of transistors N1, P1, P4, and P5 will be OFF, so that the logical value of this memory cell is rightly changed to 0. Therefore, write operation can also be completed successfully.

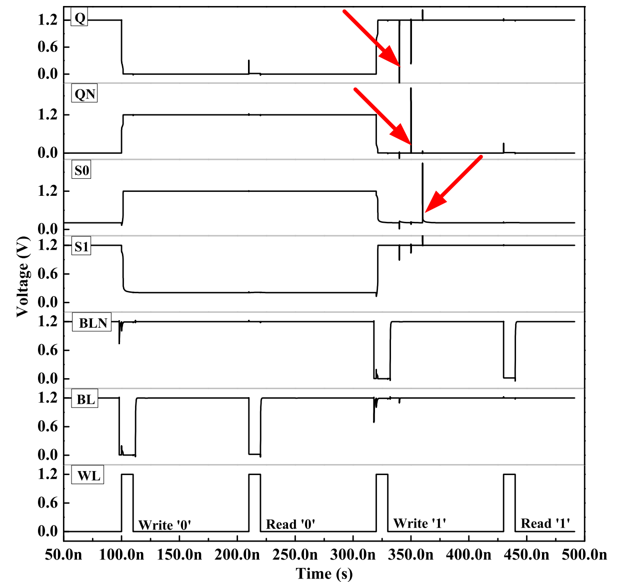

Fig. 2. Timing and SEU simulation verification.

The timing simulation of the proposed RHBD 10T cell has been obtained in Cadence Spectre with models derived from Taiwan Semiconductor Manufacturing Company (TSMC) CMOS 65-nm technology, as shown in Fig. 2. From this figure, we can see that a “write 0, read 0, write 1, and read 1” timing simulation result is successfully completed. Therefore, the proposed RHBD 10T memory cell can rightly achieve its timing operation.

B. SEU Recovery Analysis

Let us consider the stored 1 state again, as shown in Fig. 1. For the RHBD 10T memory cell, according to SEU physical mechanism, nodes Q, QN, and S0 are three sensitive nodes for this stored value.

1) If the sensitive node Q is flipped to state 0 by a charged particle, transistor N1 will be temporarily OFF, and the switch state of transistor P6 will be ON temporarily. However, the voltage of node S1 will be its initial state, because the size of transistor P1 is larger than that of transistor P6 (2.1× larger). As a result, the voltage of node S0 is unchanged. Hence, transistor P4 will be always ON. Finally, the voltage of node Q will be flipped to the initial voltage.
2) If the sensitive node S0 is induced to change the initial state by a radiation particle, both transistors P1 and P4 will be temporarily turned OFF, and the nodes Q, QN, and S1 will be unchanged due to capacitive effect. Therefore, transistor P5 will be always ON, and the voltage of node S0 will be restored.
3) When node QN is flipped, the switch states of transistors N2 and P5 will be temporarily turned ON and OFF, respectively, and then the voltage of node Q will be changed to 0 state. Hence, transistors P6 and N1 will be also temporarily turned ON and OFF, respectively. However, due to the larger size of transistor P1, the value of node S1 will be its initial value so that transistor P2 also remains its OFF state. Therefore, the affected node Q will be pulled up to 1 state, and then transistor N1 will be turned ON again, and node QN will be pulled down to 0 state.

III. Results

A. SEU Tolerance Verification

The proposed RHBD 10T memory cell has been simulated in Cadence Spectre for fault injections. In order to mimic the single event, we take advantage of the double-exponential current source

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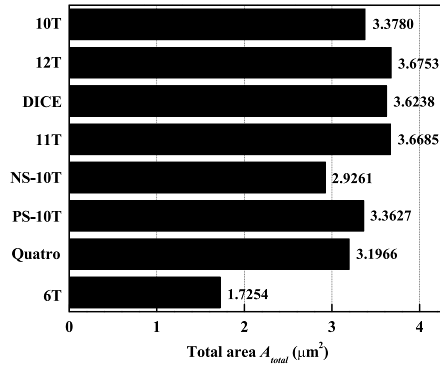

Fig. 3. Area comparison result among different memory cells.

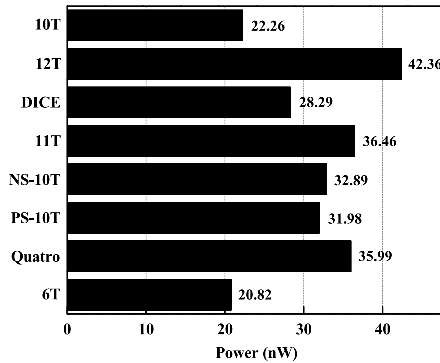

Fig. 4. Power comparison result among different memory cells.

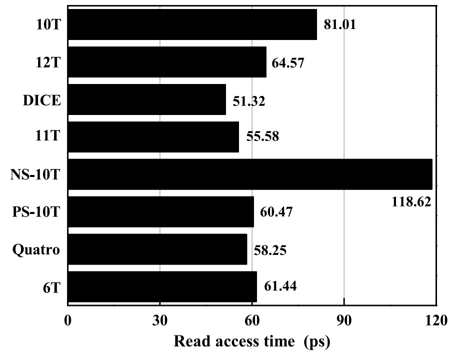

Fig. 5. Read access time comparison result among different memory cells.

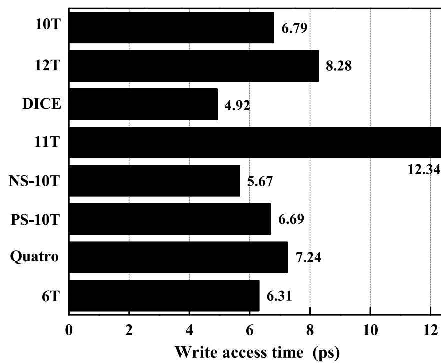

Fig. 6. Write access time comparison result among different memory cells.

to approximately simulate radiation effects in a semiconductor device [9]. Simulation results of nodes Q, QN, and S0 are shown in Fig. 2, and SEU fault injections are at 340, 350, and 360 ns, respectively. From this figure, it is easily demonstrated that the proposed RHBD 10T cell can provide full SEU tolerance in a single node (supply VDD = 1.2 V, typical process corner, and at the room temperature 25 °C). In other words, its tolerance capability is the same as with 11T, DICE, and 12T cells, which can recover a $1 \rightarrow 0$ SEU but also $0 \rightarrow 1$ SEU in any one node, as discussed above.

B. Cost Comparison

The area comparison result of these memory cells is shown in Fig. 3. This figure provides proofs that the area of our RHBD 10T memory cell is 91.91%, 93.21%, 92.08%, 115.44%, 100.45%, 105.67%, and 195.78% of cells 12T, DICE, 11T, NS-10T, PS-10T, Quatro, and 6T, respectively. However, some hardened memory cells, such as PS-10T and Quatro, can tolerate only $0 \rightarrow 1$ or $1 \rightarrow 0$ SEU so that they cannot provide enough fault-tolerate capability. For the 11T memory cell, due to its single-ended structure, it has no differential read and write properties. Moreover, it also needs more extra refreshing and write select signals to maintain a minimum level of functionality for tolerating an SEU so that its peripheral circuits are larger [9].

Fig. 4 shows the power dissipation comparison result for different memory cells, and it also provides proofs that our RHBD 10T memory cell has the smallest power dissipation among various radiation hardened memory cells. Compared with 12T, DICE, 11T, NS-10T, PS-10T, and Quatro cells, due to using more PMOS transistors [12], the power dissipation of the proposed RHBD 10T memory cell can reduce 47.5%, 21.3%, 38.9%, 32.3%, 30.4%, and 38.1%, respectively.

For these memory cells, Figs. 5 and 6 have compared their read and write access times, respectively. It can be shown that our RHBD 10T cell requires more time for completing read operation compared with cells 12T, DICE, 11T, PS-10T, Quatro, and 6T. This is because two PMOS transistors P5 and P6 introduce the loss of threshold voltage, so that the driving voltages in two redundant nodes S0 and S1 are decreased. As a result, its read access time is increased compared with other memory cells except NS-10T cell. For our RHBD 10T cell, its write access time is 82% and 55% of 12T and 11T cells, respectively. Compared with Quatro cell, the proposed RHBD 10T memory cell has smaller write access time due to the decreased driving capabilities. Compared with other memory cells, because of without differential read and write capabilities, an RHBD 11T memory cell has larger access times, which is determined by its single-ended structure [9].

C. Comparison of Static Noise Margin

Generally, SNMs are expressed in terms of immunity to noise in memory read, write, and hold operations [8], [13]–[16]. Hence, SNMs are also investigated and calculated analytically. The measurement results of SNMs for different memory cells have been shown in Fig. 7. From Fig. 7(a), it can be seen that the read SNM (RSNM) value of our RHBD 10T memory cell is higher than the one of 6T, DICE, Quatro, and PS-10T cells, which indicates that the proposed RHBD 10T memory cell has better read stability. In addition, Fig. 7(b) shows that our RHBD 10T memory cell has a higher write SNM (WSNM) value than the Quatro cell. The hold SNM (HSNM) comparison result in Fig. 7(c) demonstrates that the HSNM value of the proposed RHBD 10T cell is higher compared with other cells due to its longer feedback path and the larger size of transistors P1 and P2.

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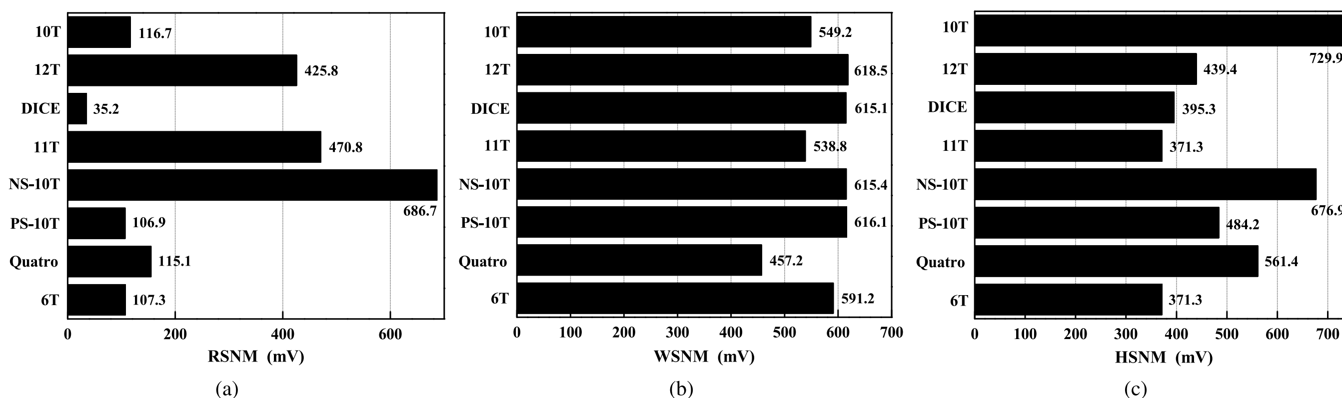

Fig. 7. SNM comparison. (a) RSNM. (b) WSNM. (c) HSNM.

IV. Conclusion

A novel RHBD 10T cell in TSMC 65-nm CMOS process is proposed in this brief. Compared with previous hardened 10T memory cell, the proposed cell can recover an error in any one sensitive node. The simulation results present that the penalty introduced for the proposed 10T cell is the increased write/read access time that may affect its applications with high-speed requirements. However, when considering the constraints of the target applications, compared with other hardened memory cells, the proposed RHBD 10T cell can be regarded as a good choice for aerospace applications as it provides a good balance among performance, area, power, and reliability for memories working at radiation environment.

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