# A New Single-Phase Switched-Coupled-Inductor DC-AC Inverter for Photovoltaic Systems

Kisu Kim, Honnyong Cha, *Member, IEEE,* and Heung-Geun Kim, *Senior Member, IEEE,*

***Abstract*— This paper presents a new single-phase switched-coupled-inductor DC-AC inverter featuring higher voltage gain than the existing single-phase qZ-source and semi-Z-source inverters. Similar to the single-phase qZ-source and semi-Z-source inverters, the proposed inverter also has common grounds between the DC input and AC output voltages, which is beneficial especially for photovoltaic inverter systems. The inverter volume and maximum current flowing can be reduced significantly through the coupling of all inductors. A theoretical analysis of the proposed inverter is described and a 280-W experimental prototype is built to verify the performance of the inverter.**

***Index Terms*— Common ground, dc-ac inverter, high voltage gain, qZ-source inverter, single-phase inverter, switched-coupled-inductor, Z-source inverter.**

## I. INTRODUCTION

Nowadays, there is an increasing demand for low cost single-phase dc-ac inverters in many applications such as photovoltaic (PV), fuel cell, and battery powered systems. The conventional methods are shown in Fig. 1. Fig. 1(a) shows the well-known full-bridge (FB) inverter referred to as buck inverter in this paper [1]–[3]. In this circuit, the inverter output voltage ( $v_o$ ) cannot be greater than input voltage ( $V_{in}$ ). When the input voltage is low, a boost dc-dc converter is inserted between $V_{in}$ and the inverter bridge as shown in Fig. 1(b). However, the two topologies in Fig. 1 have different input and output grounds. This may result in large leakage current in applications such as transformer-less grid-tied PV inverter, which will cause safety and electromagnetic interference problem [4]–[7].

In order to overcome the disadvantages of the conventional inverters, a large number of single-stage inverters are proposed [8], [9]. In addition, the Z-source inverter topologies overcome the limitations mentioned above [10]–[16].

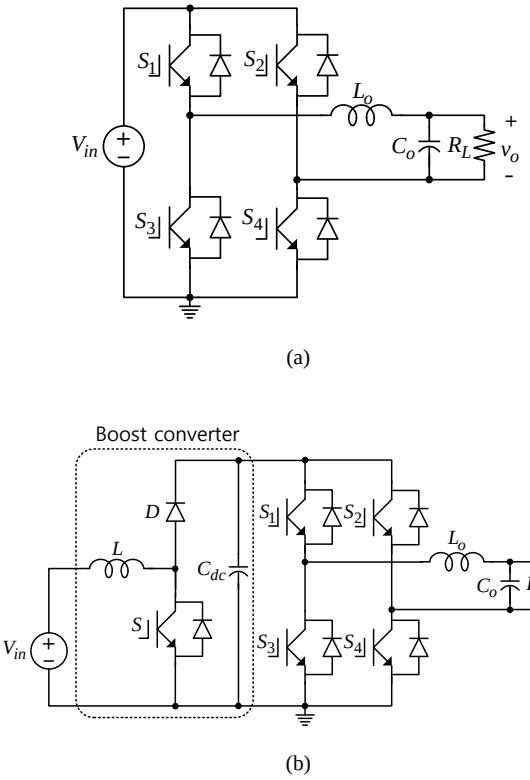


Fig. 1. Conventional single-phase inverters. (a) FB inverter. (b) FB inverter with dc-dc boost converter.

Fig. 2(a) shows the current-fed (CF) single-phase qZ-source inverter [14], and Fig. 2(b) is the semi-qZ-source inverter [15], which is an improved version of Fig. 2(a). Both the inverters have the same voltage gain as shown below and require only two active switches to obtain the same maximum voltage gain as the FB inverter shown in Fig. 1(a)

$$\frac{v_o}{V_{in}} = \frac{2D-1}{D} \tag{1}$$

In (1), D is defined as the duty ratio of switch $S_2$.

As shown in Fig. 2, the two topologies share common grounds between $V_{in}$ and $v_o$, thus they can minimize the possible ground leakage current problem effectively [7] when they are used for PV inverter. However, as depicted in Fig. 2(c), their attainable maximum voltage gain is limited to 1, which means that they are not suitable for applications where input voltage is low.

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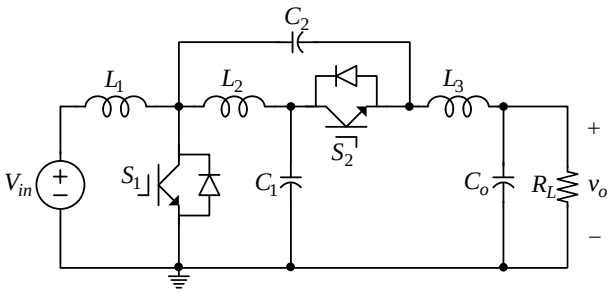
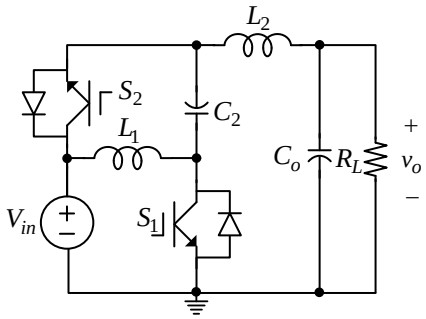



(a)

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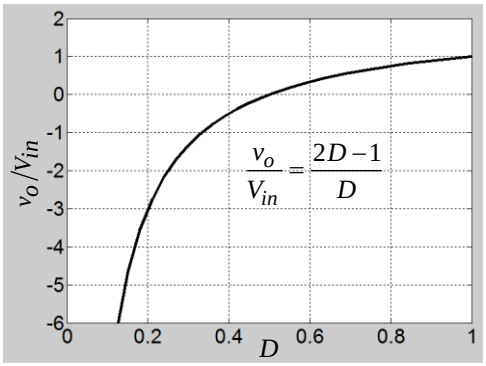


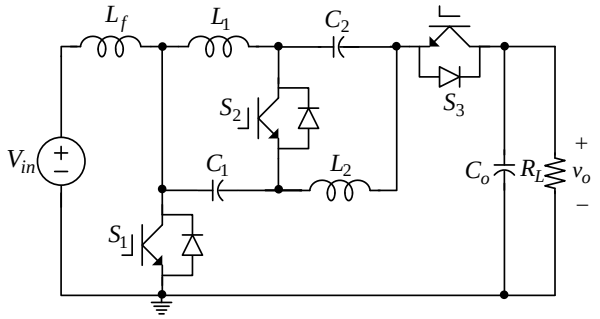

(c)

Fig. 2. Single-phase qZ-source inverters. (a) Single-phase CF-qZ-source inverter. (b) Semi-qZ-source inverter. (c) Voltage gain.

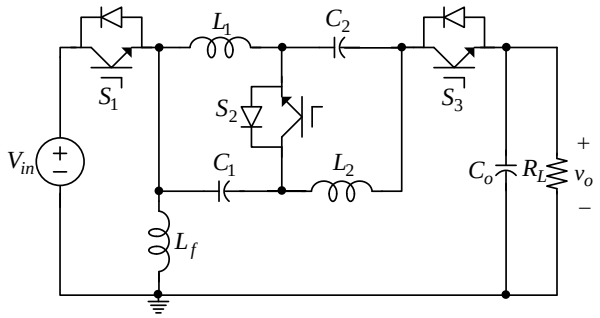
In order to overcome the limitations of Fig. 2 while maintaining the doubly ground features, a three-switch three-state single-phase Z-source inverter (TSTS-ZSI) was introduced in [17]. Fig. 3 shows the boost-based TSTS-ZSI and buck-boost-based TSTS-ZSI, respectively. The inverters can have higher voltage gain than 1, and they comprise three switches, three capacitors, and three inductors.

Although higher voltage gain is obtained, the three inductors ( $L_1$ , $L_2$ and $L_3$ ) in the TSTS-ZSI make the circuit a bit bulky and heavy. In addition, the switch signals of the inverter are all different and relatively complicated.

In this paper, a single-phase switched-coupled-inductor (SCL) dc-ac inverter is proposed. Similar to the TSTS-ZSIs, the proposed inverter can obtain higher voltage gain than the circuits in Fig. 2 and maintains same ground between $V_{in}$ and $v_o$. The proposed inverter also requires three active switches, but all the inductors in the circuit can be coupled together,




(a)




(b)

Fig. 3. Three-switch three-state single-phase Z-source inverter [17]. (a) Boost-based TSTS-ZSI. (b) Buck-boost-based TSTS-ZSI.

which will leads to more compact and cost effective solution than the TSTS-ZSI. In addition, the switch signal generation is relatively simpler than the TSTS-ZSI. A 280 W prototype inverter is built and its performances are verified through experiment.

## II. Operation Principle of the Proposed DC-AC Inverter

Fig. 4 shows the proposed inverter and it takes similar structure with the single-phase CF-qZ-inverter shown in Fig. 2(a). Compared with Fig. 2(a), the proposed inverter has an additional switch ( $S_x$ ), capacitor ( $C_x$ ), and inductor ( $L_2$ ) coupled with inductor $L_1$ [18]–[19].

The inductors $L_1$ and $L_2$ are coupled with $1:n$ turns ratio and all the inductors in the proposed topology can be coupled altogether as will be discussed in Section III. The added $1:n$ coupled inductor contributes to the increase of voltage gain [16], [21]. Although the leakage inductance of the coupled inductor may induce a voltage spike across switch $S_1$, this is not a major problem because such a voltage spike and the voltage of $S_1$ are low. In section III, it will be found that the voltage stress of $S_1$ is always half of $S_2$ or $S_x$ if leakage inductance is not considered. Therefore, as long as the voltage overshoot caused by the leakage inductance is not so high, the voltage stress of $S_1$ will be less than that of $S_2$ and there is not much problem in selecting switching device for $S_1$. On the other hand, the leakage inductance is beneficial in limiting the current passing through $C_x$. Switches $S_1$ and $S_2$ are complementary as in the

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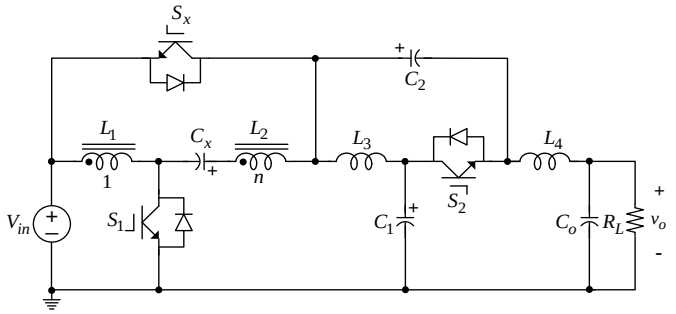



Fig. 4. Proposed dc-ac inverter.

single-phase qZ-source inverter and the switch $S_x$ is synchronized with $S_1$.

### A. *Mode Analysis of the Proposed Inverter*

Fig. 5 shows operation of the proposed inverter and there are two operational modes during one switching cycle. In mode 1, switches $S_1$ and $S_x$ are turned-on, and $S_2$ is turned-off. In mode 2, switches $S_1$ and $S_x$ are turned-off, and $S_2$ is turned-on. Followings are the detailed mode analysis of the proposed inverter.

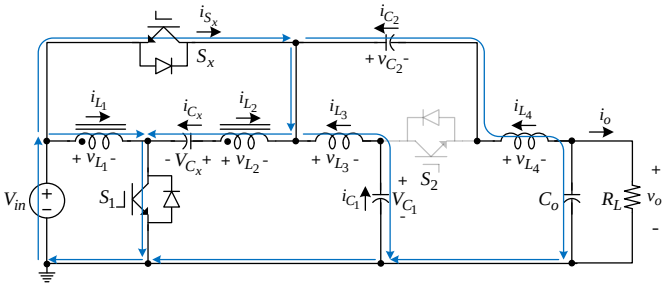
In mode 1, the capacitor $C_x$ is charged to $(n+1)V_{in}$. Since the $C_x$ is being charged and discharged during one switching period, its voltage has ripple and the ripple voltage depends on the output power [18]–[20]. Therefore, when the voltage difference between $(n+1)V_{in}$ and $C_x$ is high, relatively high surge (charging) current will flow through $V_{in}$ - $D_x(S_x)$ - $L_2$ - $C_x$ - $S_1$ and the switching devices in this path ( $S_x$ and $S_1$ ) can be damaged. In order to limit the high surge current, a current limiting inductor is necessary. In this paper, the leakage inductance generated by the coupling of $L_1$ and $L_2$ serves as the current limiting inductor. From Fig. 5(a), the voltage and current relations in mode 1 are derived as

$$V_{C_x} = V_{in} + v_{L_2} = (n+1)V_{in} \tag{2}$$

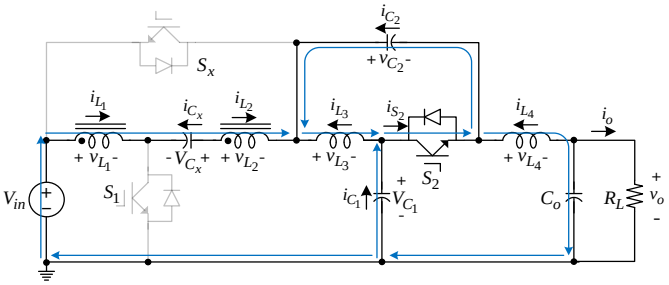
$$\begin{cases} v_{L_1} = V_{in} \\ v_{L_3} = V_{in} - V_{C_1} \\ v_{L_4} = V_{in} - v_{C_2} - v_o \end{cases} \tag{3}$$

$$\begin{cases} i_{C_1} = i_{L_3} \\ i_{C_2} = i_{L_4} \\ i_{C_x} = i_{in} - i_{L_1} + i_{L_3} + i_{L_4} \end{cases} \tag{4}$$

In mode 2, capacitor $C_x$ is discharged by the inductor current, $i_{L_1}$. From Fig. 5(b), the voltage and current relations in mode 2 are derived as




(a)




(b)

Fig. 5. Mode analysis of the proposed inverter. (a) Mode 1 : $S_1$ and $S_X$ are ON, and $S_2$ is OFF. (b) Mode 2 : $S_1$ and $S_x$ are OFF, and $S_2$ is ON.

$$\begin{cases} (1+n)v_{L_1} = V_{in} + V_{C_x} - v_{C_2} - V_{C_1} \\ v_{L_3} = v_{C_2} \\ v_{L_4} = V_{C_1} - v_o \end{cases} \tag{5}$$

$$\begin{cases} i_{C_1} = -i_{L_1} - i_{L_4} \\ i_{C_2} = -i_{L_1} - i_{L_3} \\ i_{C_x} = -i_{\mathrm{L}_1} \end{cases} \tag{6}$$

From the above equations, voltage relations are derived as

$$V_{C_1} = v_{C_2} + v_o \tag{7}$$

$$V_{C_1} = (n+2)V_{in} \tag{8}$$

From the flux (volt-second) balance condition on $L_3$, the capacitor $C_2$ voltage is derived as

$$v_{C_2} = \frac{(1-D)(n+1)}{D} V_{in} \tag{9}$$

where $D$ is the duty cycle of switch $S_2$.

By using (7)–(9), the voltage gain of the proposed inverter is derived as

$$\frac{v_o}{V_{in}} = \frac{(2n+3)(2D-1)+1}{2D} \le n+2 \tag{10}$$

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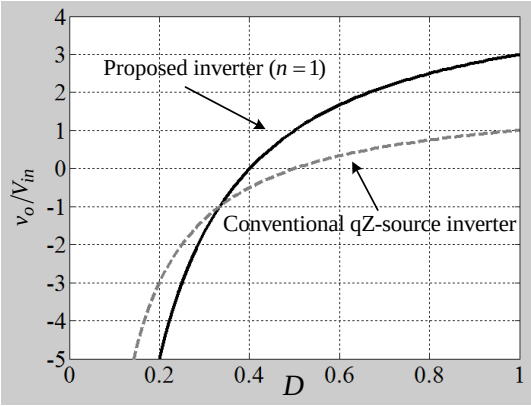


Fig. 6. Voltage gain comparison.

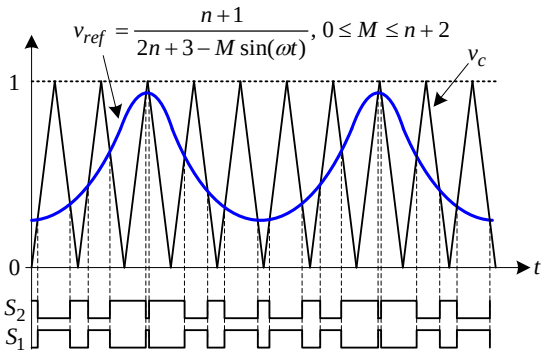


Fig. 7. Gate signal generation of the proposed inverter.

Fig. 6 shows the voltage gain of the proposed inverter when $n=1$ and compared with the conventional inverters shown in Fig. 2. It is found that the proposed inverter has a higher voltage gain than the conventional inverters shown in Figs. 1(a) and 2.

According to the charge balance condition on $C_x$, $C_1$, and $C_2$, the inductor currents averaged in one switching period are derived as

$$i_{L_{1.avg}} = \frac{(2D-1)(n+1)}{D} i_o \tag{11}$$

$$i_{L_{2.avg}} = 0 \tag{12}$$

$$i_{L_{3.avg}} = i_{L_{4.avg}} = -i_o \tag{13}$$

$$i_{S_{2.avg}} = i_{S_{x.avg}} = i_o \tag{14}$$

Currents of inductors $L_1$ and $L_2$ are different in respective mode unlike inductor currents $i_{L_3}$ and $i_{L_4}$. In mode 1, where current ripple is ignored, they are derived:

$$i_{L_1} = \frac{(2D-1)(n+1-D)}{D(1-D)} i_o \tag{15}$$

$$i_{L_2} = -\frac{(2D-1)}{(1-D)} i_o \tag{16}$$

In mode 2, they are expressed as

$$i_{L_1} = i_{L_2} = \frac{2D-1}{D} i_o \tag{17}$$

## B. Modulation Scheme of the Proposed Inverter

Modulation scheme of the proposed inverter is the same as that of the single-phase qZ-source inverter. By defining the output voltage of the inverter as (18), modulation index (M) of the inverter is derived as

$$v_o = V_m \sin \omega t \tag{18}$$

$$M = \frac{V_m}{V_{in}} \tag{19}$$

By substituting (18) and (19) into (10), the following duty cycle equation is derived as

$$D = \frac{n+1}{2n+3-M\sin(\omega t)}, \ (0 \le M \le n+2) \tag{20}$$

When $n=1$ and $M=3$, the duty cycle range of the proposed inverter is 0.25 to 1.0. Fig. 7 represents the gate signal generation of the proposed inverter. When reference signal ($v_{ref}$) is greater than the carrier signal ($v_c$), switch $S_2$ is turned on and switch $S_1$ is turned off.

# III. Magnetic Integration of Inductors and Comparison

## A. Magnetic Integration of Inductors

As discussed in Section II, the $L_1$ and $L_2$ are coupled with $1:n$ ratio to obtain higher voltage gain. In this Section, it is revealed that all the four inductors ($L_1$, $L_2$, $L_3$, and $L_4$) in the proposed inverter can be coupled using one magnetic core.

The previous analysis shows that the voltages across each inductor during mode 1 are as follows

$$\begin{cases} v_{L_1} = V_{in} \\ v_{L_2} = nV_{in} \\ v_{L_3} = V_{in} - V_{C_1} = -(n+1)V_{in} \\ v_{L_4} = V_{in} - v_{C_2} - v_o = -(n+1)V_{in} \end{cases} \tag{21}$$

Similarly, the voltages across each inductor during mode 2 are as follows

$$\begin{cases} v_{L_1} = \frac{1}{n+1}(V_{in} + V_{C_x} - V_{C_1} - v_{C_2}) = -\frac{1}{n+1} v_{C_2} \\ v_{L_2} = -\frac{n}{n+1} v_{C_2} \\ v_{L_3} = v_{C_2} \\ v_{L_4} = V_{C_1} - v_o = v_{C_2} \end{cases} \tag{22}$$

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TABLE I
DEVICE STRESS OF THE PROPOSED INVERTER

| | Voltage stress | Current stress |
|---|---|---|
| $S_1$ | $\frac{2n+3+M}{2M}V_o$ | $\frac{(2n+3-M)(M-1)}{n+2-M}I_o$ |
| $S_2$ | $\frac{2n+3+M}{M}V_o$ | $\frac{2n+3+M}{n+1}I_o$ |
| $S_x$ | $\frac{2n+3+M}{M}V_o$ | $\frac{2n+3-M}{n+2-M}I_o$ |

TABLE II
COMPARISON OF INVERTERS

| | | Proposed inverter ( $n=1$ ) | | Boost based TSTS-ZSI ( $k=3$ ) | |
|---|---|---|---|---|---|
| | | Voltage stress | Current stress | Voltage stress | Current stress |
| $S_1$ | | $\frac{5+M}{2M}V_o$ | $\frac{(M-1)(5-M)}{3-M}I_o$ | $\frac{5}{M}V_o$ | $(M+2)I_o$ |
| $S_2$ | | $\frac{5+M}{M}V_o$ | $\frac{5+M}{2}I_o$ | | |
| $S_x$ | | | $\frac{5-M}{3-M}I_o$ | | |
| No. of capacitors | | 4 | | 3 | |
| No. of inductors | | 1 (coupled inductor) | | 3 (discrete inductors) | |
| Current | Input | Quasi-continuous | | Continuous | |
| | Output | Continuous | | Discontinuous | |
| Gate signal generation | | Relatively simple | | Complex | |
| $\Delta i_{L_{\max}}$ | | $\Delta i_{L_1}=\Delta i_{L_2}=\frac{(3+M)(1+M)}{(5+M)^2}\times\frac{V_{in}T_s}{L_1}$, $\Delta i_{L_3}=\Delta i_{L_4}=\frac{4(3+M)}{(5+M)^2}\times\frac{V_{in}T_s}{L_3}$ ( $L_1=L_2$, $L_3=L_4$ ) | | $\Delta i_{L_f}=\frac{4}{5}\times\frac{V_{in}T_s}{L_f}$, $\Delta i_{L_1}=\Delta i_{L_2}=\frac{5}{4}\times\frac{V_{in}T_s}{L_{1,2}}$ ( $L_1=L_2$ ) | |
| $i_{L_{avg}}$ (one switching period) | | $i_{L_{1\_avg}}=I_o(M\sin(\omega t)-1)$, $i_{L_{2\_avg}}=0$, $i_{L_{3\_avg}}=i_{L_{4\_avg}}=-I_o\sin\omega t$ | | $i_{L_{f\_avg}}=I_oM\sin\omega t$, $i_{L_{1\_avg}}=i_{L_{2\_avg}}=I_o\sin\omega t$ | |
| $V_{C_{\max}}$ | | $V_{C_x}=\frac{2}{M}V_o$, $V_{C_1}=\frac{3}{M}V_o$, $V_{C_2}=\frac{3+M}{M}V_o$ | | $V_{C_1}=V_{C_2}=\frac{5+M}{2M}V_o$ | |

From (21) and (22), it is found that regardless of the operating mode the four inductors in the proposed inverter have the following voltage relationships.

$$v_{L_1}:v_{L_2}:v_{L_3}:v_{L_4}=1:n:-(n+1):-(n+1) \tag{23}$$

Therefore, all the inductors can be coupled using one core [22], which leads to significant reduction in magnetic volume and converter size. It should be noted that $n$ is the turns ratio and it is not the real number of turns. Fig. 8 shows the final completed circuit of the proposed inverter with the inductor polarity dots marked. The operation with magnetic integration is the same as that of the previous analysis in Section II.

## *B. Comparison of Switch Stress and Others*

From Fig. 5 and (8), (9), (21), (22), voltage stresses of the three switches can be determined. Similarly, the switch current stresses can be determined from (4), (6), (13)–(17) and Fig. 5. Table I shows maximum switch stress of the proposed inverter. Table II compares the proposed inverter when $n=1$ with the boost based TSTS-ZSI shown in Fig. 3(a). $k$ is maximum of modulation index [17].

Although the buck-boost based TSTS-ZSI has lower device stresses, it has drawbacks like more complicated gate signal generation, discontinuous input and output current, and requires additional LC filter that builds the circuit structure more complex and large inductor [17]. For these reasons, the boost based TSTS-ZSI is compared with the proposed inverter.

From the result of Table II, it is evident that the overall voltage and current stresses of the proposed inverter are greater than those of the TSTS-ZSI and the proposed inverter requires one more capacitor. However, current stress of the proposed

inverter is lower than that of the boost-based TSTS-ZSI when $M$ is lower than 2.4. Moreover, the proposed inverter can reduce the magnetic volume through the coupling of all separate inductors. Comparison of maximum current ripple, average current and maximum capacitor voltage is summarized in Table II. According to the Table II, when compared with the boost-based TSTS-ZSI, the inductor current ripples of the proposed inverter are reduced by more than two due to coupling effect. In Table II, $L_1$ and $L_3$ of the proposed inverter are self-inductances of the coupled inductor. In addition, self-inductances $L_1$ and $L_2$ of the proposed inverter are the same and $L_3$ and $L_4$ are also the same when all inductors are coupled with $n=1$. The boost-based TSTS-ZSI is assumed that $L_1$ and $L_2$ are equal [17]. Although, the $C_2$ capacitor voltage of the proposed inverter is greater than that of the boost-based TSTS-ZSI, the capacitor voltages of $C_x$ and $C_1$ in the proposed converter are lower than those of the boost-based TSTS-ZSI. Moreover, inductor has more influence on size and weight than capacitor. The average inductor currents of the proposed inverter and boost-based TSTZ-ZSI in one switching period are almost the same.

In conclusion, the proposed inverter can reduce overall magnetic volume because lower inductance is required. In addition, the boost-based TSTS-ZSI should have large output capacitor because of discontinuous output current. Moreover, the gate signal generation of the proposed inverter is much simpler than that of the TSTS-ZSI.

## IV. Experimental Results

A 280-W prototype inverter is built and tested. Detailed electrical specifications of the proposed inverter are summarized in Table III.

As already mentioned in Section II, a relatively small current limiting inductor is required in the path $V_{in}$ - $D_x(S_x)$ - $L_2$ - $C_x$ - $S_1$ to limit the high surge current. In the proposed circuit, the leakage inductance (about 300 nH) generated by coupling of $L_1$ and $L_2$ is used for this purpose. Followings are the experimental waveforms of the proposed inverter when $V_{in}$= 62 V, M = 2.5,

TABLE III
Electrical Specifications of the Proposed Inverter

| | | |
|---|---|---|
| Output power | | 280 W |
| Input voltage | | 62 VDC |
| Output voltage | | 110 Vrms / 60 Hz |
| Switching frequency | | 20 kHz |
| IGBT ( $S_x$ , $S_1$, $S_2$ ) | | FGH40N60 |
| Coupled inductor | Core | EE7066 |
| | Inductance ( $L_1$, $L_2$ ) | 60 uH |
| | Inductance ( $L_3$, $L_4$ ) | 240 uH |
| Capacitance ( $C_x$, $C_1$ ) | | 100 uF |
| Capacitance ( $C_o$ ) | | 4.4 uF |

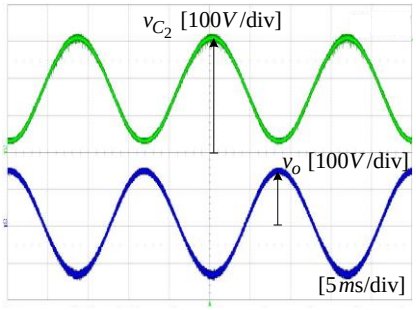



Fig. 9. Experimental waveforms of the proposed inverter. ( $v_{C_2}$ , $v_o$ )

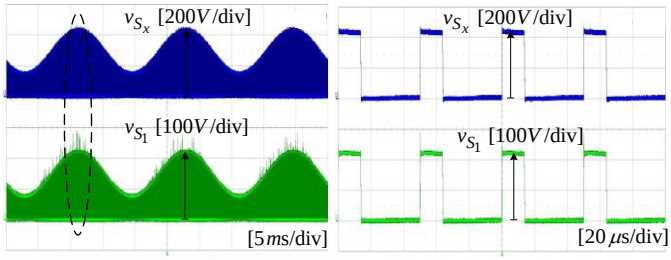



Fig. 10. Experimental waveforms of the proposed inverter ( $v_{S_x}$ , $v_{S_1}$ ). (a) Switching waveform. (b) Zoomed-in waveform of (a).

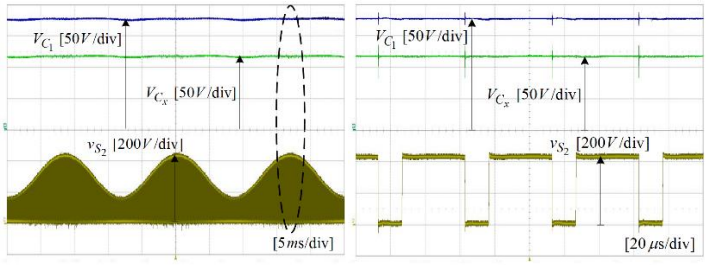



Fig. 11. Experimental waveforms of the proposed inverter ( $v_{S_2}$ , $V_{C_1}$ , $V_{C_x}$ ). (a) Switching waveform. (b) Zoomed-in waveform of (a).

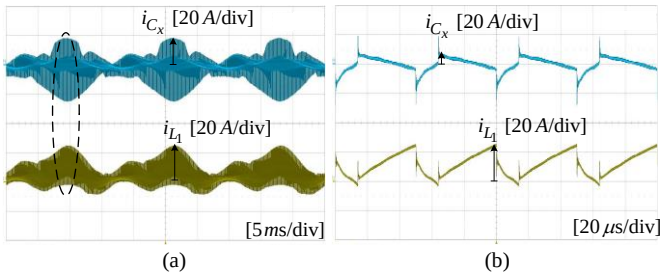
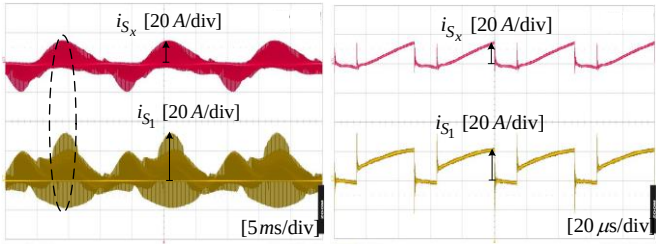



Fig. 12. Experimental waveforms of the proposed inverter. (a) Current waveforms ( $i_{L_1}$ , $i_{C_x}$ ). (b) Zoomed-in waveform of (a).

and $P_o$ = 280 W.

Fig. 9 shows the experimental waveform of the output voltage and the capacitor $C_2$ voltage. Fig. 10 and Fig. 11 show the voltages across all switches ( $v_{S_x}$ , $v_{S_1}$ , and $v_{S_2}$ ). As expected, there is voltage overshoot in switch $S_1$ caused by the leakage inductance and there are no noticeable overshoots in the switches $S_2$ voltage varying with $D$ , the voltages across $C_1$ and $C_x$ are almost constant and they are fixed to $3V_{in}$ and




(a) (b)

Fig. 13. Experimental waveforms of the proposed inverter. (a) Switch current waveforms ( $i_{S_1}$ , $i_{S_2}$ ). (b) Zoomed-in waveform of (a).

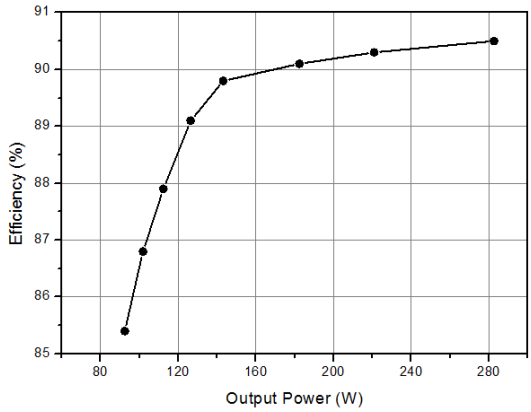



Fig. 14. Efficiency of the proposed inverter.

$2V_{in}$ , respectively. Fig. 12 and Fig. 13 show current waveforms. Fig. 14 shows the efficiency of the proposed inverter tested with $V_{in}$ = 62 V with output power varies.

## V. Conclusions

In this paper, the single-phase switched coupled inductor DC-AC inverter was presented. It has an operation principle similar to that of a single-phase qZ-source inverter. With the addition of components $S_x$ , $C_x$ , and the coupled inductor, voltage gain of the proposed inverter can be extended to greater than 2. The magnetic integration of all inductors decreases the converter volume significantly and the proposed inverter has relatively simple gate signal generation. Moreover, similar to the single-phase qZ-source inverter and the TSTS-ZSI, the proposed inverter shares common grounds between the DC input and the AC output voltage. A 280-W prototype inverter was built and tested to verify operation of the proposed inverter.

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