

Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application

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Abstract—In this paper, a novel radiation-hardened 14-transistor SRAM bitcell with speed and power optimized [radiation-hardened with speed and power optimized (RSP)-14T] for space application is proposed. By circuit- and layout-level optimization design in a 65-nm CMOS technology, the 3-D TCAD mixed-mode simulation results show that the novel structure is provided with increased resilience to single-event upset as well as single-event-multiple-node upsets due to the charge sharing among OFF-transistors. Moreover, the HSPICE simulation results show that the write speed and power consumption of the proposed RSP-14T are improved by ~65% and ~50%, respectively, compared with those of the radiation hardened design (RHD)-12T memory cell.

Index Terms—High speed, low power, radiation-hardened SRAM, single-event-multiple-node upsets (SEMNUs), single-event upset (SEU).

I. INTRODUCTION

SINGLE-event upset (SEU) is a soft-error and nondestructive form of single-event effects (SEEs) [1]. In the radiation environment, when the heavy ion is incident on the semiconductor material, the particles will be ionized. These excess charges will be collected by the sensitive nodes of the device. As a result, a voltage perturbation will appear at those nodes. For SRAM bitcell, when the amplitude of the voltage perturbation is strong enough and exceeds the logic threshold level of the inverter, the data stored might be turned over, as shown in Fig. 1; that is, an SEU is caused.

With the continuous scaling of CMOS technology, the minimum spacing between the transistors is decreased. As a result, multiple transistors are susceptible to the charge deposited from a single particle strike compared to older processes where only one transistor was affected [2]. The charge sharing results in single-event-multiple-node upsets (SEMNUs), which is becoming the main effect of energetic particle strikes in emerging nanometer CMOS technology [3], [4]. In addition, supply

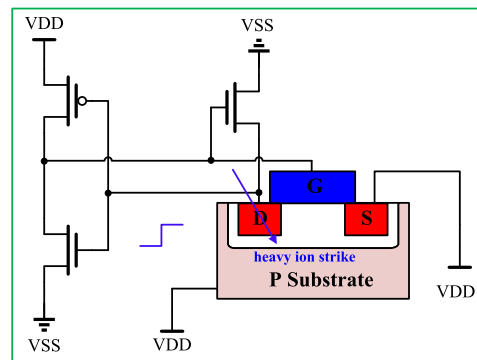


Fig. 1. SEU induced by an ion strike in an SRAM memory.

voltage reduction further increases the susceptibility of circuits to radiation. Thus, the development of radiation-hardened technologies in digital circuits is extremely urgent [5]. Due to the larger sensitive volume per bit and lower node capacitance than the dynamic counterpart, SRAM is more prone to soft errors. Therefore, the soft error rate (SER) [6] in SRAM is increased with the technology scaled in the nanometer regime. In order to reduce the SER, numerous alternatives have been proposed to the standard 6T SRAM cell [7]–[15]. The main reinforcement method is through constructing special topology of transistor connections inside cells to achieve circuit-level protection. The soft error robust Quatro-10T SRAM cell, offering differential read operation with large noise margin was proposed in [7]. However, it can only recover from “1” to “0”; thus, it cannot immune SEU completely. Due to the feedback of the dual node, the dual interlocked storage cell (DICE) [8] can fully immune against single-event transient (SET) occurring on any of its single nodes. However, the very minimum ability of SEMNUs immunity and radiation hardness performance of it has yet to be improved. In [4], based on Schmitt trigger, the Schmitt trigger based (STB)-13T memory cell with fully SEU immune was proposed. However, the limited promotion of SEMNUs immune ability of it is achieved at the expense of writing speed, power consumption, and layout area compared with DICE. Based on the STB-13T, two novel hardened memory cells with more reliability, radiation hardened design (RHD)-11T and RHD-13T, were proposed in [9]. Unfortunately, the writing speed, as well as write margin, of them is deteriorated. In [10], for low power and highly reliable radiation-hardened application, the RH memory (RHM)-12T was proposed; however, the authors used

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nMOS as pull-up devices causing worse read noise margins. Recently, the RHD-12T memory cell with favorable radiation hardness performance, as shown in Fig. 2(a), was proposed in [12]. Besides the toleration for an SEU on any of its internal single nodes, it can also provide the SEMNUs immune to some extent. Unfortunately, the slow write speed as well as large power consumption limits the application of it. In addition to the reinforcement at the circuit level, specific layout techniques as an alternative method for improving the radiation tolerance have also been proposed [13], [14]. As presented in [13], a new layout technique named layout design through error-aware transistor positioning (LEAP) was applied to DICE, resulting in a new sequential element, LEAP-DICE. The TCAD simulations show that it is effective for increasing the linear energy transfer (LET) upset threshold. In order to investigate the charge sharing, a Monte Carlo simulation platform named tool suite for radiation reliability assessment (TIARA) was given in [14]. By analysis of the TIARA simulations results, the layout optimization of the most vulnerable transistor pairs will be targeted.

In this paper, the radiation-hardened with speed and power optimized (RSP)-14T bitcell is proposed. Compared with RHD-12T, its radiation hardness has been improved by the reinforcement of redundant nodes with two extra pMOS transistors. Furthermore, due to the supply of the branch where the redundant nodes located are controlled by the extra PMOSs, during the write operation, the feedback mechanism will be interrupted easily. Thus, the write speed and power consumption have been improved effectively. Generally, SPICE simulations by using the double-exponential current source model are applied for evaluating the radiation tolerance of the circuit, which is time saving. However, the model relies on calibration parameters that are not physical. The charge sharing between transistors will be neglected; it may overestimate the SEU immune ability of other SRAM cells [16]. Thus, in order to consider the charge sharing between transistors as well as reducing the CPU burden, TCAD mixed-mode simulation as a good qualitative approach to value SEU immune is adopted in this paper. Combined with the layout-level design, the simulation results show that the proposed circuit has better SEU immunity.

The rest of this paper is organized as follows. In Section II, operating principles along with the soft-error robustness of our proposed differential 14-transistor SRAM cell are discussed in detail. In Section III, the SEU, as well as SEMNUs, immune ability, and the circuit performance of the proposed RSP-14T are verified and analyzed. Section IV draws the conclusion.

II. PROPOSED RSP-14T SRAM CELL

A. Read and Write Operation

The schematic of the proposed RSP-14T is shown in Fig. 2(b). Here, the transistors N4 and N5, controlled by a word line (WL), are access transistors, which control the connection between the bit lines (BL and BLB) and the storage nodes (Q and QB). The nodes S1 and S0 are redundant nodes of Q and QB. If the stored bit is “1,” the logic values at nodes Q, QB, S1, and S0 are “1,” “0,” “1,” and “0,” respectively.

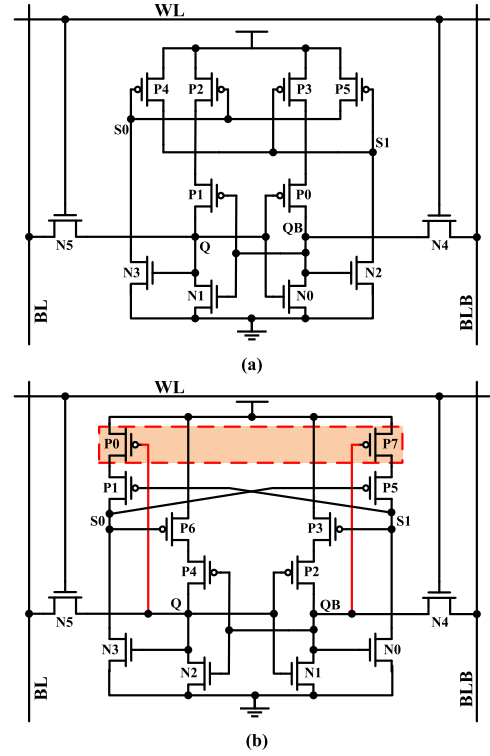


Fig. 2. (a) RHD-12T bitcell. (b) Proposed RSP-14T bitcell.

The functional analysis of the proposed RSP-14T is sequentially presented: 1) write; 2) read; and 3) hold operation. In write operation, we assume that $Q = “1”$ and $QB = “0”$ and the bitlines BL and BLB are set to “0” and “1,” respectively. When the WL is activated, the value stored in Q and QB will be changed to “0” and “1,” respectively. After that, once WL is discharged to “0,” the new state of the memory cell is stored. For a read operation, the BL and BLB are precharged to “1.” When the selected WL is enabled, the transistors N4 and N5 are turned on, BLB will be discharged through transistors N4 and N1. As a result, the differential voltage of the BLs will be generated and amplified by the sense amplifier. During the hold operation, WL is deactivated and the storage nodes are isolated from the BLs; thus, they maintain the initial state. In this paper, the transistors P0 and P7 are used to control the connection or cutoff between the power supply and transistors P1/P5, which is beneficial to improve the write speed and power consumption compared with RHD-12T.

B. Error Tolerance Analysis

Regardless of the charge sharing between the transistors in the actual layout, the analyses of SEU recovery behavior at circuit level are given. Assuming that $Q = “1,”$ $QB = “0,”$ $S1 = “1,”$ and $S0 = “0,”$ respectively, the analyses of the nodes (Q, QB, S1, and S0) are demonstrated as follows.

Case 1 (Positive Transient Pulse at Node S0): When the drain of P1 is hit by a particle, it will collect positive charge and increase the voltage at node S0 (i.e., S0 will be changed from “0” to “1”). As a result, P6 and P5 will be turned off. However, it cannot further affect the OFF/ON-states of other transistors, and the storage status of Q and S1 nodes will

remain unchanged. Therefore, the transient fault at S0 cannot propagate inside the cell. Finally, the nodal logic level will be recovered after the radiation events.

Case 2 (Positive Transient Pulse at Node QB): When the drain of P2 is hit by a particle, it will collect positive charge and increase the voltage at node QB (i.e., QB will be changed from “0” to “1”). As a result, N2 and N0 will be turned on. Correspondingly, Q and S1 will be changed from “1” to “0,” P0 and P1 will be turned on, and N3 will be turned off, and then S0 will be changed from “0” to “1.” Finally, the storage state of the cell will be turned over. (It has been made difficult to change in the layout-level design as presented in Section III.) Due to the transistors being stacked and topology optimized, the parasitic bipolar amplification effect of P2 (the source of P3 is connected with VDD, whereas the source of P2 with weak connection “1”) is mitigated. As a result, the quantity of charge collected by the drain of P2 is reduced, which improves the SEU tolerance of node QB.

Case 3 (Negative Transient Pulse at Node S1): When the drain of N0 is hit by a particle, it will collect negative charge and S1 will be discharged from “1” to “0,” and P3 and P1 will be turned on. However, due to the blocking effect of transistors P2 and P0, the fault at S1 cannot further propagate in the cell. Therefore, QB and S0 will remain in their original status. Due to the low status at QB and S0, P7 and P5 are always at open state. Hence, the current provided by P7 and P5 will charge S1 continuously. This positive feedback will accelerate the recovery process of S1. Finally, the nodal storage status will be recovered after the radiation events.

Case 4 (Negative Transient Pulse at Node Q): When the drain of N2 is hit by a particle, negative charge will be collected and Q will be discharged from “1” to “0,” and then N1 and N3 will be turned off. This is very similar to case 1, thus, the storage status of Q will finally recover after the radiation events.

For time efficiency, in order to prove that the above-mentioned analyses are correct and locate the most vulnerable node of the proposed RSP-14T, the transient injections at S0, QB, S1, and Q nodes are simulated, as shown in Fig. 3, by the double-exponential current source. On this basis, further analysis of SEU is given by TCAD in Section III. Here, the double-exponential current is expressed as

$$I(t) = I_0(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

$$I_0 = Q/(\tau_\alpha - \tau_\beta) \quad (2)$$

where I_0 is the peak of current source, Q is the amount of deposited charge, τ_α is the collection time constant of the junction, and τ_β is the time constant for initially establishing the ion track [11]. In this paper, I_0 is set as $\sim 174 \mu\text{A}$, while τ_α and τ_β are set as 200 and 50 ps, respectively.

From the above-mentioned analyses and simulation results, it is observed that QB (or Q depending on whether the node stores “0”) is the most vulnerable node. Thus, it is essential to make it stronger through the layout-level design. As illustrated in Fig. 2(b), the drains of the OFF-transistors are the sensitive areas. When the drain of P2 (OFF-state) is struck, many holes

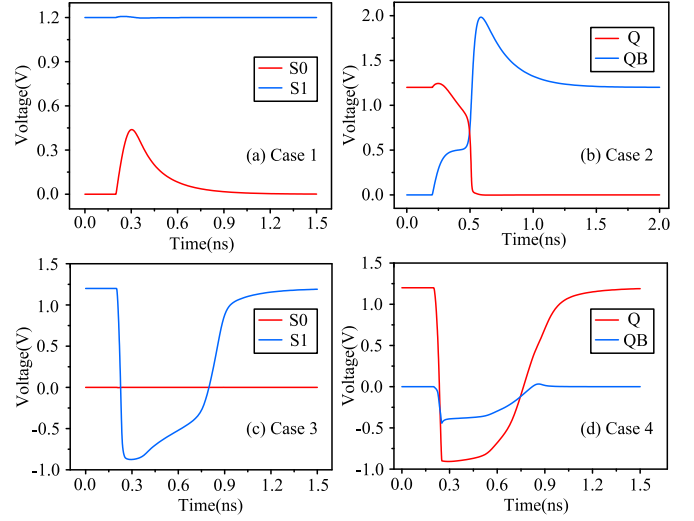


Fig. 3. HSPICE simulation results of the proposed RSP-14T structure with a positive (negative) transient injection. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

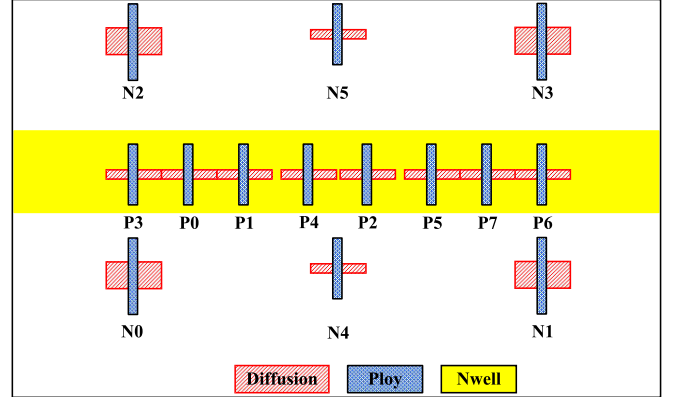


Fig. 4. Transistors placement of the proposed RSP-14T.

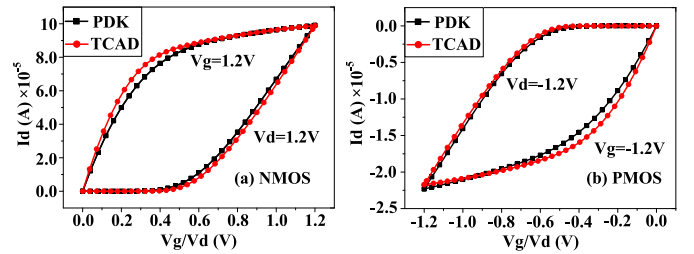


Fig. 5. $I_{\text{drain}}-V_{\text{drain}}$ and $I_{\text{drain}}-V_{\text{gate}}$ current curves of (a) nMOS between the TCAD model and PDK and (b) pMOS.

will be injected into the n-well from the VDD due to the bipolar effect. Consequently, the number of holes collected by the drain will be increased. Therefore, mitigating the bipolar effect in the pMOS connecting the storage node is a prior selection for enhancing the SRAM SEU immune. The source isolation technique, which has been proven highly effective in mitigating p-hit SET as [17] and [18] presented, is adopted for the proposed structure to complete the strengthening of the node. On this basis, in order to further mitigate the upset from “0” to “1” (occurring on node QB), the special design

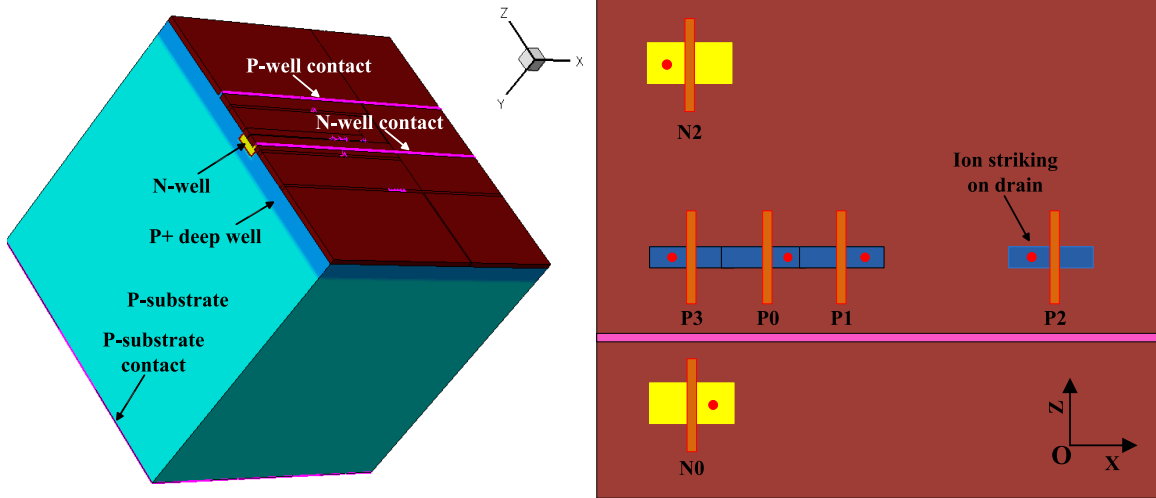


Fig. 6. TCAD model and the top view of the proposed RSP-14T.

of stacking pMOS transistors with layout-level optimization is also adopted simultaneously. As discussed in case 2, when the drain of P2 is struck, N0 and N2 will be affected, which fosters the upset of the SRAM cell. Therefore, in order to avoid charge sharing, the OFF-transistor N0 together with N2 should be distant from the other OFF-pMOS transistors. Similarly, P2 and P3 should be also distant from each other to prevent them from turning on at the same time. For layout-level optimization, the transistors placement of the proposed RSP-14T is shown in Fig. 4. With the above-mentioned circuit- and layout-level optimization, QB of the proposed RSP-14T can be as strong as possible. This deduction will be proven through the TCAD mixed-mode simulation in Section III.

III. SIMULATION RESULTS AND ANALYSIS

A. SEU Simulation

As mentioned earlier, the TCAD 3-D mixed-mode simulation, which has been confirmed to be a practical means, is used to investigate SEEs in ICs [19]–[22]. In order to match the electrical characteristics well, the TCAD models used in this paper are calibrated from the commercial 65-nm bulk CMOS process design kit (PDK). The calibration results of nMOS and pMOS are shown in Fig. 5(a) and (b), respectively. Here, the dimension of p-type silicon substrate used for simulation in TCAD is $20\ \mu\text{m} \times 20\ \mu\text{m} \times 20\ \mu\text{m}$, and the number of mesh elements is 299539. The transistors are made on the p-substrate with a constant doping of $1 \times 10^{16}\ \text{cm}^{-3}$. Meanwhile, their doping implants are created by Gaussian profiles. Concretely, the n-well Gaussian Arsenic profile results in a maximum concentration of $0.25 \times 10^{17}\ \text{cm}^{-3}$ at a depth of $0\ \mu\text{m}$, and with the concentration dropping off to $1 \times 10^{16}\ \text{cm}^{-3}$ at $0.65\ \mu\text{m}$; the p-well Gaussian Boron profile with a maximum concentration of $1 \times 10^{18}\ \text{cm}^{-3}$ at a depth of $0\ \mu\text{m}$, and with the concentration dropping off to $1 \times 10^{17}\ \text{cm}^{-3}$ at $0.55\ \mu\text{m}$; and the p+well Gaussian Boron profile with a maximum concentration of $1 \times 10^{18}\ \text{cm}^{-3}$ at a depth of $0\ \mu\text{m}$, and with the concentration dropping off to $1 \times 10^{16}\ \text{cm}^{-3}$ at $0.4\ \mu\text{m}$. Moreover, the back side of the substrate contact

is utilized along the bottom surface. The heavy ion physical model of TCAD is used to simulate the striking ion, where the charge track length and radius are fixed at $10\ \mu\text{m}$ and $50\ \text{nm}$, respectively. The spatial and temporal distributions of charge around the ions track are modeled using a Gaussian radial profile. In this paper, it is assumed that the center of the drain of the struck device is where the ion strikes, and the LET value is kept constant along the heavy ion track [12].

The TCAD model and schematic top view of the proposed RHS-14T cell are shown in Fig. 6. The xz plane and the $+y$ -axis are parallel and vertical to the surface of the cell, respectively. Here, the keywords θ and β are defined as the angle between the incident ion direction and the $-y$ -axis and the angle between the projection direction of the incident ion in the xz plane and the $+x$ -axis with clockwise orientation, respectively [12]. In this paper, it is assumed that $Q = "1,"$ QB = "0," S1 = "1," S0 = "0," and WL = "0." The SEMNUs caused by charge sharing between the OFF-transistors, when the single node is struck, are mainly investigated. Thus, as show in Fig. 6, transistors P0, P1, P2, P3, N0, and N2 are built in TCAD models and others are modeled by SPICE models. In order to avoid the charge sharing between transistors which may result in QB changed from "0" to "1," P2 is remote from P1, P0, and P3 in the layout. Meanwhile, in order to reduce the impact of charge sharing on N2 and N0 when P2 is hit by a particle, they are also moved away from P2. The SET is obtained by heavy ions striking on drain of OFF-transistors, and the efficiency of the charge sharing among the OFF-transistors is evaluated by the angle of the hit. Generally, the angle strike of 60° is utilized to estimate the dependence of the ion strike angle on SET [19], [23]; thus, in this paper, the angle of 60° and the normal angle strike are chosen to evaluate radiation hardness properties of the proposed RSP-14T.

Figs. 7 and 8 show the TCAD mixed-mode simulation results that the heavy ion strikes on the drain of the corresponding OFF-transistors (N0, N2, P0, P1, P2, and P3) with normal and angle strikes, respectively. As shown in Fig. 7, with a normal strike, the data of

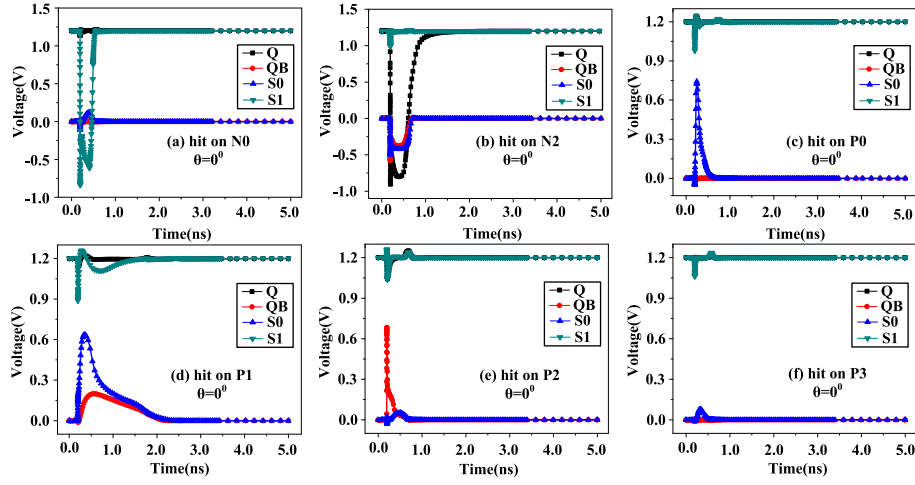


Fig. 7. TCAD mixed-mode simulation of node voltage versus time under normal strike with $\text{LET} = 60 \text{ MeV-cm}^2/\text{mg}$. (a) Hit on N0: $\theta = 0^\circ$. (b) Hit on N2: $\theta = 0^\circ$. (c) Hit on P0: $\theta = 0^\circ$. (d) Hit on P1: $\theta = 0^\circ$. (e) Hit on P2: $\theta = 0^\circ$. (f) Hit on P3: $\theta = 0^\circ$.

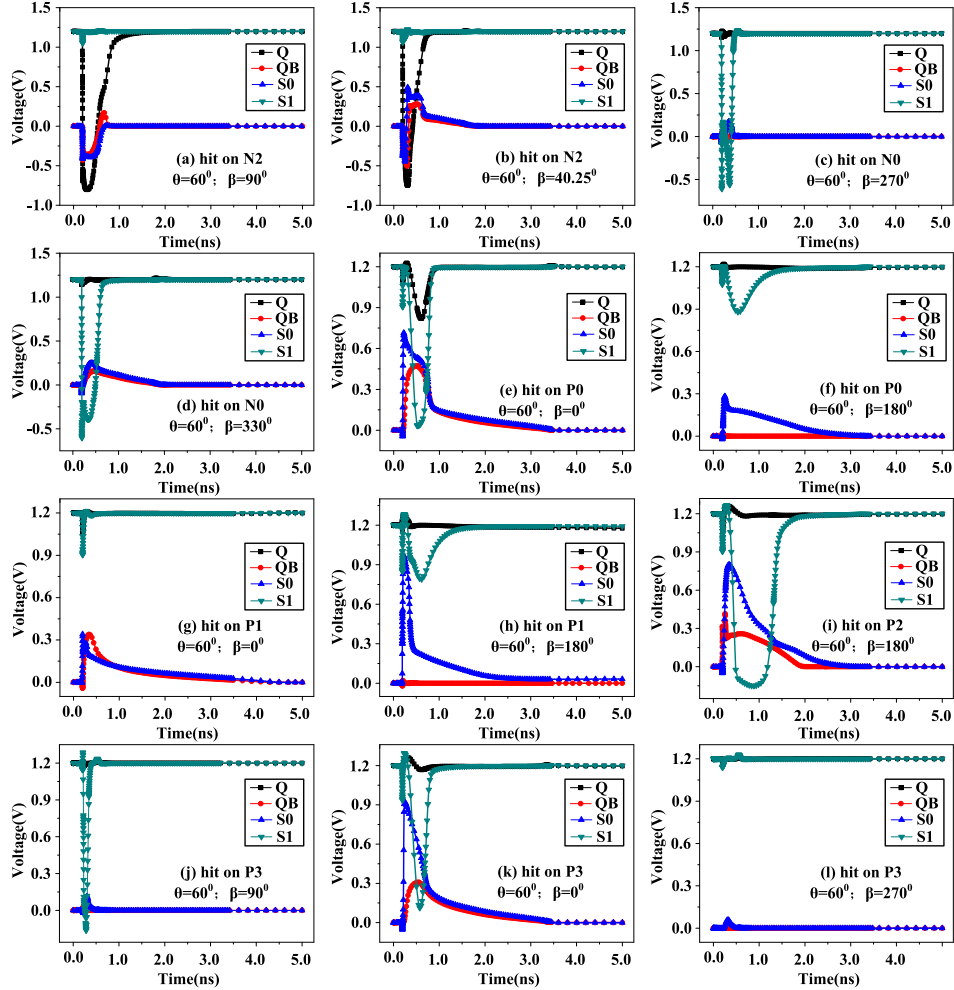


Fig. 8. TCAD mixed-mode simulation of node voltage versus time under angle strikes with $\text{LET} = 60 \text{ MeV-cm}^2/\text{mg}$. (a) Hit on N2: $\theta = 60^\circ$ and $\beta = 90^\circ$. (b) Hit on N2: $\theta = 60^\circ$ and $\beta = 40.25^\circ$. (c) Hit on N0: $\theta = 60^\circ$ and $\beta = 270^\circ$. (d) Hit on N0: $\theta = 60^\circ$ and $\beta = 330^\circ$. (e) Hit on P0: $\theta = 60^\circ$ and $\beta = 0^\circ$. (f) Hit on P0: $\theta = 60^\circ$ and $\beta = 180^\circ$. (g) Hit on P1: $\theta = 60^\circ$ and $\beta = 0^\circ$. (h) Hit on P1: $\theta = 60^\circ$ and $\beta = 180^\circ$. (i) Hit on P2: $\theta = 60^\circ$ and $\beta = 180^\circ$. (j) Hit on P3: $\theta = 60^\circ$ and $\beta = 90^\circ$. (k) Hit on P3: $\theta = 60^\circ$ and $\beta = 0^\circ$. (l) Hit on P3: $\theta = 60^\circ$ and $\beta = 270^\circ$.

the proposed RSP-14T can remain at its original value when the SEU occurs on whichever of its storage nodes, at $\text{LET} = 60 \text{ MeV-cm}^2/\text{mg}$. In addition, in order to

evaluate the efficiency of the charge sharing among the OFF-transistors of the proposed RSP-14T, the critical angles referring to Fig. 6 are selected. The simulation results,

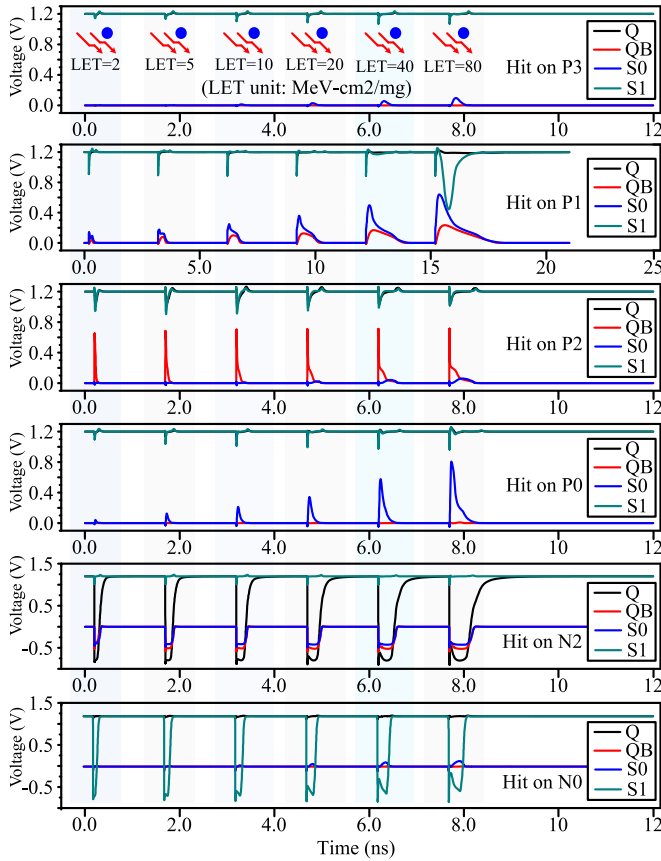


Fig. 9. Simulation results of the node voltage versus time with normal strikes at various LET values.

as shown in Fig. 8, present that with varying angles the proposed cell also mitigates the impact of the ion strike at $LET = 60 \text{ MeV-cm}^2/\text{mg}$. As the charge sharing of OFF-transistors has been considered in TCAD mixed-mode simulation, therefore, it can be concluded that the proposed RSP-14T can also mitigate multiple-node upsets caused by charge sharing between the OFF-transistors under an ion strike with the value of LET equaling to $60 \text{ MeV-cm}^2/\text{mg}$, which is larger than that reported for RHD-12T, $50 \text{ MeV-cm}^2/\text{mg}$ [12].

For further investigation, according to [17] and [18], the normal continuous strikes with the LET values at 2, 5, 10, 20, 40, and 80 $\text{MeV-cm}^2/\text{mg}$ have been also simulated by TCAD on the proposed RSP-14T, as shown in Fig. 9. It can be seen that SET becomes more and more obvious with the increasing LET value which means a much stronger perturbation in the cell. Nonetheless, with a normal strike, even when the LET value equals $80 \text{ MeV-cm}^2/\text{mg}$, our proposed RSP-14T cell can remain at its original data due to structure optimization and layout-level design.

In addition, with the angle θ increasing, there are more nodes directly affected by the ion striking. Fig. 10 presents the simulation results of the minimum LET that causes the storage state to turn over (LET_{th}) with θ varying from 70° to 89° under the ion strike on drain of P2 at three directions of $\beta = 180^\circ$, 220° , and 152° , respectively. As a function of the angle θ , the LET_{th} decreases sharply with the increase of it in

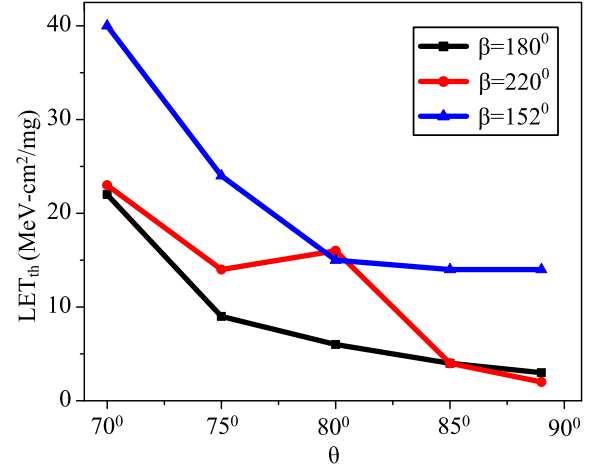


Fig. 10. LET_{th} as a function of the angle θ with $\beta = 180^\circ$, 220° and 152° , respectively.

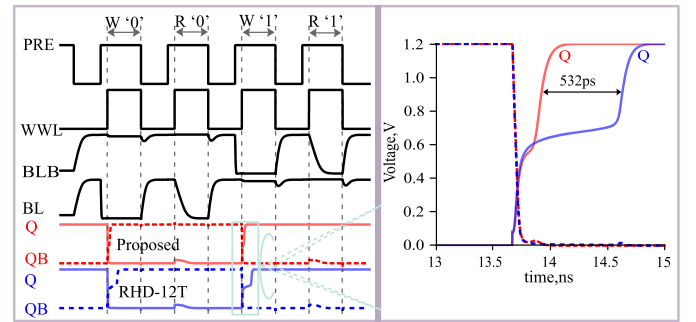


Fig. 11. Simulation waves of the proposed RSP-14T and RHD-12T by HSPICE.

terms of the overall trend [13]. Therefore, the proposed RSP-14T needs to be hardened further for more nodes to become upset simultaneously.

B. Circuit Performance Simulation

In order to characterize the performances of the proposed RSP-14T, the circuit-level simulations are accomplished in 65-nm commercial CMOS technology with 1.2-V power supply and nMOS typical corner and pMOS typical corner at 25°C . For a fair comparison, W/L of the pullup transistors (P0, P1, P2, P3, P4, P5, P6, and P7) and W/L of the driver transistors (N0, N1, N2, and N3) are $70 \text{ nm}/65 \text{ nm}$ and $210 \text{ nm}/65 \text{ nm}$, respectively. In addition, in order to ensure a successful write operation, W/L of the access transistors in RHD-11T and RHD-13T is $900 \text{ nm}/75 \text{ nm}$. Other than that, W/L of the access transistors (N4 and N5) is $70 \text{ nm}/65 \text{ nm}$ for other cells.

As mentioned earlier, transistors P0 and P7 are used to control the connection status of the internal feedback, which is beneficial for the write operation of the proposed RSP-14T. For characterization, the capacitance load of the bitline is set to 20 fF and write access time is defined as the time used for the voltage rising to 90% VDD. As shown in Fig. 11, the write access time of the proposed RSP-14T is 298 ps , which is 532 ps faster (i.e., $\sim 65\%$ improvement) compared

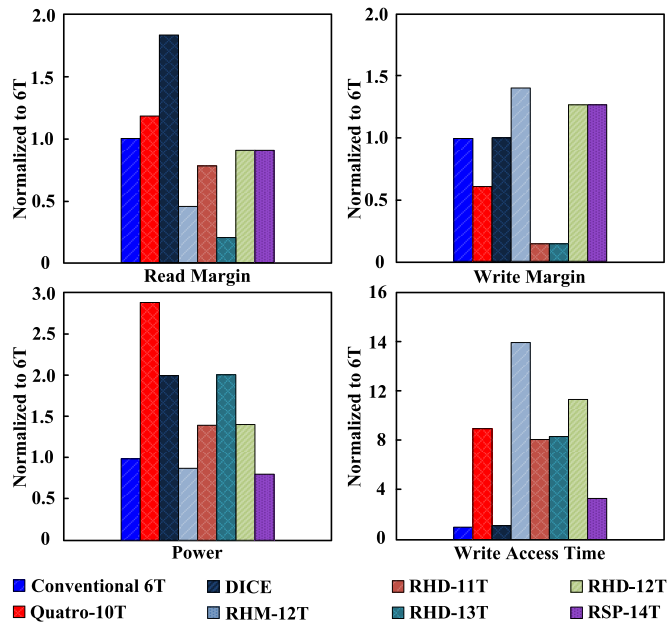


Fig. 12. Comparisons of different memory cells with normalized to conventional 6T.

with that of RHD-12T. Furthermore, as shown in Fig. 12, the write access time of the proposed RSP-14T is about 346%, 38%, 336%, 25%, 43%, and 40% of that of conventional 6T, Quatro-10T, DICE, RHM-12T, RHD-11T, and RHD-13T, respectively. Thus, the proposed RSP-14T is competitive for high-speed application compared with the above-mentioned alternatives.

In addition, as a criterion of stability for SRAM, static noise margin is widely used. Thus, to characterize the read and write stability of the proposed RSP-14T, it also presented in this paper. As shown in Fig. 12, the read margin of the proposed RSP-14T is 95%, 81%, 52%, 211%, 124%, 483%, and 100% of 6T, Quatro-10T, DICE, RHM-12T, RHD-11T, RHD-13T, and RHD-12T, respectively. Meanwhile, the write margin of the proposed RSP-14T is 133%, 227%, 133%, 92%, 1026%, 1026%, and 100% of 6T, Quatro-10T, DICE, RHM-12T, RHD-11T, RHD-13T, and RHD-12T, respectively. It can be seen that the proposed RSP-14T has the same read/write margins as those of RHD-12T.

The power consumption (average of write and read operation) of the proposed RSP-14T is 72%, 22%, 32%, 74%, 46%, 32%, and 51% of 6T, Quatro-10T, DICE, RHM-12T, RHD-11T, RHD-13T, and RHD-12T, respectively, which indicates that the proposed RSP-14T has lower power consumption than the above-mentioned alternatives. Especially, compared with RHD-12T, the two pMOS-transistors added in the proposed RSP-14T inevitably lead to an area being increased slightly. However, its power and write speed have a substantial improvement without read and write margins decreased. Thus, considering the speed, power consumption, and the immune capability of SEU, the proposed RSP-14T is more acceptable.

Moreover, considering the effects of process, voltage, and temperature variations, the SEU tolerance capability of the above-mentioned cells is also analyzed by 2000 times

Monte Carlo simulations with the injected charge set 24 fC. The results show that the failure probabilities of conventional 6T, RHD-11T, and RHD-13T are 100%, when the transmission gates of RHD-11T and RHD-13T are on, and those of DICE and RHM-12T are 0%. However, as mentioned earlier, the worse read noise margin as well as a larger write access time of RHM-12T limits its application, and the failure probabilities of Quatro-10T, RHD-12T, and the proposed RSP-14T are 6.7%, 3.3%, and 2.4%, respectively. Nonetheless, compared with the referenced RHD-12T, lower failure probability of the proposed RSP-14T was achieved by the circuit-level simulation without considering the charge sharing.

IV. CONCLUSION

In this paper, the radiation-hardened 14T SRAM bitcell with speed and power optimized (RSP-14T) based on the source isolation technique is presented. Through the circuit- and layout-level optimization, the mixed-mode simulation results show that it can not only tolerate an SEU on any of its inner single node, but also have partial SEMNUs immune even at the LET value equal to 60 MeV-cm²/mg, which is larger than that reported for RHD-12T. Meanwhile, compared with RHD-12T, its write speed and power consumption are significantly improved. Thus, the excepting area increased slightly, and the proposed RSP-14T cell is more suitable for the space application.

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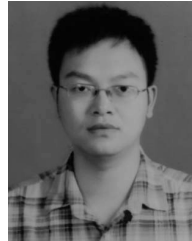
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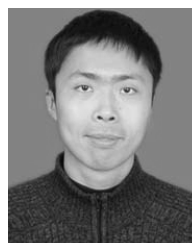


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