

# A New Six-Switch Five-Level Active Neutral Point Clamped Inverter for PV Applications

Hongliang Wang, *Senior Member, IEEE*, Lei Kou, *Student Member, IEEE*, Yan-Fei Liu, *Fellow, IEEE* and Paresh C. Sen, *Life Fellow, IEEE*

**Abstract**—Multilevel inverters are one of the preferred solutions for medium-voltage and high-power applications and have found successful industrial applications. Five-level Active Neutral Point Clamped inverter (5L-ANPC) is one of the most popular topologies among five-level inverters. A Six-Switch 5L-ANPC (6S-5L-ANPC) topology is proposed. Compared to the conventional 5L-ANPC inverters, the 6S-5L-ANPC reduces two active switches and has lower conduction loss. The proposed modulation enables the 6S-5L-ANPC inverter to operate under both active and reactive power conditions. The FC capacitance is designed under both active and reactive power conditions. The analysis shows the proposed topology is suitable for photovoltaic (PV) grid-connected applications. A 1KVA single-phase experimental prototype is built to verify the validity and flexibility of the proposed topology and modulation method.

**Index Terms**—Multilevel inverter, Active Neutral Point Clamped (ANPC), Flying-Capacitor (FC), PWM modulation

## I. INTRODUCTION

Multilevel inverters have received increased attention in both academia and industry nowadays as one of the optimal solutions of power conversion for medium and high power applications [1]–[4]. For medium power application, the motivation for the use of multilevel inverters is to reduce the switch voltage stress as well as the output filter size. They also have the advantages of improved output quality, lower Total Harmonic Distortion (THD), lower common-mode voltage and lower Electromagnetic Interference (EMI) in contrast to their two level counterparts [5]. Furthermore, the multilevel inverters have possibility to achieve higher efficiency over the conventional inverters due to the use of low voltage drop devices, leading to their low voltage application such as photovoltaic (PV) cells [6]–[8].

There are three types of classic multilevel inverter topologies: Neutral Point Clamped (NPC) type [9], [10], Flying-Capacitor (FC) type [11], [12], and Cascaded H-Bridge (CHB) type [13], [14]. A single-phase leg of three types of topologies generating five-level output are shown in Fig. 1.

The NPC type multilevel inverters generate the voltage levels from the neutral point voltage by adopting the clamping diodes. However, when voltage levels increase, more clamping diodes, active semiconductor switches and DC-link capacitors are needed. Excessive number of clamping diodes

are connected in series to block the higher voltage, thus producing more conduction losses and generating reverse recovery currents that affect the switching losses of other devices. The DC-link voltage balancing problem is another issue for higher levels NPC inverters.

As another type of classic multilevel inverters, the FC inverter produces the required output voltage levels by summing the FC and DC-link voltages. The increased number of capacitors in higher levels leads to complex control method to balance the voltages of both DC-link capacitors and FCs. The higher switching frequency to keep the capacitors properly balanced and capacitors maintenance costs result in the less industrial penetration of FC type.

The CHB multilevel inverters use series-connected H-bridge cells with an isolated dc voltage sources connected to each cell. Similarly, to have more output levels, more cells are needed. This will lead to impracticality of this type of topology since more isolated DC sources are required.

A generalized multilevel inverter topology is presented in [15], which is capable of balancing each voltage level regardless of the inverter control and load characteristics. The aforementioned conventional multilevel inverters can be derived from this generalized inverter topology. Besides, some new multilevel topologies, such as Multilevel Modular Capacitor Clamped (MMCC) [16] and zigzag multilevel inverter [17] can also be derived using the method in [15].

Hybrid multilevel inverters topologies combine some features of NPC and FC that provides the possibilities to take advantages of both topologies [18], [19]. Among hybrid topologies, the Five-Level Active Neutral Point Clamped (5L-ANPC) inverter provides an acceptable compromise between cost and performance [20]–[28]. As shown in Fig. 2 (a), the 5L-ANPC inverter combines a 3L-ANPC leg with a 3L-FC power cell. The number of levels is increased with the levels introduced by the FC. This topology enables the modularity factor that is lacking in the NPC type inverter by adding the FC to reach higher level without adding series-connected diodes. In addition, the ANPC inverters splits the DC-link into two capacitors, so the complexity of DC-link capacitor voltages balancing is reduced compared to the conventional NPC and FC type inverters which need four DC capacitors in series. Due to the reduced costs, volume and control complexity, the 5L-ANPC inverter is receiving more attention recently and is already commercially used for medium power level industrial applications [29]. Fig. 2 (b) and (c) show additional two types of 5L-ANPC inverter [30].

The Authors are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada. (email: hongliang.wang@queensu.ca, kou.lei@queensu.ca, yanfei.liu@queensu.ca, senp@queensu.ca)

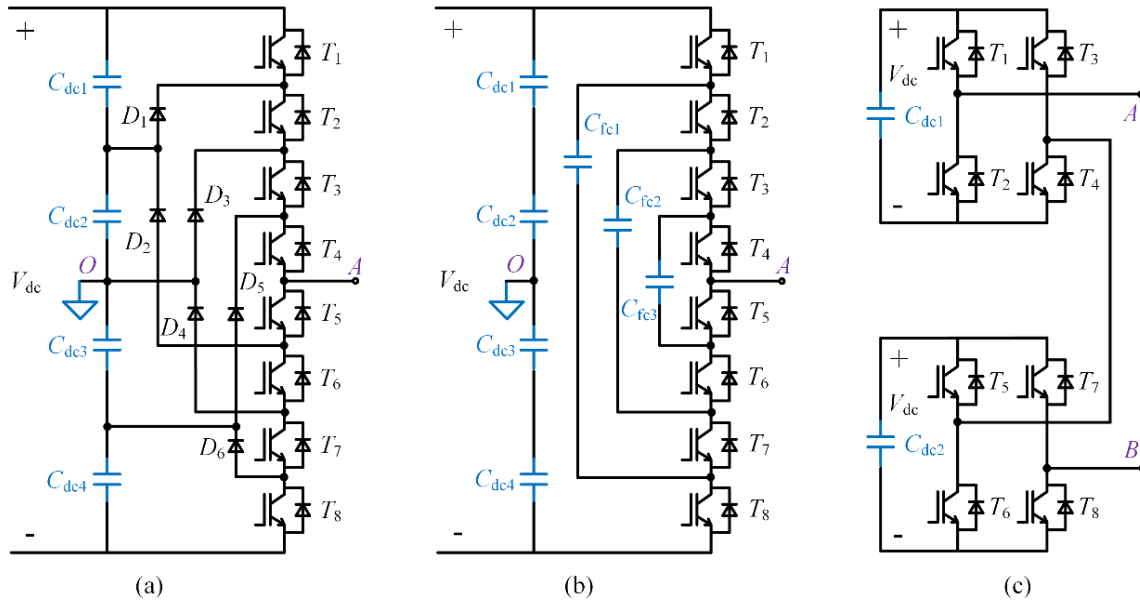


Fig. 1. The conventional multilevel inverter topologies (five-level). (a) NPC type. (b) FC type. (c) CHB type.

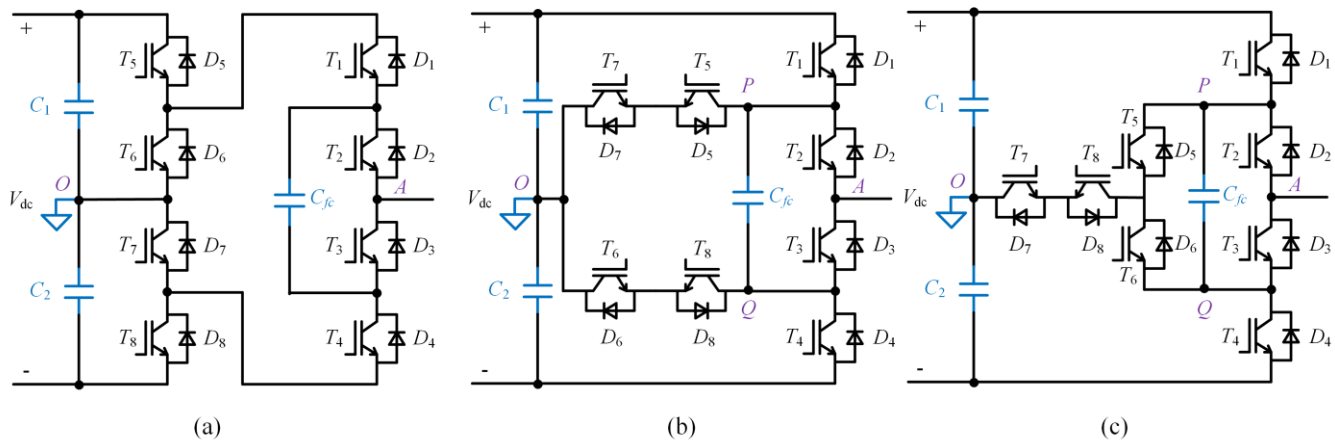


Fig. 2. The conventional 5L-ANPC inverter topologies. (a) Type I. (b) Type II. (c) Type III.

The redundant switching states in ANPC inverters allow the voltage across FC to be regulated. To generate the switching pulses and simultaneously regulate the FC voltage, a variety of modulation strategies have been presented such as carrier-based Pulse Width Modulation (PWM) [31], modified carrier-based PWM [23], real time THD minimization [32] and selective harmonic elimination PWM [33][34].

From Fig. 2, it is observed that for the existing conventional 5L-ANPC inverter topologies, at least eight active switches are required. And from the point view of industrial application, it would be more desirable if the cost of the system can be reduced. The motivation of this paper is to reduce the number of active switches. For PV application, the output current and grid voltage are generally in phase, so some of reactive current paths can be removed. Based on this, a novel Six-Switch Five-Level ANPC (6S-5L-ANPC) inverter topology is proposed [35]. Compared to the conventional 5L-

ANPC inverter, the proposed topology requires only six active semiconductor switches, reducing the volume of system. Additionally, with the proposed modulation method applied to the proposed 6S-5L-ANPC inverter, the system is capable of operating under both active and reactive power conditions.

This paper is organized as follows: Section II describes operating principles of the proposed 6S-5L-ANPC inverter; Section III makes a comparison between the conventional 5L-ANPC and 6S-5L-ANPC inverters in terms of device voltage stress, efficiency and system volume; Section IV discusses the modulation strategy of 6S-5L-ANPC topology; Section V provides a design method for the FC capacitance under active and reactive power conditions; Section VI gives the simulation verification and the maximum reactive power capability of the proposed topology; Section VII presents the experimental results and Section VIII gives the conclusion.

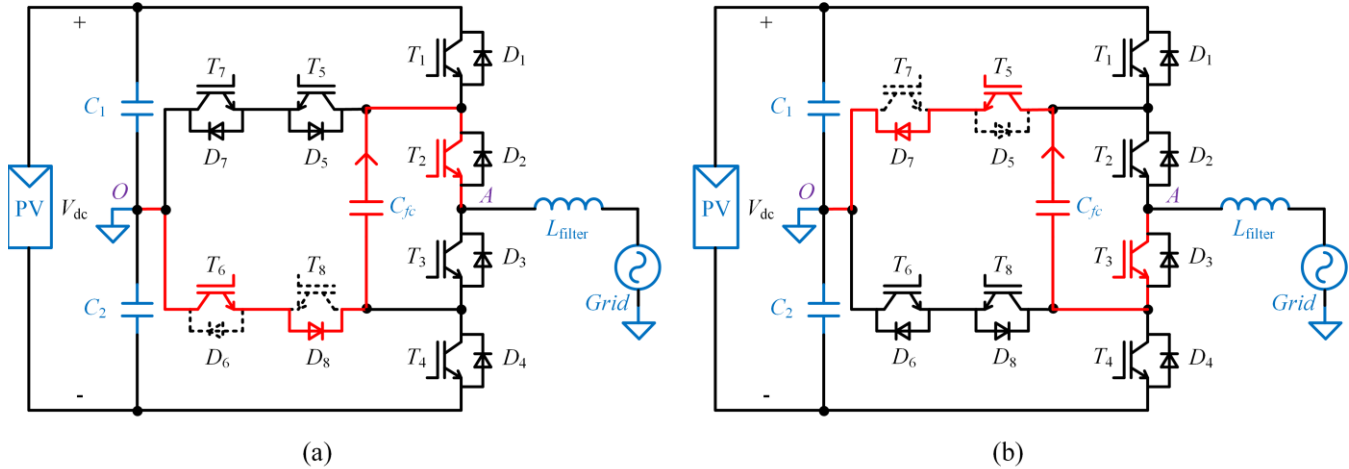


Fig. 3. Active current paths for two switching states of type II conventional 5L-ANPC inverter. (a) +1 level switching state. (b) -1 level switching state.

## II. OPERATING PRINCIPLES OF PROPOSED 6S-5L-ANPC INVERTER

### A. Introduction of 6S-5L-ANPC Inverter

The 5L-ANPC inverter is a good choice for renewable energy harvesting because of its improved efficiency and output waveform. The configuration of Type II conventional 5L-ANPC inverter is shown in Fig. 2 (b). First, the DC-link voltage is defined as  $V_{dc}$ . The DC-link consists of two capacitors ( $C_1$ ,  $C_2$ ), whose voltages are rated at half of dc voltage ( $V_{dc}/2$ ). A flying-capacitor ( $C_{fc}$ ) is required to provide one quarter of dc voltage ( $V_{dc}/4$ ). Five output voltage levels  $+V_{dc}/2$ ,  $+V_{dc}/4$ ,  $0$ ,  $-V_{dc}/4$  and  $-V_{dc}/2$  (which are defined as +2, +1, 0, -1 and -2 respectively) are achieved by summing the FC voltage and DC-link capacitor voltages.

For PV grid-connection application, the inverter output current is required to be in phase with grid voltage. In this situation, some of the reactive current paths can be ignored, which means some active switches can be replaced by fast recovery diodes. For the switching states which output +2 and -2 levels, ( $T_1$ ,  $T_2$ ) and ( $T_3$ ,  $T_4$ ) are turned on for active current flow and the reactive current path is pass through their anti-parallel diodes. So these four active switches cannot be removed. Similarly, for the switching states which output +1 and -1 levels, ( $T_1/D_1$ ,  $T_3/D_3$ ) and ( $T_2/D_2$ ,  $T_4/D_4$ ) are turned on. Both switching states are charging the FC in unity power factor condition. To balance the FC voltage, there are additional two switching state which also output +1 and -1 level to discharge the FC, which are called redundant switching states, as shown in Fig. 3 (a) and (b). The red line shows the active power current path. With above motivation, the parts for reactive power operation (dashed parts) can be ignored. There are also two redundant 0 switching states: one is through  $T_6$ ,  $D_8$  and  $T_2$ ; the other is through  $T_3$ ,  $T_5$  and  $D_7$ . Since  $T_1/D_1$  to  $T_4/D_4$  are kept, there is no change for 0 output level switching states. Finally, a novel six-switch 5L-ANPC (6S-5L-ANPC) inverter topology is derived, as shown in Fig. 4.

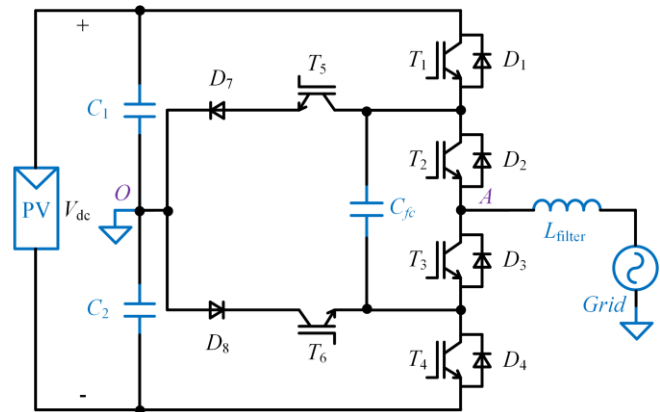


Fig. 4. Configuration of the proposed 6S-5L-ANPC inverter.

TABLE I  
SWITCHING STATES, OUTPUT VOLTAGE AND IMPACT ON THE FC VOLTAGE OF 6S-5L-ANPC INVERTER

No	Active Switch State						$V_{out}$	Flying Capacitor $C_{fc}$	
	$T_1$	$T_2$	$T_3$	$T_4$	$T_5$	$T_6$		$i_{out} > 0$	$i_{out} < 0$
A	1	1	0	0	0	1	+2	--	--
B	1	0	1	0	0	1	+1	Charge	Discharge
C	0	1	0	0	0	1	+1	Discharge	Charge
D	0	0	1	0	0	1	+0	--	--
E	0	1	0	0	1	0	-0	--	--
F	0	0	1	0	1	0	-1	Charge	Discharge
G	0	1	0	1	1	0	-1	Discharge	Charge
H	0	0	1	1	1	0	-2	--	--

In Fig. 4, six active power semiconductor switches ( $T_1$  –  $T_6$ ) and two discrete diodes ( $D_7$ ,  $D_8$ ) are needed to generate five-level output. The outer switches ( $T_1$  –  $T_4$ ) operate at switching frequency and inner switches ( $T_5$ ,  $T_6$ ) commute at line frequency. Additionally, the current paths including  $T_5$  and  $T_6$  also flow through the fast recovery diodes, which can only achieve unidirectional current flow. Thus the selection of inner switches ( $T_5$ ,  $T_6$ ) can be IGBT without antiparallel diode, further reducing the system cost.

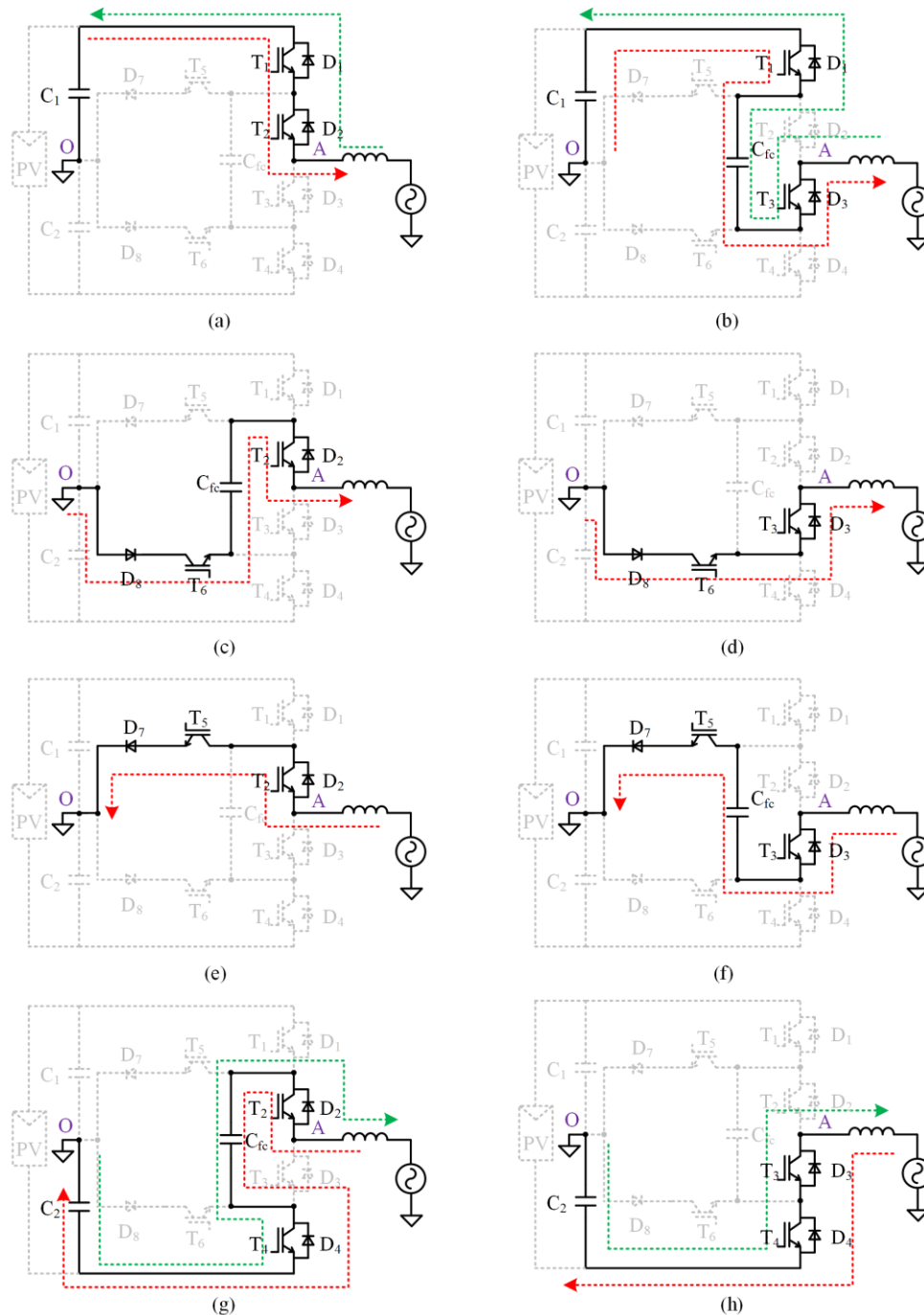


Fig. 5. Eight switching states for 6S-5L-ANPC inverter. (a) State A: +2. (b) State B: +1. (c) State C: +1. (d) State D: 0. (e) State E: 0. (f) State F: -1. (g) State G: -1. (h) State H: -2.

As can be observed from Fig. 4, in contrast to the conventional 5L-ANPC inverters which need eight active switches and other types of five-level inverters which require more devices, the proposed 6S-5L-ANPC inverter employs only six active switches and two discrete diodes. The reduced number of active switches sacrifice some reactive current paths. However, with special modulation method, the proposed topology has the capability of feeding reactive power

into the grid to support the stability of the power system, which will be addressed in the Section IV.

### B. Operation of 6S-5L-ANPC Topology

The 6S-5L-ANPC inverter consists of eight switching states that generate five-level voltage levels at the output based on capacitor voltages, as shown in Table I. The output current is defined as  $i_{out}$ .  $V_{out}$  represents the output voltage level. Fig. 5 shows eight different switching states (state A to H) and

current paths (red line shows the active current path while green line represents the reactive power path).

In Table I, it is observed that there are three pairs of redundant switching states which generate same output voltage level: states B and C are redundant switching states to generate +1 voltage level; similarly, (D, E) and (F, G) are redundant states to generate 0 and -1, respectively. Although the redundant states (B, C) and (F, G) generate the same output voltage level, their effect on the FC voltage is opposite to each other due to the change in the direction of FC current. This leads to the possibility of regulating the FC voltage to a constant value ( $V_{dc}/4$ ). The sign of load current  $i_{out}$  and deviation sign of FC voltage from its reference value are required to decide which redundant switching state to be chosen.

In Fig. 5, it is observed that among eight switching states, four states (C, D, E, and F) allow unidirectional current flow due to the presence of discrete diode. Therefore, appropriate selection of switching states under reactive power operation is very important. The special modulation strategy for the proposed topology will be discussed in Section IV.

### III. COMPARISON BETWEEN 6S-5L-ANPC AND THE CONVENTIONAL 5L-ANPC INVERTERS

To better illustrate the advantage of the proposed topology, it is important to make a comparison between 6S-5L-ANPC inverter and the conventional 5L-ANPC inverters in terms of device voltage rating, switching frequency, efficiency and system volume.

#### A. Device voltage stress and switching frequency

Table II shows the voltage stress and switching frequency of devices for four types of 5L-ANPC inverters.  $f_{Line}$  and  $f_s$  represent the line frequency and switching frequency respectively.

Compared to Type I 5L-ANPC inverter: the voltage stress of  $T_1/D_1$  and  $T_4/D_4$  for 6S-5L-ANPC inverters is increased to  $0.75V_{DC}$ , which means a higher voltage rating device should be selected for these two switches. However, the switching loss of these two devices are generated in the same way as in Type I 5L-ANPC inverter. For example,  $T_1/D_1$  will carry the output current  $i_{out}$  when switched on and block the voltage levels of  $0.25V_{DC}$  when switched off in the positive grid cycle. On the other hand, for Type I 5L-ANPC inverter,  $T_1/D_1$  and  $T_4/D_4$  are switched on and off at high frequency  $f_s$  for the whole grid cycle; while for the proposed topology,  $T_1/D_1$  and  $T_4/D_4$  are only operating at high frequency for half line period and turned off for the other half line period, so the switching loss of these two devices will be lower (approximately half of switching loss in Type I topology).

Compared to Type II 5L-ANPC inverter: the voltage stress of devices in the proposed topology is the same as that of Type II 5L-ANPC topology, and two active switches are reduced.

Compared to Type III 5L-ANPC inverter: the difference between the proposed topology and Type III is the voltage stress of  $T_5/D_5$  and  $T_6/D_6$  in Type III 5L-ANPC inverter is

reduced to  $0.25V_{DC}$ . However, the conduction loss of Type III 5L-ANPC topology is higher, which will be given in the following part.

#### B. Conduction Loss Analysis

The conduction loss comparison can be performed considering the number of connected devices in series when they are on, as shown in Table III. The symbols + and - represent the minimum and maximum number of conducting devices.

For Type I 5L-ANPC inverter, three devices are always connected in series to carry the main current for all eight states; while for the proposed topology: during the switching states A, B, G and H, the output current is going through only two devices. Therefore, compared to Type I 5L-ANPC topology, the conduction loss of the proposed topology during these four states is reduced by 1/3, and the whole conduction loss is approximately reduced by 1/6.

Compared to Type II 5L-ANPC inverter: the conduction loss of 6S-5L-ANPC inverter is the same as that of Type II 5L-ANPC topology.

The difference between 6S-5L-ANPC and Type III 5L-ANPC topologies is: during the switching states C, D, E and F, three devices are needed to conduct the output current for 6S-5L-ANPC inverter while Type III requires four devices. Similarly, compared to Type III 5L-ANPC topology, the conduction loss of the proposed topology during four states C, D, E and F is reduced by 1/4, and the whole conduction loss is approximately reduced by 1/8.

With above analysis, it is concluded that the conduction loss of the proposed 6S-5L-ANPC topology is the same as that of Type II conventional 5L-ANPC topology, and is lower than Type I and Type III 5L-ANPC inverters.

#### C. Switching Loss Analysis

Table IV shows the switching loss in terms of switching states commutations.

Compared to Type I 5L-ANPC inverter: as mentioned earlier, for 6S-5L-ANPC inverter, the devices  $T_1/D_1$  and  $T_4/D_4$  need to block  $0.75V_{DC}$  voltage when they are not conducting current. However, the switching loss of these two devices are generated in the same way as in Type I 5L-ANPC inverter. From Table IV, it is observed that for all switching state transitions, the device voltage change is  $0.25V_{DC}$  and the current is output current  $i_{out}$ . Therefore, if the device selection for 6S-5L-ANPC and Type I 5L-ANPC is the same, then the switching loss for two topologies should be identical. If higher voltage rating devices are selected for  $T_1/D_1$  and  $T_4/D_4$  in 6S-5L-ANPC topology, then its switching loss will be slightly higher than Type I due to the increased turn-on energy for higher voltage rating device.

Compared to Type II, III 5L-ANPC inverter: based on Table II and IV, it is observed that, due to the same device selection and switching states commutations, the switching loss of 6S-5L-ANPC inverter is the same as that of Type II and III 5L-ANPC inverters.

TABLE II  
VOLTAGE STRESS AND SWITCHING FREQUENCY OF DEVICES FOR FOUR TYPES OF 5L-ANPC INVERTERS

Device	Type I 5L-ANPC		Type II 5L-ANPC		Type III 5L-ANPC		6S-5L-ANPC	
	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency
T <sub>1</sub> /D <sub>1</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.75V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.75V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.75V <sub>DC</sub>	f <sub>s</sub> for half line cycle
T <sub>2</sub> /D <sub>2</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>
T <sub>3</sub> /D <sub>3</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>
T <sub>4</sub> /D <sub>4</sub>	0.25V <sub>DC</sub>	f <sub>s</sub>	0.75V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.75V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.75V <sub>DC</sub>	f <sub>s</sub> for half line cycle
T <sub>5</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>Line</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>
T <sub>6</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>Line</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>
D <sub>5</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>Line</sub>	Not needed	Not needed
D <sub>6</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>Line</sub>	Not needed	Not needed
T <sub>7</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	Not needed	Not needed
T <sub>8</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	Not needed	Not needed
D <sub>7</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle
D <sub>8</sub>	0.5V <sub>DC</sub>	f <sub>Line</sub>	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle	0.25V <sub>DC</sub>	f <sub>s</sub> for half line cycle

TABLE III  
CONDUCTION LOSS OF FOUR TYPES OF 5L-ANPC INVERTERS

Switching State	Type I 5L-ANPC	Type II 5L-ANPC	Type III 5L-ANPC	6S-5L-ANPC
A (+2)	$i_{out} > 0$ T <sub>1</sub> , T <sub>2</sub> , T <sub>3</sub>	-	T <sub>1</sub> , T <sub>2</sub>	+ T <sub>1</sub> , T <sub>2</sub>
	$i_{out} < 0$ D <sub>1</sub> , D <sub>2</sub> , D <sub>5</sub>	-	D <sub>1</sub> , D <sub>2</sub>	+ D <sub>1</sub> , D <sub>2</sub>
B (+1)	$i_{out} > 0$ T <sub>1</sub> , T <sub>3</sub> , D <sub>3</sub>	-	T <sub>1</sub> , D <sub>3</sub>	+ T <sub>1</sub> , D <sub>3</sub>
	$i_{out} < 0$ D <sub>1</sub> , D <sub>5</sub> , T <sub>3</sub>	-	D <sub>1</sub> , T <sub>3</sub>	+ D <sub>1</sub> , T <sub>3</sub>
C (+1)	$i_{out} > 0$ T <sub>2</sub> , T <sub>7</sub> , D <sub>4</sub>	+	T <sub>2</sub> , T <sub>6</sub> , D <sub>8</sub>	+ T <sub>2</sub> , T <sub>5</sub> , T <sub>8</sub> , D <sub>6</sub>
	$i_{out} < 0$ D <sub>2</sub> , D <sub>7</sub> , T <sub>4</sub>	+	D <sub>2</sub> , D <sub>6</sub> , T <sub>8</sub>	+ D <sub>2</sub> , D <sub>5</sub> , D <sub>8</sub> , T <sub>6</sub>
D (0)	$i_{out} > 0$ T <sub>7</sub> , D <sub>3</sub> , D <sub>4</sub>	+	D <sub>3</sub> , T <sub>6</sub> , D <sub>8</sub>	+ D <sub>3</sub> , T <sub>5</sub> , T <sub>8</sub> , D <sub>6</sub>
	$i_{out} < 0$ D <sub>7</sub> , T <sub>3</sub> , T <sub>4</sub>	+	T <sub>3</sub> , D <sub>6</sub> , T <sub>8</sub>	+ T <sub>3</sub> , D <sub>5</sub> , D <sub>8</sub> , T <sub>6</sub>
E (0)	$i_{out} > 0$ T <sub>1</sub> , T <sub>2</sub> , D <sub>6</sub>	+	T <sub>2</sub> , T <sub>7</sub> , D <sub>6</sub>	+
	$i_{out} < 0$ D <sub>1</sub> , D <sub>2</sub> , T <sub>6</sub>	+	D <sub>2</sub> , D <sub>7</sub> , T <sub>3</sub>	+
F (-1)	$i_{out} > 0$ T <sub>1</sub> , D <sub>3</sub> , D <sub>6</sub>	+	D <sub>3</sub> , T <sub>7</sub> , D <sub>5</sub>	+
	$i_{out} < 0$ D <sub>1</sub> , T <sub>3</sub> , T <sub>6</sub>	+	T <sub>3</sub> , D <sub>7</sub> , T <sub>5</sub>	+
G (-1)	$i_{out} > 0$ T <sub>2</sub> , D <sub>4</sub> , D <sub>8</sub>	-	T <sub>2</sub> , D <sub>4</sub>	+ T <sub>2</sub> , D <sub>4</sub>
	$i_{out} < 0$ D <sub>2</sub> , T <sub>4</sub> , T <sub>8</sub>	-	D <sub>2</sub> , T <sub>4</sub>	+ D <sub>2</sub> , T <sub>4</sub>
H (-2)	$i_{out} > 0$ D <sub>3</sub> , D <sub>4</sub> , D <sub>8</sub>	-	D <sub>3</sub> , D <sub>4</sub>	+ D <sub>3</sub> , D <sub>4</sub>
	$i_{out} < 0$ T <sub>3</sub> , T <sub>4</sub> , T <sub>8</sub>	-	T <sub>3</sub> , T <sub>4</sub>	+ T <sub>3</sub> , T <sub>4</sub>

TABLE IV  
SWITCHING LOSS OF FOUR 5L-ANPC INVERTERS

Switching State	Type I 5L-ANPC	Type II 5L-ANPC	Type III 5L-ANPC	6S-5L-ANPC	$\Delta V$	$\Delta I$
A (+2) ↔ B (+1)	$i_{out} > 0$ T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$
A (+2) ↔ C (+1)	$i_{out} > 0$ T <sub>1</sub> , D <sub>4</sub>	T <sub>1</sub> , D <sub>8</sub>	T <sub>1</sub> , D <sub>8</sub>	T <sub>1</sub> , D <sub>8</sub>	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>1</sub> , T <sub>4</sub>	D <sub>1</sub> , T <sub>8</sub>	D <sub>1</sub> , T <sub>8</sub>	Not needed	0.25V <sub>DC</sub>	$i_{out}$
B (+1) ↔ D (0)	$i_{out} > 0$ T <sub>1</sub> , D <sub>4</sub>	T <sub>1</sub> , D <sub>8</sub>	T <sub>1</sub> , D <sub>8</sub>	T <sub>1</sub> , D <sub>8</sub>	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>1</sub> , T <sub>4</sub>	D <sub>1</sub> , T <sub>8</sub>	D <sub>1</sub> , T <sub>8</sub>	Not needed	0.25V <sub>DC</sub>	$i_{out}$
C (+1) ↔ D (0)	$i_{out} > 0$ T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$
F (-1) ↔ E (0)	$i_{out} > 0$ T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$
G (-1) ↔ E (0)	$i_{out} > 0$ T <sub>1</sub> , D <sub>4</sub>	D <sub>4</sub> , T <sub>7</sub>	D <sub>4</sub> , T <sub>7</sub>	Not needed	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>1</sub> , T <sub>4</sub>	T <sub>4</sub> , D <sub>7</sub>	T <sub>4</sub> , D <sub>7</sub>	T <sub>4</sub> , D <sub>7</sub>	0.25V <sub>DC</sub>	$i_{out}$
H (-2) ↔ F (-1)	$i_{out} > 0$ T <sub>1</sub> , D <sub>4</sub>	D <sub>4</sub> , T <sub>7</sub>	D <sub>4</sub> , T <sub>7</sub>	Not needed	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>1</sub> , T <sub>4</sub>	T <sub>4</sub> , D <sub>7</sub>	T <sub>4</sub> , D <sub>7</sub>	T <sub>4</sub> , D <sub>7</sub>	0.25V <sub>DC</sub>	$i_{out}$
H (-2) ↔ G (-1)	$i_{out} > 0$ T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	T <sub>2</sub> , D <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$
	$i_{out} < 0$ D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	D <sub>2</sub> , T <sub>3</sub>	0.25V <sub>DC</sub>	$i_{out}$

#### D. System Volume

In terms of volume of DC-link capacitors: for all 5L-ANPC inverter topologies including the proposed 6S-5L-ANPC inverter, the upper DC-link capacitor and FC are providing the

energy to the output side in positive grid cycle while during negative grid cycle the lower DC-link capacitor and FC are transferring the energy to the output side. Therefore, the DC-link capacitance selection for 6S-5L-ANPC is the same as the conventional 5L-ANPC inverters.

In terms of volume of FC: under unity power factor condition, the FC value of the proposed topology is the same as the conventional 5L-ANPC inverters. When power factor is getting lower, with same FC capacitance, the voltage ripple of the proposed topology will be larger than the conventional ANPC inverters. The specific analysis of FC design is discussed in Section V and the maximum reactive power capability of the proposed topology is presented in Section VI.

With the loss and cost analysis developed above, it is concluded that: 1) The efficiency of the proposed topology is the same as Type II 5L-ANPC inverter; 2) Compared to Type I 5L-ANPC topology, the conduction loss of the proposed topology is lower, but the switching loss of the proposed topology is slightly higher. Therefore, under high power condition whose switching frequency is low, the proposed topology has higher efficiency over Type I 5L-ANPC inverter [30]; 3) Compared to Type III 5L-ANPC inverter, the efficiency of the proposed 6S-5L-ANPC inverter is higher because its conduction loss is lower than that of Type III 5L-ANPC topology; 4) The DC-link capacitance selection for 6S-5L-ANPC inverter is the same as the conventional 5L-ANPC inverters. For high power factor applications such as PV application, the proposed 6S-5L-ANPC topology is a good choice because it achieves the reduction of two active switches and the same performance as the conventional 5L-ANPC inverters.

#### IV. MODULATION STRATEGY

As can be observed from Fig. 5, during the four switching states (C, D, E and F), the current can only flow in one direction due to the use of fast recovery diode. Therefore, there are limitations for the selection of four switching states with unidirectional current path. This section describes the modulation strategy for the proposed 6S-5L-ANPC inverter.

The diagram of modulation for 6S-5L-ANPC inverter under reactive power operation is shown in Fig. 6. The Phase

Disposition (PD) pulse-width-modulation (PWM) scheme is used because of its lower THD [36].

In Fig. 6, four carriers and one reference signals are used for one phase of the inverter. By comparing each of the carriers with the reference, the corresponding switching states are switched and five-level output voltage waveform is generated. From Fig. 6, it is observed that during a complete grid line cycle, four operating zones can be identified based on the polarities of the output current and grid voltage: in Z1 and Z3, the output current and reference voltage are in opposite direction; in Z2 and Z4, the output current and reference voltage are in the same direction.

It is noted that both zero switching states (D and E) belong to unidirectional current path states. The selection of two redundant switching states which give zero output is based on the direction of output current. So from  $t_1$  to  $t_5$ , the current is positive and mode D is chosen. Similarly, from  $t_0$  to  $t_1$  and  $t_5$  to  $t_8$ , mode E is selected due to the negative output current.

Among two pairs of redundant states which output  $\pm 1$  level, states C (+1) and F (-1) allow unidirectional current-flow path. These two states can only be used when output voltage and current are in same direction. Therefore, under reactive power condition, when directions of current and voltage are different, only mode B (+1) and G (-1) can be used to achieve 1 output level.

##### A. Modulation in Z1 [from $t_0$ to $t_1$ ]

During this period, the output voltage level varies between +1 and 0. In this region, only mode B can be used to generate +1 output because voltage and current are in opposite direction. Therefore, the FC voltage cannot be regulated and it has always been discharged. For zero output, mode E is selected due to the negative current. So, the circuit rotates in the sequence of (B, E, B, E). The specific modulation in this region is shown in Fig. 7.

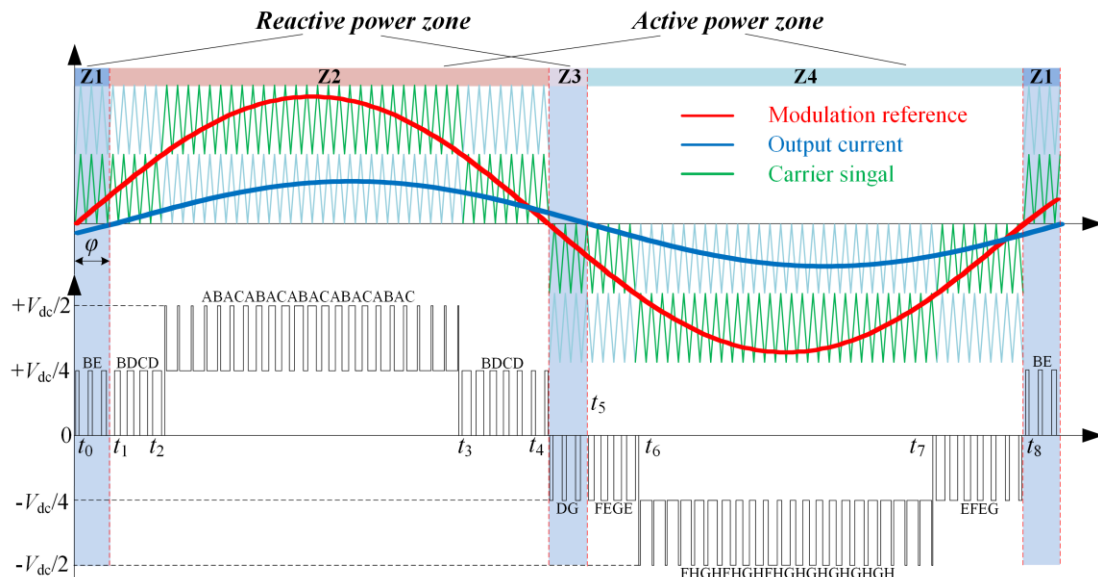


Fig. 6. PWM modulation for 6S-5L-ANPC inverter.

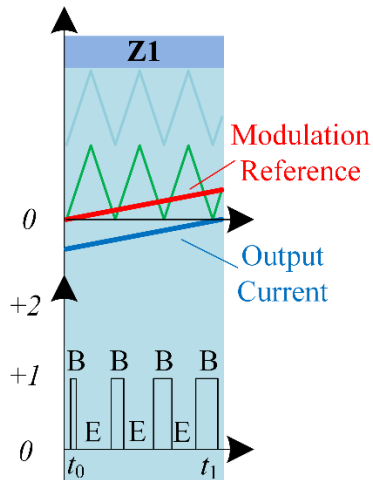


Fig. 7. PWM Modulation in Z1.

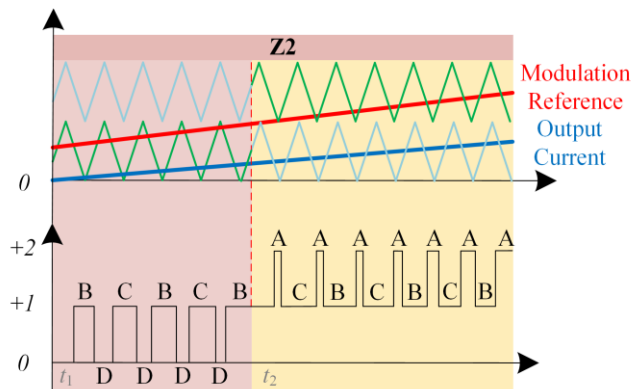


Fig. 8. PWM Modulation in Z2.

### B. Modulation in Z2 [From $t_1$ to $t_4$ ]

From  $t_1$  to  $t_2$  and  $t_3$  to  $t_4$ , the output voltage is also switched between +1 and 0. Both redundant +1 states (B, C) can be used, which gives an opportunity to regulate the voltage across FC. When actual FC voltage is lower than the reference value, charging state B is chosen; when greater than reference FC voltage, mode C is selected to discharge FC. When outputting zero voltage level, mode D is chosen. Consequently, the switching state sequence of (B, D, C, D) is achieved.

From  $t_2$  to  $t_3$ , the output reference voltage is between +2 and +1. Mode A is required to generate +2 output level. Similarly, appropriate selection of redundant switching states (B, C) leads to self-balancing of FC. In this way, sequence of (B, A, C, A) guarantees FC voltage balancing and inverter output. The modulation in Z2 is shown in Fig. 8.

### C. Modulation in Z3 [from $t_4$ to $t_5$ ]

In the capacitive power factor condition, the output current during  $t_4$  to  $t_5$  is positive. Therefore, modes D and G are selected to generate 0 and -1 output, so the circuit rotates in the sequence of (D, G).

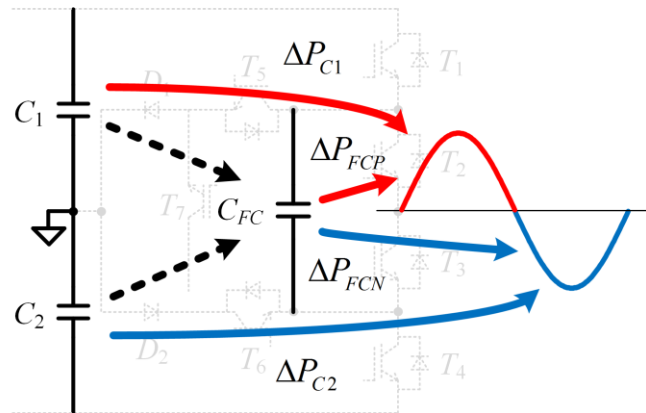


Fig. 9. Relationship of power transmission between DC capacitors, FC and output side during a whole grid cycle.

### D. Modulation in Z4 [From $t_5$ to $t_8$ ]

Similar to Z2, mode E and mode H are selected for zero and -2 output levels. When -1 voltage level is required, redundant switching states (F, G) are employed alternately to keep FC voltage balanced. Consequently, during  $t_5$  to  $t_6$  and  $t_7$  to  $t_8$ , switching state sequence (F, E, G, E) is achieved; from  $t_6$  to  $t_7$ , switching state sequence (F, H, G, H) is used.

### E. DC-link capacitor voltage balancing

The DC-link capacitor voltage balancing is one problem encountered in single-phase applications, which cannot be solved using three-phase technique such as adding zero-sequence voltage. For 5L-ANPC inverters, the output power in positive grid cycle is provided by upper side DC capacitor and FC; similarly, the lower DC capacitor and FC are transferring the energy to the output side during negative grid cycle. If the inverter is controlled to generate symmetrical output current, then the power relationship can be obtained

$$\Delta P_{C1} + \Delta P_{FCp} = \Delta P_{C2} + \Delta P_{FCn} \quad (1)$$

where  $\Delta P_{C1}$ ,  $\Delta P_{FCp}$  is the energy offered by  $C_1$  and FC in positive grid cycle respectively;  $\Delta P_{C2}$ ,  $\Delta P_{FCn}$  is the energy from  $C_2$  and FC in negative grid cycle respectively. The power transmission relationship is shown in Fig. 9.

It should be noted that the energy provided by FC ( $\Delta P_{FCp}$  and  $\Delta P_{FCn}$ ) also comes from DC-link capacitors (the dashed lines). Based on this, the regulation of DC-link capacitor voltages can be achieved by controlling the FC voltage: if  $V_{C1}$  is greater than  $V_{C2}$ , then in positive grid cycle  $C_1$  can be controlled to transfer more energy to FC and then during negative grid cycle FC is providing more energy to the output side so that  $C_2$  will output less power. Consequently, the voltage difference between two DC-link capacitors will be decreased. To control the FC voltage, this paper uses the control technique proposed in reference [27].

## V. FLYING CAPACITOR DESIGN

The role of FC in 6S-5L-ANPC inverter is to provide  $\pm 1$  output voltage levels. In addition to the modulation method which keeps the FC voltage balanced, selection of FC



capacitance which limits its voltage ripple is of equal importance to achieve a stable output voltage level. This section gives the parameter design of FC under unity power factor condition and reactive power operating condition, and the specific design will also be given.

### A. Unity power factor condition

Under unity power factor condition, the FC design is decided by its voltage ripple. As discussed earlier, the same charging time and discharging time during one grid period leads to self-balance of FC. Here, the charging time is used to calculate the FC voltage ripple. The modulation index  $M$  is assumed to be greater than 0.5 in consideration of high voltage utilization. Fig. 10 gives modulation of 6S-5L-ANPC during positive grid cycle. +2, +1C and +1D in Fig. 10 represent +2, +1 charging and +1 discharging output levels respectively.

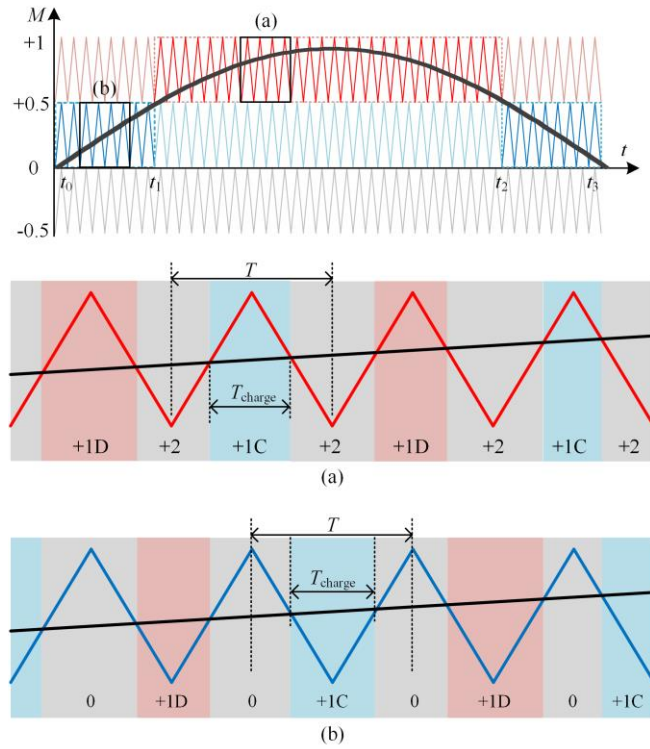


Fig. 10. 6S-5L-ANPC modulation in positive grid cycle. (a)  $M \cdot \sin\theta \geq 0.5$ . (b)  $M \cdot \sin\theta \leq 0.5$ .

From Fig. 10, it is obtained that the charging time of FC ( $T_{charge}$ ) during one switching cycle ( $T_s$ ) can be written as

$$\begin{cases} T_{charge} = \frac{2M \cdot \sin\theta}{f_s} & (M \cdot \sin\theta \leq \frac{1}{2}) \\ T_{charge} = \frac{2(1 - M \cdot \sin\theta)}{f_s} & (M \cdot \sin\theta \geq \frac{1}{2}) \end{cases} \quad (2)$$

where  $f_s$  is the switching frequency,  $\theta$  is the reference phase angle. From (2), it is obtained that when  $M \cdot \sin\theta \leq 0.5$ , the FC charging time function is increasing function; when  $M \cdot \sin\theta \geq 0.5$ , it is monotone decreasing function; and it reaches its peak value which is  $T_s$  when  $M \cdot \sin\theta = 0.5$ .

During the FC charging time  $T_{charge}$ , the FC voltage variation  $\Delta V_{fc}$  can be calculated using

$$\Delta V_{fc} = \frac{\Delta Q_{fc}}{C_{fc}} = \frac{I_{pk} \sin\theta \cdot T_{charge}}{C_{fc}} \quad (3)$$

where  $I_{pk}$  is the peak value of output current. According to (2) and (3), the FC voltage ripple can be written as

$$\begin{cases} \Delta V_{fc} = \frac{2I_{pk}}{C_{fc} f_s} \cdot M \cdot \sin^2\theta & (M \cdot \sin\theta \leq \frac{1}{2}) \\ \Delta V_{fc} = \frac{2I_{pk}}{C_{fc} f_s} \cdot (-M \cdot \sin^2\theta + \sin\theta) & (M \cdot \sin\theta \geq \frac{1}{2}) \end{cases} \quad (4)$$

The FC voltage ripple reaches its peak when  $\sin\theta = 1/(2M)$ . Therefore, the capacitance of FC can be calculated as follows

$$C_{fc} = \frac{I_{pk}}{2\Delta V_{fc} f_s M} \quad (5)$$

### B. Reactive power condition

For 6S-5L-ANPC inverter under reactive power operation, due to the limitation of redundant switching states selection, the FC voltage cannot be regulated in Z1 and Z3 in Fig. 6. According to the analysis earlier, it is observed that FC is continuously discharged in reactive power region. Thus the selected FC capacitance value should be large enough to keep the continuous voltage drop within an acceptable range (e.g. 5% of reference FC voltage). As shown in Fig. 6, due to the symmetry, the FC voltage drop in Z1 is the same as Z3, thus the FC voltage drop in Z1 is chosen for calculation. Fig. 11 shows the reactive power modulation of 6S-5L-ANPC inverter during positive grid cycle, and 0 and +1D in Fig. 11 represent zero and +1 discharging output states.

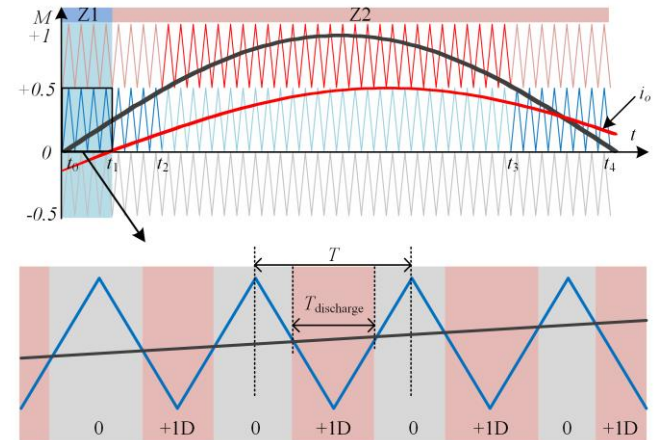


Fig. 11. 6S-5L-ANPC modulation in positive grid cycle under reactive power operating condition.

From Fig. 11, it is observed that in Z1, the output voltage varies between +1 (state B) and 0 (state E). The discharging time of FC ( $T_{discharge}$ ) during one switching cycle is given by

$$T_{discharge} = \frac{2M \sin\theta}{f_s} \quad (6)$$

During each discharging period, the electric charge variation of FC  $\Delta Q_{fc}$  is calculated according to

$$\Delta Q_{fc} = i \cdot T_{discharge} = \frac{2MI_{pk} \sin^2 \theta}{f_s} \quad (7)$$

To calculate the total electric charge of FC in Z1, the number of switching cycles N in Z1 is required, which is given by

$$N = \frac{\varphi}{2\pi} \cdot \frac{f_s}{f_{Line}} \quad (8)$$

where  $f_{Line}$  represents line frequency. The relationship of FC capacitance  $C_{fc}$ , voltage drop  $\Delta V_{fc}$  and electric charge  $\Delta Q_{fc}$  is then obtained

$$C_{fc} = \frac{\sum_{n=1}^N \Delta Q_{fc}}{\Delta V_{fc}} = \frac{2MI_{pk}}{\Delta V_{fc} \cdot f_s} \cdot \frac{\varphi}{2\pi} \cdot \frac{f_s}{f_{Line}} \cdot \sum_{n=1}^N \sin^2(n \cdot \frac{f_{Line}}{f_s} \cdot 2\pi) \quad (9)$$

For grid-connection application, there will be double line frequency ripple power in DC-link capacitors. With proper DC-capacitance selection, suitable output filter design and control method, the impact of double line frequency ripple power on the output current THD is small. Therefore, the impact of double line frequency ripple power on the FC value calculation can be ignored.

### C. Specific Design

As discussed before, the proposed topology is suitable for PV application. This part will give the specific design. For a 1 KVA PV grid-connected system: the grid voltage is 110 V<sub>RMS</sub>; DC voltage is 400 V; switching frequency is 15 KHz; modulation index is 0.78; the peak-to-peak FC voltage ripple is restricted within 2% of FC voltage. From the FC value calculation equation (5) in unity power factor condition, the calculated FC capacitance value is 275  $\mu$ F. And if the system is operating under 0.9 power factor condition, according to (9), a 3.6 V voltage drop is obtained.

Another case is: in 0.9 power factor condition, if the maximum FC voltage drop is 20 V, then based on (9) the calculated FC capacitance is 56  $\mu$ F. And FC with 56  $\mu$ F will lead to 10 V peak-to-peak voltage ripple in unity power condition. The simulation section will give the comparison results to show the impact of voltage drop on output current THD.

## VI. SIMULATION VERIFICATION

To verify the effectiveness of modulation strategy especially under reactive power condition as well as the FC capacitance calculation, computer simulation by MATLAB/Simulink has been carried out. The maximum power factor capability of 6S-5L-ANPC inverter is also provided. Based on the specific design in previous section, the simulation is conducted in two cases: a larger FC value and a smaller FC value. First, to limit the voltage ripple within 2% in unity power factor condition, the calculated FC value is 275  $\mu$ F and 310  $\mu$ F is chosen (part number: 947C311K102CBMS

used in experimental prototype). Then, to have 20 V voltage drop in 0.9 power condition, the calculated FC capacitance is 56  $\mu$ F. The system parameters are shown in Table V. Each DC-link capacitor is selected to be 2000  $\mu$ F to limit its voltage ripple within 15 V (= 15 V/200 V = 7.5%) according to reference [23].

TABLE V  
SYSTEM PARAMETERS

<b>Power</b>	1 KVA	<b>Grid Voltage (RMS value)</b>	110 V @ 60 Hz
<b>DC-link Voltage</b>	400 V	<b>Output Filter Inductance</b>	1.6 mH
<b>FC Capacitance</b>	310 $\mu$ F (947C311K102CBMS)	<b>Power Factor</b>	0.9 - 1
<b>DC Capacitance</b>	2000 $\mu$ F each	<b>Switching Frequency</b>	15 KHz

### A. Case I: Larger FC value

First, 310  $\mu$ F FC value is used for simulation. Fig. 12 gives the simulation results in unity power factor condition. Fig. 12 (a) shows the five-level inverter output. Fig. 12 (b) shows the FC voltage. It can be observed that the FC voltage is kept at  $V_{dc}/4$  which is 100 V. A small section of FC voltage waveform in Fig. 12 (b) is zoomed to show the voltage ripple. The measured peak-to-peak FC voltage ripple in this case is 1.8 V (= 1.8 V/100 V = 1.8%). Fig. 12 (c) shows the grid voltage and inverter output current. Under unity power factor, the current and voltage are in phase. The output current is sinusoidal wave without distortion. Fig. 12 (d) shows the measured output current THD which is 1.57%.

Simulation verification is also carried out under reactive power condition (PF= 0.9, capacitive). Fig. 13 shows the waveforms of inverter output voltage, FC voltage, grid voltage, output current and THD of output current. In Fig. 13 (b), it is observed that there is 3.4 V voltage drop in the reactive power region. However, this voltage drop occurs in the region near the zero-crossing point. Since the duty cycles of the output signal in this region are very small, the FC voltage drop has less impact on the output current THD, which is still 1.57%.

### B. Case II: Smaller FC value

To evaluate the impact of FC voltage drop on output harmonics, simulation has also been conducted under smaller FC value condition. The FC capacitance is selected to be 56  $\mu$ F according to (8) to achieve 20% FC voltage drop. Fig. 14 and Fig. 15 show the simulation results in unity power factor and reactive power factor (PF = 0.9) conditions respectively.

As can be observed in Fig. 14 (b), the peak-to-peak FC voltage ripple in unity power factor condition is increased to 10.3 V. The output current THD is still 1.57%, which is shown in Fig. 14 (d). Under 0.9 PF condition, the FC voltage drop is increased to 20 V, as shown in Fig. 15 (b), which verifies the FC design procedures. The output THD in Fig. 15 (d) is only increased by 0.03%, which is 1.60%.

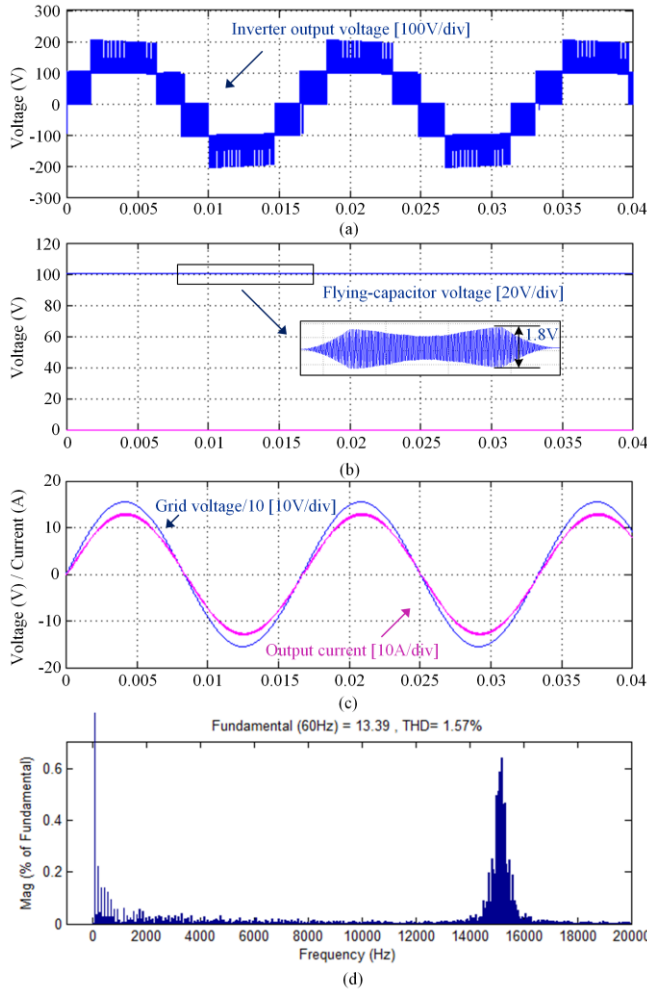


Fig. 12. Simulation results with 310  $\mu\text{F}$  FC value under unity power factor condition. (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

### C. Low switching frequency operation

From the analysis in Section III, it is concluded that the proposed topology is suitable for high power application whose system switching frequency is low (e.g. 2 KHz or lower). Therefore, it is important to evaluate its performance under low switching frequency operation. The switching frequency  $f_s$  in this case is selected to be 1.5 KHz. The FC value is 310  $\mu\text{F}$ , and the output filter value is unchanged.

Fig. 16 shows the simulation results when  $\text{PF} = 1$ . As can be observed from Fig. 16 (b), the FC voltage ripple is increased to 13 V due to low switching frequency according to (5). Fig. 17 shows the simulation results when  $\text{PF} = 0.9$ . The measured FC voltage ripple in this case is still 13 V, as shown in Fig. 17 (b). Therefore, the FC voltage ripple in both cases ( $\text{PF} = 1$  and 0.9) is decided by equation (5), which is the same as the conventional 5L-ANPC inverter topologies, so the output performance of proposed topology under low switching frequency condition is the same as that of conventional 5L-ANPC inverters.

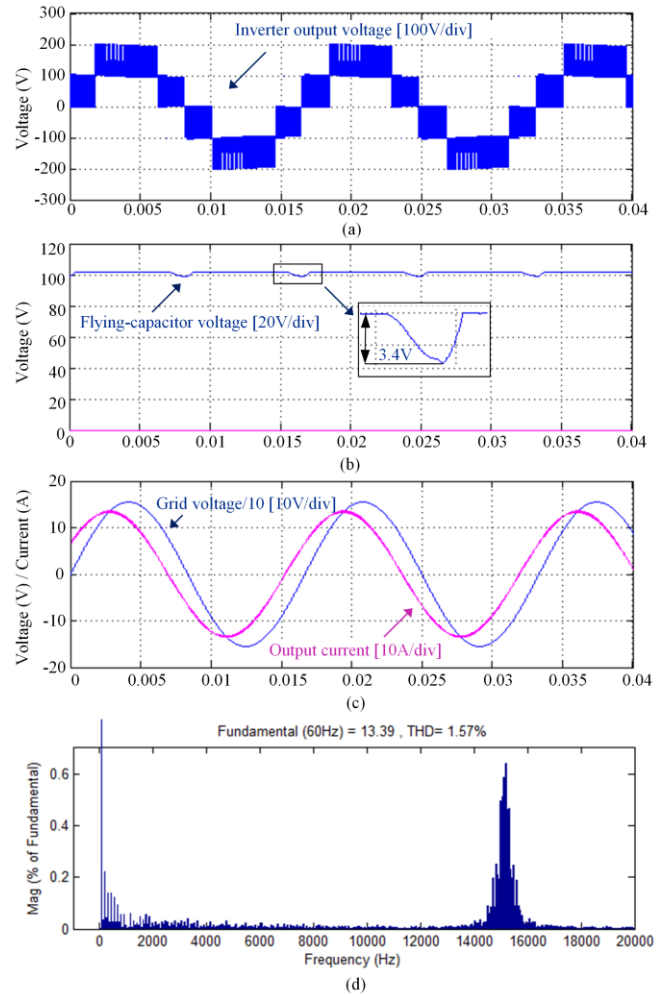


Fig. 13. Simulation results with 310  $\mu\text{F}$  FC value under reactive power operation ( $\text{PF} = 0.9$ ). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

### D. Maximum reactive power capability

Although the proposed topology is suitable for unity power factor operation, the functionalities of low-voltage ride-through (LVRT) and the grid support capability are required for the inverters at high power conversion, even for PV inverters. Therefore, inverters should be capable of injecting some reactive current when the grid presents a voltage sag fault. This part will discuss the maximum power factor capability of proposed topology.

For 6S-5L-ANPC inverter, there are FC voltage drops under reactive power condition. This FC voltage drop  $\Delta V_{fc}$  will increase the voltage stress of switches  $T_1$  and  $T_4$  by  $\Delta V_{fc}$ . In addition, even though the output current is compensated by closed-loop control, high FC voltage drop will cause output current distortion and then limit the maximum power factor capability of the system. Therefore, in consideration of device voltage stress and output performance, the FC voltage drop should be kept within a certain range for a proper system design. In this paper, the FC voltage drop is designed to be less than 15% of rated FC voltage ( $V_{DC}/4$ ).

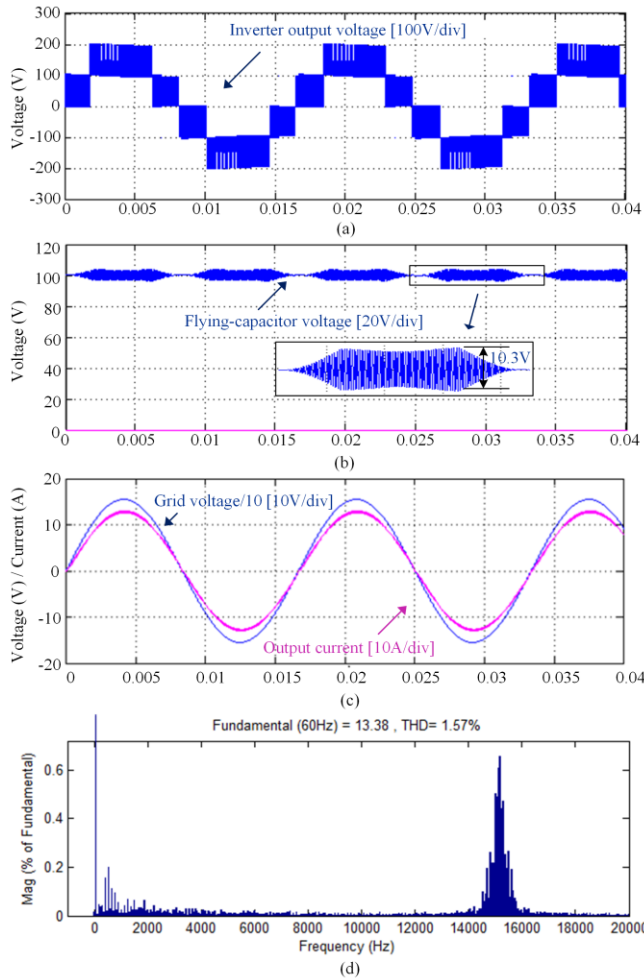


Fig. 14. Simulation results with 56  $\mu\text{F}$  FC value under unity power factor condition. (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

From FC capacitance calculation equation under reactive power condition (9), it is observed that the FC voltage drop value is influenced by FC capacitance, output current value and power factor. Additionally, with different modulation techniques, the impact of FC voltage drop on the output current performance is also different. Based on above analysis, it can be concluded that the maximum power factor capability of the system depends on the operation conditions. With the parameters selection in Table V (power level is 1 KVA and FC capacitance is 310  $\mu\text{F}$ ), if FC voltage drop  $\Delta V_{fc}$  is 15% of rated FC voltage which is 15 V, then based on equation (9) the calculated power factor is around 0.6. Fig. 18 (a) shows the simulation waveforms in this case. As can be observed, the output current THD is 1.65% which is closed to that under unity power factor condition (1.57%). The maximum power factor capability in this case is 0.6.

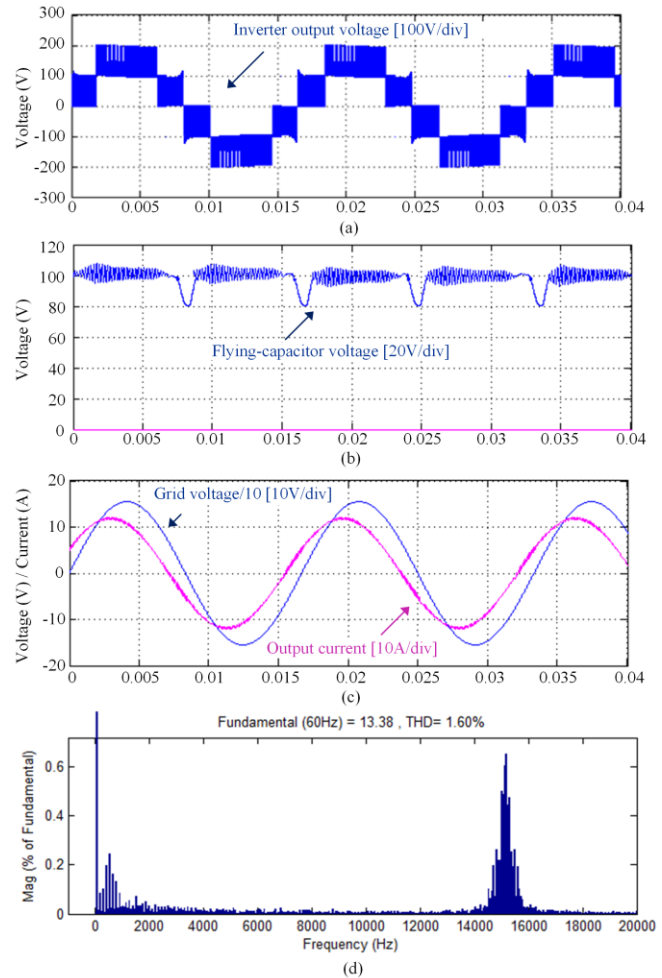


Fig. 15. Simulation results with 56  $\mu\text{F}$  FC value under reactive power operation (PF = 0.9). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current. (d) THD of output current.

When FC value is decreased to 56  $\mu\text{F}$ : based on (9), the calculated power factor is 0.8 to have 15 V FC voltage drop. The simulation result is shown in Fig. 18 (b). The measure output current THD is 1.63% which is also closed to the value in unity power factor condition. For the design requirement in this paper, the maximum power factor capability in this case is 0.8.

## VII. EXPERIMENTAL RESULTS

To verify the feasibility and advantages of the proposed topology and its modulation strategy, a 1 KVA single-phase 6S-5L-ANPC inverter grid-connected experimental prototype is designed and tested, as shown in Fig. 19. The system includes main circuit, DSP and FPGA control board, DC source, output filter and measurement instruments. The control board employs a combination of the Texas Instruments TMS320F28335 DSP chip and the Altera Cyclone IV EP4CGX22 FPGA card to provide powerful real-time mathematical calculations and control functions. The specifications for experiment are identical to the ones used in simulation section, which are shown in Table V.

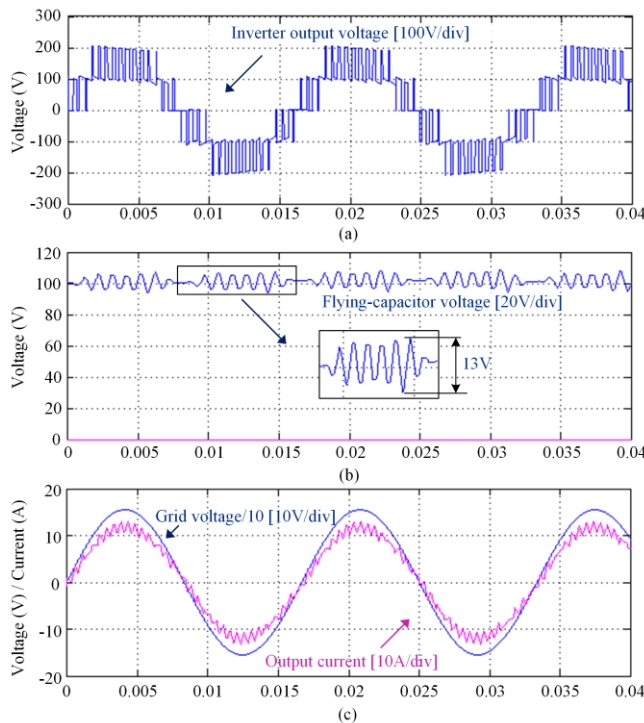


Fig. 16. Simulation results under low switching frequency operation (PF = 1). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current.

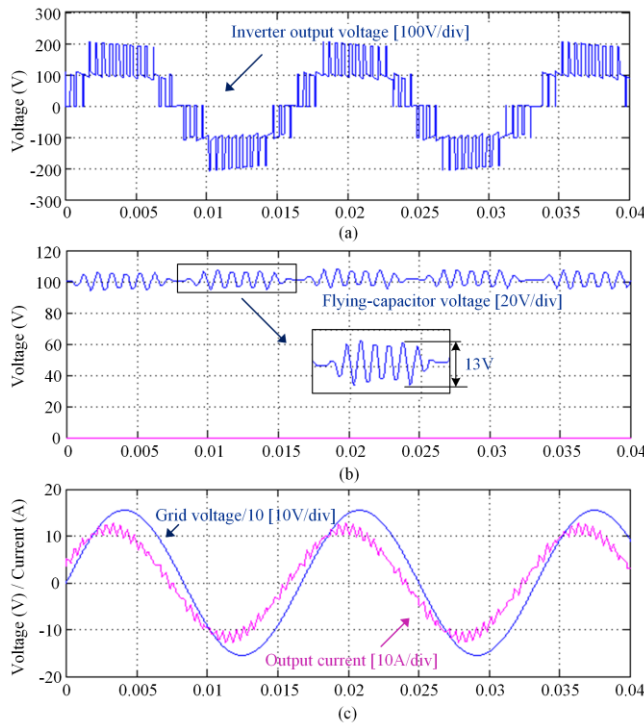


Fig. 17. Simulation results under low switching frequency operation (PF = 0.9). (a) Inverter output voltage. (b) FC voltage. (c) Grid voltage and inverter output current.

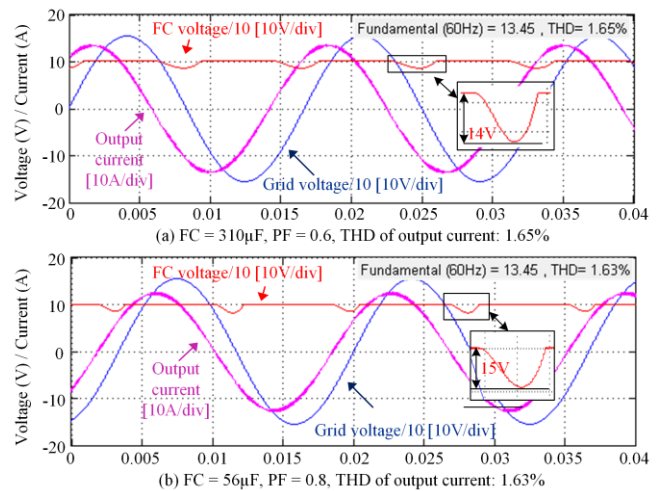


Fig. 18. Simulation results with 15% FC voltage drop using different FC value.

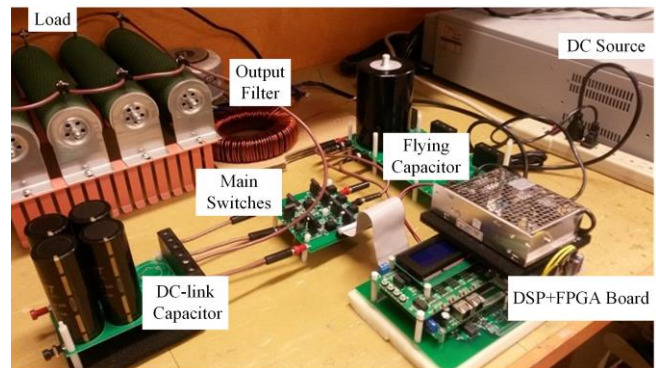


Fig. 19. Experimental prototype.

Fig. 20 and Fig. 21 show the experimental results under unity power factor condition. Fig. 20 shows inverter output voltage, FC voltage, grid voltage and output current: channel 1 is the output bridge voltage; channel 2 is 110V<sub>RMS</sub> grid voltage; channel 3 is the FC voltage, which is balanced at 100 V; channel 4 is the output current, which is sinusoidal without distortion and in phase with grid voltage in this case. The measured output current THD is 1.6%. In addition to the FC voltage and AC current waveforms, Fig. 21 also shows the voltages of two DC-link capacitors: channel 1 is lower DC-link capacitor voltage and channel 2 is upper DC-link capacitor voltage. The measured peak-to-peak FC voltage ripple is 2.1 V (= 2.1 V/100 V = 2.1%) and DC-link capacitor line-frequency voltage ripple is 12 V (= 12 V/200 V = 6%). The balanced FC and DC-link capacitors voltages verify the modulation method in active power condition.

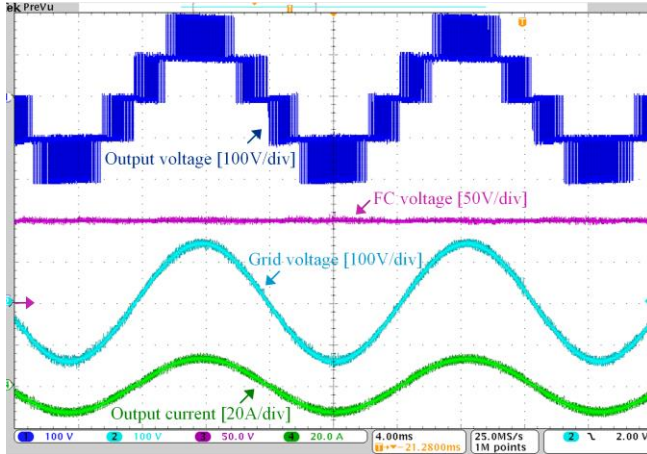


Fig. 20. Experimental results under unity power factor condition: waveforms of inverter output voltage, FC voltage, grid voltage and output current

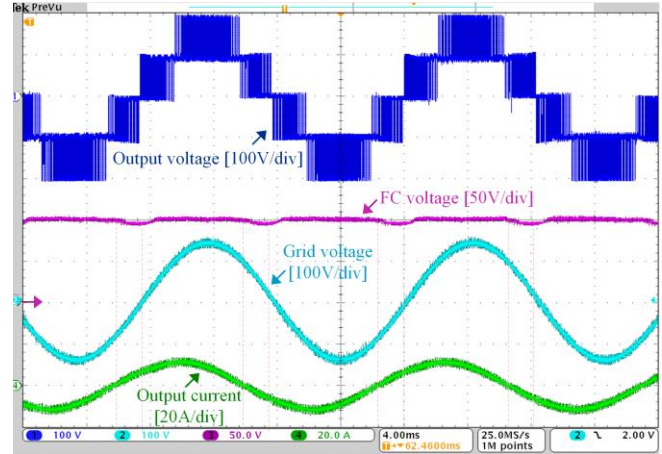


Fig. 22. Experimental results under reactive power operation (PF = 0.9, capacitive): waveforms of inverter bridge voltage, FC voltage, grid voltage and output current.

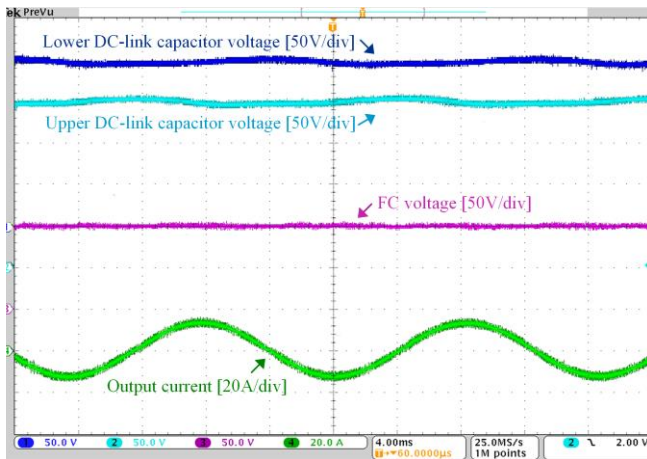


Fig. 21. Experimental results under unity power factor condition: waveforms of lower DC-link capacitor voltage, upper DC-link capacitor voltage, FC voltage and output current.

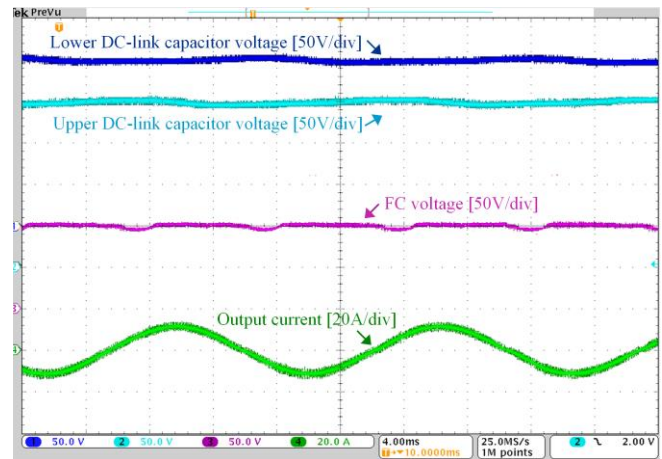


Fig. 23. Experimental results under reactive power condition (PF = 0.9, capacitive): waveforms of lower DC-link capacitor voltage, upper DC-link capacitor voltage, FC voltage and output current.

The reactive power operation mode is also tested. The power factor is selected to be 0.9 (capacitive). Fig. 22 and Fig. 23 show the experimental results.

In Fig. 22, channel 1 shows the five-step waveform of bridge voltage. Channel 3 shows the FC voltage waveform. As can be observed, the continuous FC voltage drop is 4 V ( $= 4 \text{ V}/100 \text{ V} = 4\%$ ). The grid voltage in channel 2 leads the inverter output current in channel 4 by 25 degrees because of 0.9 system power factor. In this situation, the inverter still produces good quality current waveform without distortion. The measured THD value of output current is still 1.6%.

Fig. 23 shows two DC-link capacitors voltages, FC voltage and output current. The DC-link capacitors voltages waveforms in this situation are almost the same as one under active power condition. The measured peak-to-peak DC-link capacitor ripple voltage is 11.4 V ( $= 11.4 \text{ V}/200 \text{ V} = 5.7\%$ ).

## VIII. CONCLUSION

In this paper, a novel 6S-5L-ANPC inverter topology has been proposed. As compared with the conventional 5L-ANPC inverter, it requires only 6 switches for single phase, a reduction from 8 switches. The operating principles and switching states are presented. The results of comparison between 6S-5L-ANPC and the conventional 5L-ANPC topologies show that 6S-5L-ANPC topology has lower conduction loss and thus higher efficiency in high power condition. The specific modulation strategy of 6S-5L-ANPC inverter under reactive power operation has been proposed. Issues related to the DC-link capacitors and FC voltages balancing and the maximum reactive power capability are discussed. The equations to calculate the FC capacitance value in active and reactive power conditions are provided. Computer simulation and experimental prototype based on a single phase 1KVA prototype have been carried out in both active and reactive power conditions to demonstrate the reliability of the proposed topology and modulation method.

## REFERENCE

- [1] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter / inverter topologies and applications," in *Proc. IPEC*, 2010, pp. 492–501.
- [2] J. Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Apr. 2002.
- [3] A. Sanchez-ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, "Medium voltage-high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1462–1476, Mar. 2012.
- [4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. W. Bin Wu, J. Rodriguez, M. a. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [5] J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [6] H. Abu-rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters — state of the industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.
- [7] G. Buticchi, D. Barater, E. Lorenzani, C. Concarì, and G. Franceschini, "A nine-level grid-connected converter topology for single-phase transformerless PV systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3951–3960, Aug. 2014.
- [8] J. C. Wu and C. W. Chou, "A solar power generation system with a seven-level inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3454–3462, Jul. 2014.
- [9] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, May 1981.
- [10] H. Wang, Y. Liu, and P. C. Sen, "A neutral point clamped multilevel topology flow graph and space NPC multilevel topology," in *Proc. IEEE ECCE*, 2015, pp. 3615–3621.
- [11] X. Kou, K. A. Corzine, and Y. L. Familiant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 979–987, Apr. 2004.
- [12] T. a. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Proc. IEEE 23rd PESC*, 1992, pp. 397–403.
- [13] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *Ind. Electron. IEEE Trans.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [14] J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," *Ind. Electron. IEEE Trans.*, vol. 58, no. 2, pp. 412–420, Feb. 2011.
- [15] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 37, no. 2, pp. 611–618, Feb. 2001.
- [16] L. M. Tolbert, "A Multilevel Modular Capacitor Clamped DC-DC Converter," in *Proc. 41st IAS*, 2006, pp. 966–973.
- [17] F. Zhang, S. Yang, F. Z. Peng, and Z. Qian, "A Zigzag Cascaded Multilevel Inverter Topology with Self Voltage Balancing," in *Proc. IEEE Appl. Power Electron. Conf.*, 2008, pp. 1632–1635.
- [18] G. Gateau, T. a. Meynard, L. Delmas, and H. Foch, "Stacked multicell converter (SMC): topology and control," *Eur. Power Electron. Drives J.*, vol. 12, no. 2, pp. 14–18, Feb. 2002.
- [19] Y. Kashihara and J. I. Itoh, "Performance evaluation among four types of five-level topologies using Pareto front curves," in *Proc. IEEE ECCE*, 2013, pp. 1296–1303.
- [20] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. 36th IEEE PESC*, 2005, pp. 2296–2301.
- [21] T. Brückner, S. Bernet, and H. Güldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Mar. 2005.
- [22] Y. Jiao and F. C. Lee, "New Modulation Scheme for Three-Level Active Neutral-Point-Clamped Converter With Loss and Stress Reduction," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5468–5479, Sep. 2015.
- [23] Y. Kashihara and J. I. Itoh, "Parameter design of a five-level inverter for PV systems," in *Proc. 8th IEEE ICPE ECCE*, 2011, pp. 1886–1893.
- [24] J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 961–972, Mar. 2011.
- [25] J. Li, A. Q. Huang, Z. Liang, and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 519–533, Feb. 2012.
- [26] L. A. Serpa, P. M. Barbosa, P. K. Steimer, and J. W. Kolar, "Five-level virtual-flux direct power control for the active neutral-point clamped multilevel inverter," in *Proc. IEEE PESC*, 2008, pp. 1668–1674.
- [27] H. R. Teymour, D. Sutanto, K. M. Muttaqi, and P. Ciuffo, "A novel modulation technique and a new balancing control strategy for a single-phase five-level ANPC converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1215–1227, Feb. 2015.
- [28] K. Wang, L. Xu, Z. Zheng, and Y. Li, "Capacitor voltage balancing of a five-level ANPC converter using phase-shifted PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1147–1156, Mar. 2015.
- [29] F. Kieferndorf, M. Basler, L. A. Serpa, J.-H. Fabian, A. Coccia, and G. A. Schauer, "ANPC-5L technology applied to medium voltage variable speed drives applications," in *SPEEDAM*, 2010, pp. 1718–1725.
- [30] T. B. Soeiro, R. Carballo, J. Moia, G. O. Garcia, and M. L. Heldwein, "Three-phase five-level active-neutral-point-clamped converters for medium voltage applications," in *Proc. COBEP*, 2013, pp. 85–91.
- [31] C. F. C. S. Gonzalez, M. I. Valla, "Five-level cascade asymmetric multilevel converter," *IET Power Electron.*, vol. 3, no. 11, pp. 120–128, Nov. 2010.
- [32] R. Solution, T. H. D. Minimization, J. Li, and A. Q. Huang, "An optimum PWM strategy for 5-level active NPC (ANPC) converter based on real-time solution for THD minimization," in *Proc. IEEE ECCE*, 2009, pp. 1976–1982.
- [33] S. R. Pulikanti, V. G. Agelidis, and A. A. Fc, "Hybrid flying-capacitor-based converter operated with SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4643–4653, Oct. 2011.
- [34] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.
- [35] H. Wang, L. Kou, Y. Liu, and P. C. Sen, "New low-cost five-level active neutral-point clamped converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2016, pp. 1489–1496.
- [36] V. G. Agelidis, "Non-deterministic AM-PWM strategy for three-phase VSI," in *Proc. 20th IECON*, 1994, pp. 73–78.



**Hongliang Wang** (M'12-SM'15) received the B.Sc. degree from Anhui University of Science and Technology, Huainan, China in 2004, and received the Ph.D. degree from Huazhong University of Science and Technology, Wuhan, China in 2011.

From 2004 to 2005, he worked as an electrical engineer of Zhejiang Hengdian Thermal Power Plant. From 2011 to 2013, he worked as a senior system engineer of Sungrow Power Supply Co., Ltd. He is a Post-Doctoral Fellow at Queen's University since 2013.

His research in the area of power electronics, including digital control, modulation and multilevel topology of inverter for photovoltaic application and micro-grids application; resonant converters and server power supplies, and LED drivers. He has published more than 40 papers in conferences and journals. He is the inventor/co-inventor of 41 China issued patents, 13 US pending patents and 4 PCT pending patents.

Dr. Wang is currently a senior member of China Electro-Technical Society (CES); a senior member of China Power Supply Society (CPSS). He serves as a member of CPSS Technical Committee on Standardization; a member of CPSS Technical Committee on Renewable Energy Power Conversion; a vice-chair of Kingston Section, IEEE; a session chair of ECCE 2015; a TPC member of ICEMS2012; a China Expert Group Member of IEC standard TC8/PT 62786.



**Lei Kou** (S'15) received the B.S and M.S degree in electrical engineering from Hunan University, Changsha, Hunan, China in 2010 and 2013 respectively. He is current is working toward the Ph.D. degree in power electronics at Queen's University, Kingston, Ontario, Canada.

His current research interests include digital control techniques, modulation strategies, topology research of multilevel converters and renewable energy systems.



**Yan-Fei Liu** (M'94-SM'97-F'13) Dr. Liu received his PhD degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994. From February 1994 to July 1999, he worked as a Technical Advisor with the Advanced Power System Division of Nortel Networks. Since 1999, he joined Queen's University. Currently, he is a Professor in the

Department of Electrical and Computer Engineering. His research interests include digital control technologies for high efficiency, fast dynamic response dc-dc switching converter and ac-dc converter with power factor correction, resonant converters and server power supplies, and LED drivers. Dr. Liu holds 22 US patents and has published more than 170 technical papers in IEEE Transactions and conferences. He is also a principal contributor for three IEEE standards.

Dr. Liu serves as an Editor of IEEE Journal of Emerging and Selected Topics of Power Electronics (IEEE JESTPE) since 2012, an associate Editor for IEEE Transactions on Power Electronics since 2001, an Editor in Chief for special issue of Power Supply on Chip of IEEE Transactions on Power Electronics from 2011 to 2013. He also served as Guest Editor for special issues of JESTPE: Minutization of Power Electronics Systems, as well as Green Power Supplies. He also served as Co-General Chair of ECCE 2015. He has been the chair of PELS Technical Committee on Control and Modeling Core Technologies since 2013 and chair of PELS Technical Committee on Power Conversion Systems and Components from 2009 to 2012.



**Paresh C. Sen** (M'67 – SM'74 – F'89 – LF'04) was born in Chittagong, Bangladesh. He received the B.Sc. (with honors in physics) and M.Sc. (Tech.) degrees in applied physics from the University of Calcutta, West Bengal, India in 1958 and 1962, respectively, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, Ontario, Canada, in 1965 and 1967,

respectively.

Dr. Sen is currently Emeritus Professor of Electrical and Computer Engineering at Queen's University, Canada. He has worked for industries in India and Canada and was a consultant to electrical industries in Canada. He has authored over 215 technical papers in the general area of electric motor drives and power electronics. He is the author of two internationally acclaimed textbooks: *Principles of Electric Machines and Power Electronics* (Wiley 1989, 1997, 2013) and *Thyristor DC Drives* (Wiley 1981). He has taught electric machines, power electronics and electric drive systems for over 45 years. His fields of interest include power electronics, electric drive systems, switching power supplies, wind energy systems, digital control, and modern control techniques for power electronics and motor drive systems.

Dr. Sen has served IEEE in various capacities: as an associate editor, distinguished lecturer, chairman of the technical committees on power electronics and energy systems, session organizer, session chairperson and paper reviewer. He served as an NSERC (Natural Science and Engineering Research Council of Canada) Scientific Liaison Officer evaluating university-industry coordinated projects.

Dr. Sen is globally recognized as an authority in power electronics and motor drive systems. He received the IEEE-IAS (Industry Application Society) Outstanding Achievement Award in 2008, and the IEEE-Canada Outstanding Engineering Educator Award in 2006 for his outstanding contributions over four decades as a researcher, supervisor, teacher, author and consultant. Dr. Sen received the IAS-IDC Prize Paper Award in 1986. He is a fellow of IEEE and a fellow of EIC. As an Emeritus Professor, Dr. Sen continues to be active in research, supervision of graduate students and in several IEEE societies.