Low Leakage Clock Tree With Dual-Threshold-Voltage Split Input–Output Repeaters

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***Abstract*— Leakage power consumption of clock distribution networks (CDNs) is an important challenge in modern synchronous integrated circuits with billions of deeply scaled transistors. Multithreshold CMOS technology is commonly used to provide power reduction in standby mode while maintaining high performance in active mode. In this paper, a novel dual-threshold-voltage repeater circuit with split inputs–outputs (SPLIT-IOs) is employed for suppressing leakage currents in gated CDNs. Three floor planning strategies are considered for clock distribution across the chip with signal transition times of less than or equal to 50 ps at the leaves. Depending on the power supply voltage and floor plan, the standby leakage power consumption is reduced by 50.36%–78.43% with the proposed clock tree with SPLIT-IO repeaters as compared to the conventional three-level H-tree in a 45-nm CMOS technology. The spread of standby leakage power due to process variations is compressed by 36.72%–73.77% with the proposed clock tree as compared to the standard network. The proposed circuit technique significantly lowers the total energy consumption of partially active networks with local clock gating as well. The energy savings provided by the SPLIT-IO buffers are enhanced with the scaling of power supply voltage and frequency in synchronous systems-on-chip.**

***Index Terms*— H-tree, multithreshold CMOS, process parameter fluctuations, split input–output (SPLIT-IO) repeater, synchronous integrated circuits.**

I. Introduction

SYNCHRONOUS clocking is the common strategy for timing of data storage and processing events in digital integrated circuits [1], [6], [10]. A global clock signal is transmitted across an integrated circuit with a network of buffers and wires [1]. Clock signal typically drives the largest capacitive load at the leaves and oscillates with the highest frequency in an integrated circuit. The clock distribution network (CDN) typically consumes the largest portion of overall chip power [6], [10]. In some specialized synchronous circuits such as field-programmable gate arrays, clock network may contribute up to 70% of the total power consumption [3]. Higher power consumption results in shorter battery lifetime, exacerbated cooling challenges, degraded reliability, and increased packaging cost in integrated circuits [4], [5].

Manuscript received October 3, 2018; revised January 28, 2019; accepted February 9, 2019. *(Corresponding author: Anil Kumar Gundu.)*

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Digital Object Identifier 10.1109/TVLSI.2019.2902215

Overall power consumption of a CDN is due to leakage currents, dynamic switching activity on parasitic capacitors, and short-circuit currents [3], [5]. Majority of prior studies address the issue of high-dynamic switching power consumption in high-frequency synchronous integrated circuits [2], [6]–[10]. The switching power consumption ($CV_{DD}^2 f$) can be suppressed by lowering the capacitive load (C), power supply voltage (V_{DD}), and switching frequency (f) of a CDN [2], [6]–[10]. Clock gating (or conditional clocking) reduces the switching power by masking off clock signal whenever the branches of a local clock tree are idle [9], [11].

Leakage currents are produced by subthreshold conduction, gate insulator tunneling, and junction tunneling in MOSFETs [5]. Leakage currents cause significant power consumption in modern integrated circuits with deeply scaled transistors [14]. Subthreshold leakage currents are typically the primary source of power consumption in idle circuits [4]. The leakage power consumption may exceed the dynamic power consumption, thereby dominating the total power consumption of even active integrated circuits depending on the supply voltage and frequency of operation [4], [7], [13]–[16], [26], [27]. Novel circuit techniques that can suppress leakage currents are therefore desirable.

Static CMOS inverters are typically used as repeaters for driving long interconnections along a conventional clock tree path [1]–[3], [6], [8]–[11], [17]–[20]. Leakage currents could be suppressed with supply voltage scaling, device threshold voltage (V_t) tuning, gate length optimization, and transistor stack effect [4], [5]. The clock frequency is however degraded if these leakage suppression techniques are applied to a CDN. Specialized leakage reduction techniques that do not cause a significant increase in silicon area or degradation of switching frequency/signal slew rate are highly desirable for achieving compact, high-performance, and power-efficient CDNs.

A triple-threshold-voltage (tri-V_t) buffer offering high switching speed and lower leakage power is discussed in [18]. A dual-threshold-voltage (dual-V_t) repeater circuit with two split inputs–outputs [(SPLIT-IOs) cell] for low leakage and high frequency clocking is presented in [21]. Leakage currents in a SPLIT-IO repeater are suppressed without degrading the speed performance by employing multi-V_t transistors [18], [21].

In this paper, a novel low leakage and high frequency CDN with SPLIT-IO repeaters is presented. The proposed CDN consumes lower leakage power as compared to the conventional CDN designed with identical clock frequency and signal transition time requirements. A closed-form formula

for the propagation delay of a SPLIT-IO repeater is derived. Dependence of the SPLIT-IO repeater propagation delay on various parameters such as the sizes of devices and wires is presented supported by the experimental data. A simplified rule of thumb to determine the size of a SPLIT-IO repeater for achieving the minimum propagation delay is provided in this paper.

Three floor plan strategies are elucidated with a symmetrical SPLIT-IO H-tree network and compared with the conventional H-tree network where standard static CMOS inverters are used as repeaters. The minimum operating voltage of a clock tree is determined for achieving the lowest active power consumption while satisfying the clock frequency and signal transition time requirements at the leaves (10% of clock cycle time). The mechanism of leakage power reduction with the SPLIT-IO clock tree is presented. The influences of leakage currents on total energy consumption of SPLIT-IO and conventional clock trees are evaluated at various operating voltages and frequencies. In typical synchronous systems-on-chip, most of the circuit blocks tend to be idle/unused during the normal operation, thereby providing opportunities for lowering energy consumption with local clock gating. The significant energy savings provided by the proposed low-leakage buffers are demonstrated with various clock gating scenarios in partially active CDNs.

This paper is organized as follows. The operation of dual-V_t SPLIT-IO repeater is described in Section II. Transistor size optimization of SPLIT-IO circuit for achieving the minimum propagation delay is discussed in Section III. Floor planning strategies for the CDNs are presented in Section IV. The power and energy consumption of SPLIT-IO CDN are compared with a conventional CDN for various floor planning strategies, power supply voltages, clock frequencies, and local clock gating scenarios in Section V. The impact of process parameter fluctuations on the electrical characteristics of the new CDN is presented. The conclusions are in Section VI.

II. Low-Power Dual-V_t Split-IO Repeaters

A novel dual-V_t SPLIT-IO cell is proposed for low-leakage buffer design in [18]. A pair of pMOS transistors (P_1 and P_2) and a pair of nMOS transistors (N_1 and N_2) are employed in the SPLIT-IO cell, as shown in Fig. 1(a). Unlike a conventional static CMOS inverter [Fig. 1(b)], a SPLIT-IO cell has two inputs and two outputs. The two pMOS transistors P_1 and P_2 are driven by the first input pMOS-IN. Alternatively, the two nMOS transistors N_1 and N_2 are driven by the second input nMOS-IN.

The SPLIT-IO cell has two outputs called PHASE 1 and PHASE 2. The PHASE1 output is connected to the drains of P_1 and N_1. The PHASE2 output is connected to the drains of P_2 and N_2. P_1, P_2, N_1, and N_2 have different threshold voltages to tradeoff circuit speed with power consumption [18]. The threshold voltages of the high threshold voltage (HVT), standard threshold voltage (SVT), and low threshold voltage (LVT) transistors are listed in Table I. A 45-nm CMOS technology is used in this paper. Connections of a chain of three SPLIT-IO repeaters are shown in Fig. 1(d).

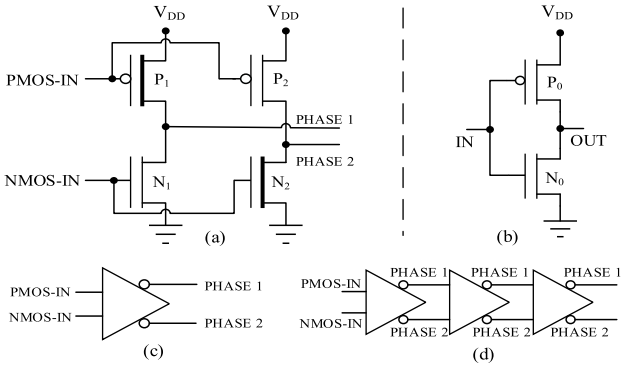

Fig. 1. Novel repeater with SPLIT-IOs [18]. (a) Structure of SPLIT-IO repeater. Thick line in channel area: HVT transistors. Thin line: SVT transistors. (b) Structure of conventional static CMOS inverter-based repeater with SVT transistors. (c) Symbol of SPLIT-IO repeater. (d) Connections in a chain of three SPLIT-IO repeaters.

TABLE I
Transistor Threshold Voltages

	HVT	SVT	LVT
PMOS V_t (mV)	-506.62	-390.71	-278.13
NMOS V_t (mV)	482.70	363.60	230.81

*Threshold voltages are extracted at V_{DD} = 1V using the technique presented in [19]. T = 27°C.

PHASE1 and PHASE2 outputs of a SPLIT-IO repeater are connected to the pMOS-IN and nMOS-IN, respectively, of the subsequent SPLIT-IO repeater along a clock path, as illustrated in Fig. 1(d).

The operation of the novel CDN is illustrated with the clock path that is shown in Fig. 2. A global clock signal CLK_IN is applied to the merged inputs (pMOS-IN and nMOS-IN) of the first-stage SPLIT-IO repeater B1 in the novel CDN. The incoming single-phase clock signal is split into two separate clock signals at the outputs of the first SPLIT-IO repeater B1, as shown in Fig. 2. The first phase of the split clock signal is produced by the PHASE1 output of B1. The second phase of split clock signal is produced by the PHASE2 output of B1. The two split phases of clock signals are transmitted in parallel by a chain of SPLIT-IO repeaters.

When CLK_IN transitions from 0 to 1, the PHASE1 and PHASE2 outputs of B1 transition from 1 to 0, as illustrated in Fig. 3. SVT N_1 produces higher discharging current as compared to HVT N_2. PHASE1 output transitions to 0 earlier as compared to PHASE2. The leading negative edge of the split clock signal is thereby produced by the PHASE1 output of B1. The pMOS transistors (P_3 and P_4) of B2 are turned on. The PHASE2 output of B1 is subsequently discharged. N_3 and N_4 in B2 are cutoff with the lagging negative edge of the split clock signal on the PHASE2 output of B1.

SVT P_4 produces higher charging current as compared to HVT P_3 in B2. The leading positive edge of the split clock signal is thereby produced by the PHASE2 output of B2. The nMOS transistors (N_5 and N_6) of the following repeater B3 are turned on with high speed. The leading negative edge of the split clock signal is thereby transferred to the

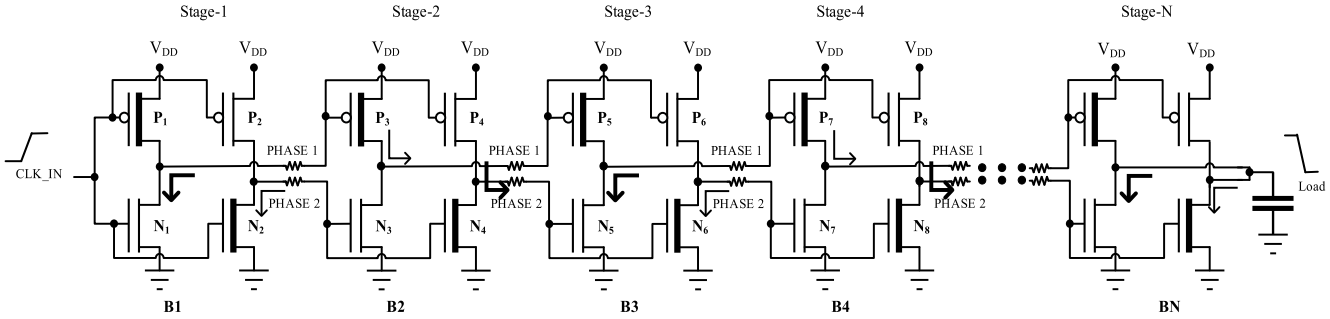

Fig. 2. Signal propagation along a chain of SPLIT-IO repeaters. Leading (high-speed) clock signal propagation path is highlighted with bold arrows. Lagging (weak) clock signal propagation path is shown with thin arrows.

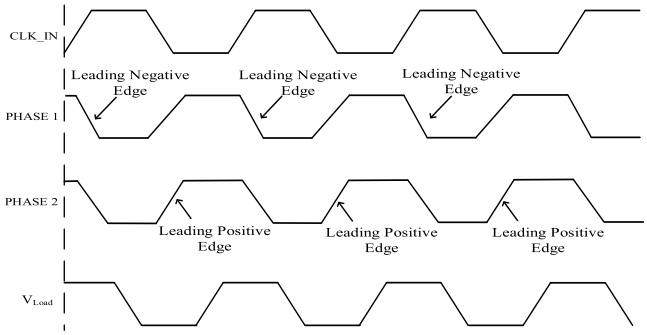

Fig. 3. Waveforms of the clock signals produced with a chain of SPLIT-IO repeaters.

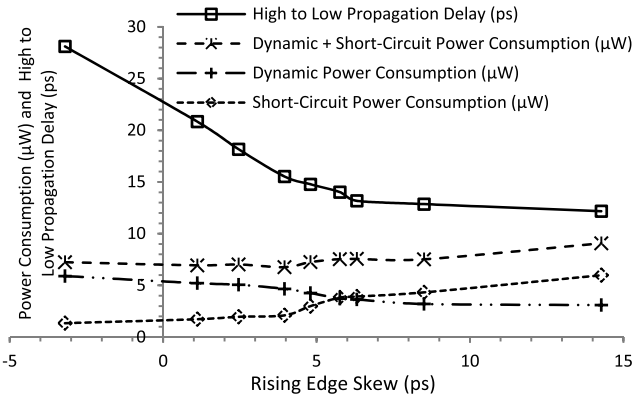

Fig. 4. Tradeoff between short-circuit power consumption and dynamic power consumption with the rising edge skew of pMOS-IN and nMOS-IN for various SPLIT-IO buffer template sizes at $V_{DD} = 1$ V. Similar tradeoff exists for the falling edge skew as well.

PHASE1 output of B3. Following the high-to-low transition of PHASE1 output of B3, the leading positive edge of the split clock signal is transferred to B4 and continues to propagate on the PHASE2 output of B4. This way, after the positive edge of the incoming single-phase clock signal CLK_IN, the leading negative edges of the split clock signals are produced and propagated by the PHASE1 outputs of the odd numbered repeater stages $(1, 3, 5\ldots)$ in the clock tree. Alternatively, the leading positive edges of the split clock signals are produced and propagated by the PHASE2 outputs of the even numbered repeater stages $(2, 4, 6\ldots)$ in the clock tree.

Similarly, after the negative edge of the incoming single-phase clock signal CLK_IN, the leading positive edges of the split clock signals are produced and propagated by the PHASE2 outputs of the odd numbered repeater stages in the clock tree. The leading negative edges of the split clock signals are produced and propagated by the PHASE1 outputs of the even numbered repeater stages. In the final stage that drives the clocked circuit elements, the repeater outputs (PHASE1 and PHASE2) are merged as shown in Fig. 2.

In a CDN, the wire capacitance is typically more significant as compared to the capacitance of transistors that are attached to the outputs of a SPLIT-IO repeater. SVT P_2 and N_1 are sized for achieving the transition time requirements of the leading clock edges with the smallest possible area and lower active power consumption. Short-circuit currents depend on the sizes of transistors (P_1, P_2, N_1, and N_2) and the skew between the arrival times of the two inputs (pMOS-IN and nMOS-IN) in a SPLIT-IO repeater as shown in Fig. 4. Short-circuit currents affect the clock signal transition time, propagation speed, and active power consumption. The skew between PHASE1 and PHASE2 is reduced by enlarging the widths of HVT devices P_1 and N_2 for the fixed sizes of SVT P_2 and N_1 of a SPLIT-IO repeater. The short-circuit current that is produced by the SPLIT-IO repeater is decreased by lowering the skew between the arrival times of inputs. A smaller skew between the arrival times of pMOS-IN and nMOS-IN, however, requires increasing the sizes of HVT transistors. Dynamic switching power consumption and propagation delay are increased due to the higher capacitance of larger HVT transistors as shown in Fig. 4. The SPLIT-IO repeaters are optimized to achieve the maximum switching speed with the minimum power consumption.

III. Size Optimization of Split-IO Repeaters

A chain of uniform repeaters is inserted into a long interconnection to enhance the signal propagation speed and slew rate in a CDN [9]. As a case study, five SPLIT-IO repeaters that are inserted into a long interconnection wire are shown in Fig. 5. The wires between two adjacent repeaters have length $= L_w$ and width $= W_w$. SPLIT-IO repeaters are based on a cell template. The transistors in the template are sized ($W_{N1} = 120$ nm, $W_{N2} = 150$ nm, $W_{P1} = 380$ nm, $W_{P2} = 220$ nm) to achieve the minimum power consumption (dynamic switching + short-circuit power) by adjusting the

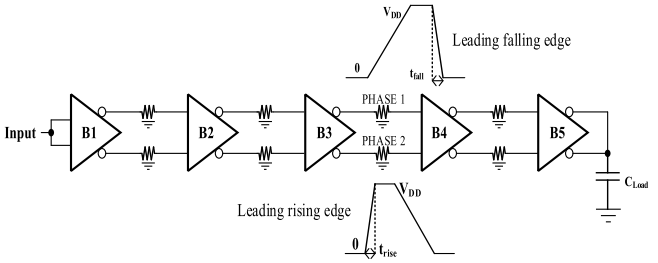

Fig. 5. SPLIT-IO cells in a five-stage repeater chain. The wires between repeaters have length $= L_w$ and width $= W_w$. The repeaters are S times larger than the SPLIT-IO cell template. S is an optimization parameter for achieving minimum delay.

skew between PHASE 1 and PHASE 2 signals. All transistors have a gate length of 40 nm ($L_{\text{pMOS}} = L_{\text{nMOS}} = L_{\min} =$ 40 nm).

PHASE1 and PHASE2 wires between B3 and B4 are insensitive to both the transition time of the ideal input signal of the first stage repeater B1 (Input) and the load capacitance of the last stage repeater B5 (C_{Load}). The PHASE1 and PHASE2 outputs of B3 are, therefore, the wires-under-test in this section. The signal propagation delay of the SPLIT-IO repeater in the third stage (B3) is evaluated with the Elmore delay model. The wires are modeled with n identical segments. The resistance and capacitance of each segment ($W_{\text{seg}} = W_w$ and $L_{\text{seg}} = L_w/n$) are R_{seg} and C_{seg}, respectively.

The leading falling edge of the split clock signals is produced by the PHASE1 output of B3, as shown in Fig. 2. The high-to-low propagation delay (τ_{HL}) of the SPLIT-IO repeater B3 is measured from the 50% of nMOS-IN low-to-high transition to the 50% of PHASE1 high-to-low transition. PHASE1 is discharged by SVT N_5 in B3, as shown in Fig. 2. R_{Driver} is the equivalent resistance of N_5 (R_{N5}) for the estimation of high-to-low propagation delay of B3. $C_{P5} + C_{N5}$ is the total intrinsic capacitance at the PHASE1 output of B3. $C_{P\text{Load}}$ is the fan-out capacitance of the PHASE1 output of B3. $C_{P\text{Load}}$ is the total gate capacitance of P_7 and P_8 in B4.

The leading rising edge of the split clock signals is produced by the PHASE2 output of B3. The low-to-high propagation delay (τ_{LH}) is measured from the 50% of pMOS-IN high-to-low transition to the 50% of PHASE2 low-to-high transition in the SPLIT-IO repeater B3. PHASE2 is charged by SVT P_6 in B3. R_{Driver} is the equivalent resistance of P_6 (R_{P6}) for the estimation of low-to-high propagation delay of B3. $C_{P6} + C_{N6}$ is the total intrinsic capacitance at the PHASE2 output of B3. $C_{N\text{Load}}$ is the fan-out capacitance of the PHASE2 output of B3. $C_{N\text{Load}}$ is the total gate capacitance of N_7 and N_8 in B4.

The Elmore delay (τ) of B3 is

$$\begin{aligned}\tau &= R_{\text{driver}}(C_P + C_N) + C_{\text{seg}}(R_{\text{driver}} + R_{\text{seg}}) + C_{\text{seg}}(R_{\text{driver}} \\ &\quad + 2R_{\text{seg}}) + \ldots + (C_{\text{seg}} + C_{\text{Load}})(R_{\text{driver}} + nR_{\text{seg}}) \\ &= nR_{\text{driver}}C_{\text{seg}} + nR_{\text{seg}}C_{\text{Load}} + R_{\text{driver}}(C_P + C_N + C_{\text{Load}}) \\ &\quad + \frac{n(n+1)}{2}R_{\text{seg}}C_{\text{seg}}. \end{aligned} \tag{1}$$

The average of high-to-low (τ_{HL}) and low-to-high (τ_{LH}) Elmore delays is given in (2), as shown at the bottom of this page.

The transistors in SPLIT-IO repeaters are $S(S \geq 1)$ times larger than the SPLIT-IO cell template in this optimization study. If S is too small, R_{P6} and R_{N5} become too large. Hence, P_6 and N_5 cannot produce sufficient currents for output switching. Alternatively, if S is too large, the delay is primarily determined by the input and output capacitors of the repeaters rather than the wires. The propagation delay is increased due to the higher parasitic capacitance of larger repeaters. An optimum repeater size that provides the shortest signal propagation delay exists. The repeater size (S) is the optimization parameter in this paper.

R_{P6} and R_{N5} are inversely proportional to S. Alternatively, C_{P5}, C_{P6}, C_{N5}, C_{N6}, $C_{P\text{Load}}$, and $C_{N\text{Load}}$ are proportional to S. The term represented at the bottom of the next page is independent of S in (2), where $n(n+1)R_{\text{seg}}C_{\text{seg}}$ is a constant. The optimum repeater size is achieved when

$$\frac{d\tau}{dS} = \frac{d(n(R_{P6} + R_{N5})C_{\text{seg}} + nR_{\text{seg}}(C_{P\text{Load}} + C_{N\text{Load}}))}{2dS} = 0 \tag{3}$$

which is equivalent to

$$\begin{aligned}&\frac{1}{2}nC_0\frac{W_{\text{seg}}}{1\ \mu\text{m}}\frac{L_{\text{seg}}}{1\ \mu\text{m}}\frac{d(R_{P6} + R_{N5})}{dS} \\ &\qquad + \frac{1}{2}nR_0\frac{L_{\text{seg}}}{W_{\text{seg}}}\frac{d(C_{P\text{Load}} + C_{N\text{Load}})}{dS} = 0 \end{aligned} \tag{4}$$

where W_{seg} and L_{seg} are the width and the length of each wire segment, respectively. C_0 is the capacitance of a wire with the width and the length of 1 μm. R_0 is the resistance of a wire with the width and the length of 1 μm. Assuming $R_{P6} = R_{P\text{-unit}}/S$, $R_{N5} = R_{N\text{-unit}}/S$, and $C_{P\text{Load}} + C_{N\text{Load}} = S \times C_{\text{in-unit}}$, the optimum repeater size is

$$S_{\text{optimum}} = \sqrt{\frac{C_0(R_{P\text{-unit}} + R_{N\text{-unit}})}{R_0 C_{\text{in-unit}}}} \cdot \frac{W_{\text{seg}}}{1\ \mu\text{m}} \tag{5}$$

where $R_{P\text{-unit}}$ and $R_{N\text{-unit}}$ are the resistances of SVT pMOS and nMOS transistors, respectively, in the SPLIT-IO template. $C_{\text{in-unit}}$ is the input capacitance of the SPLIT-IO cell template. The optimum S is independent of the number of wire segments (n), the length of each wire segment (L_{seg}), and the length of the buffered wire ($L_w = n \times L_{\text{seg}}$), as given by (5).

$$\begin{aligned}\tau = \frac{\tau_{\text{HL}} + \tau_{\text{LH}}}{2} &= \frac{n(R_{P6} + R_{N5})C_{\text{seg}} + nR_{\text{seg}}(C_{P\text{Load}} + C_{N\text{Load}}) + n(n+1)R_{\text{seg}}C_{\text{seg}}}{2} \\ &\quad + \frac{(R_{P6})(C_{P6} + C_{N6} + C_{N\text{Load}}) + R_{N5}(C_{P5} + C_{N5} + C_{P\text{Load}})}{2} \end{aligned} \tag{2}$$

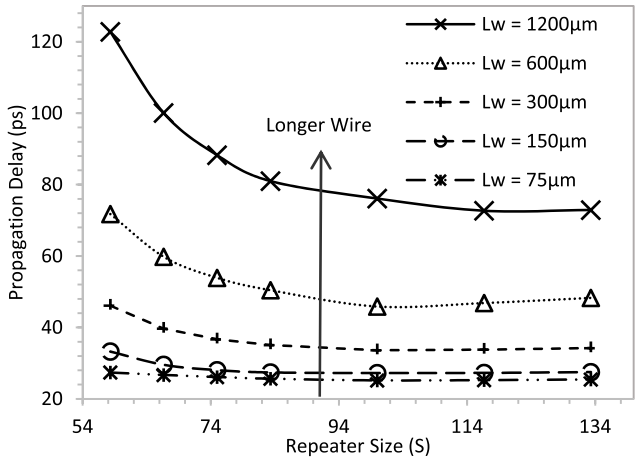

Fig. 6. Variation of propagation delay with SPLIT-IO repeater size and wire length. The propagation delay is the average of high-to-low and low-to-high propagation delays.

Assuming the wire width is minimum (400 nm in metal layer 6), the propagation delays of the SPLIT-IO repeater B3 are measured for different repeater size (S) and wire length (L_w) scenarios, as shown in Fig. 6. Data are generated by operating the circuit at $V_{\rm DD} = 1$ V and $T = 80$ °C in 45-nm CMOS technology. The shortest propagation delay is achieved for a repeater size (S) ranging from 99.91 to 116.50 regardless of the wire length (L_w). The propagation delay is increased due to smaller switching current when S is less than 99.91. Alternatively, the propagation delay is increased due to higher input and output capacitance when S is larger than 116.50. From (5), the optimum repeater size (S) that minimizes the propagation delay is 98.13. Theoretical analysis is therefore consistent with the postlayout simulation.

The optimum repeater size is increased for wider wires (larger $W_{\rm seg}$), as given in (5). For a specific wire width, the propagation speed that is achieved with the optimum repeater size (in this case, 99.91–116.50) can be further enhanced by shortening the wire segments (smaller L_w). For example, the minimum propagation delay for driving a 75-μm-long wire is 76.31% shorter as compared to a 1200-μm-long wire with the minimum width as shown in Fig. 6.

IV. Clock Distribution Network Experimental Setup

H-trees are commonly used to transmit clock signals across modern integrated circuits [9], [20]. Standard static CMOS inverters are typically used as repeaters in conventional CDNs [1], [3], [6], [9], [20]. Early stage floor planning is necessary to determine whether the proposed design fits in the chip area and to estimate the lengths of the wire segments before the layout is drawn. In this paper, H-tree CDNs are designed by applying the floor planning algorithm discussed in [23]. Three floor planning strategies that are considered for CDN design are described in Section IV-A. The criteria for determining the sizes of repeaters are presented in Section IV-B.

TABLE II
Metal Layers in 45-nm CMOS Technology

	Thickness (nm)	Minimum width (nm)	Minimum space (nm)
Metal 6 - 7	850	400	400
Metal 1 - 5	150	70	70

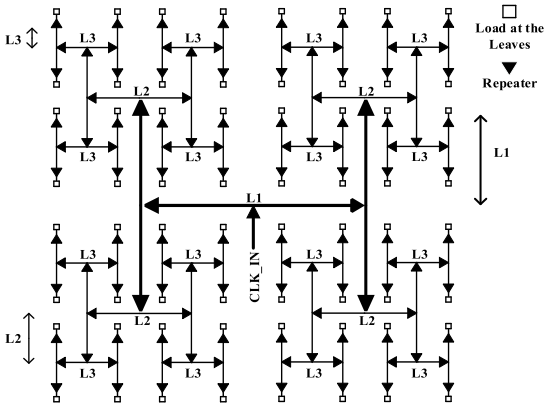

Fig. 7. Generic floor plan of a three-level H-tree CDN. The wire segments in level 1, level 2, and level 3 are L1, L2, and L3, respectively.

CDNs are designed for a chip area of 18.34 mm^2 with 2 million instances composed of various combinational logic gates, flipflops, latches, and wires in a 45-nm CMOS technology. Devices with three different threshold voltages (LVT, SVT, and HVT) and a minimum gate length of 40 nm are provided by the 45-nm CMOS technology that is used in this paper. The interconnect stack has seven copper layers as listed in Table II. Metal 1 to Metal 5 layers have a narrow pitch of 140 nm. Alternatively, Metal 6 and Metal 7 layers have a wider pitch of 800 nm. Metal layer 6 is used for the interconnects in the CDN [17].

A. Floor Planning of Symmetrical H-Tree Grid

1) Strategy-I: A symmetric H-tree driving a simple grid having uniform wire spacing is considered with strategy-I. The generic floor plan of a three-level H-tree clock network that spans an overall die area of 18.34 mm^2 is shown in Fig. 7. Wires in Level 1, Level 2, and Level 3 of the clock tree are represented by L1, L2, and L3, respectively. The lengths of L1, L2, and L3 are 1200, 600, and 300 μm, respectively. By employing relatively longer interconnects between the repeaters, the number of repeaters that is needed for clock distribution across the chip is reduced with strategy-I.

2) Strategy-II: With strategy-II, the maximum lengths of L1, L2, and L3 are exactly half of the wire segments in strategy-I. For example, a 1200-μm interconnect segment in strategy-I is replaced with two 600-μm wires separated

by a repeater in strategy-II. Similarly, the 600 and 300-μm interconnect segments in strategy-I are replaced with 300 and 150-μm wire segments, respectively, separated by repeaters in strategy-II. The wire lengths between any two consecutive repeaters in Level 1, Level 2, and Level 3 are 600, 300, and 150 μm, respectively, in this floor plan.

Sharper signal transitions at the leaves of the clock tree are achieved with floor plan strategy-II due to the increased number of buffers with shorter wire segments as compared with floor plan strategy-I. However, the active power consumption is higher due to the increased number of repeaters in strategy-II as compared to strategy-I for a given chip area.

3) Strategy-III: With strategy-III, the maximum lengths of L1, L2, and L3 are one-quarter of the wire segments in strategy-I. The wire lengths between any two consecutive repeaters in Level 1, Level 2, and Level 3 are 300, 150, and 75 μm, respectively, in strategy-III. For a given chip area, the number of repeaters is higher as compared to strategies I and II. A higher clock frequency with sharper signal transition time is thereby achieved with floor plan strategy-III as compared to the other strategies. At $V_{\rm DD} = 1$ V and $f = 2$ GHz, the output transition time at the leaves of SPLIT-IO clock tree is reduced by 35.72% and 28.58% with strategy-III when compared with strategies I and II, respectively. The active power consumption is however increased by 58.44% and 37.42% as compared to strategies I and II, respectively. The electrical characteristics of the conventional clock tree and the SPLIT-IO CDN that are implemented with these three floor plan strategies are compared for various clock frequencies and supply voltages. The tradeoff between power consumption and signal slew rate for various operating conditions is presented in Section V.

B. Transistor Sizing and Layout Area

All the CDNs are designed to maintain a clock signal transition time of less than or equal to 10% of the cycle time [1]. The transition times (slew rates) that are less than or equal to 50 ps are considered to be acceptable at the leaves of the clock trees [10]. The simplest criterion for choosing the repeater size (S) of SPLIT-IO buffer and the lengths of interconnects is to minimize the propagation delay [1]. SPLIT-IO repeaters are sized to achieve the shortest propagation delay while satisfying the target transition times requirement (less than or equal to 50 ps) at the leaves of the H-tree CDN. The optimum W_{P1}, W_{P2}, W_{N1}, and W_{N2} of SPLIT-IO repeater are 38, 22, 12, and 15 μm, respectively. The drawn gate lengths of all transistors used in the clock buffers are minimum ($L_{\rm min} = 40$ nm).

The widths of the devices P_0 and N_0 (W_{P0} and W_{N0}) of the standard static CMOS inverter-based repeaters are also optimized for achieving the minimum propagation delay while satisfying the target transition times at the leaves. W_{P0} is 55 μm and W_{N0} is 22 μm in the optimum static CMOS inverter. The transition times of clock signals tend to decrease (sharper clock signal edges) at the leaves as the numbers of buffers and wire segments are increased from floor plan strategy-I to III.

The layout area of SPLIT-IO buffer is 11.05% larger than the static CMOS inverter. Due to the SPLIT-IOs, the overall wire routing area of the proposed CDN is 66.66% larger than the conventional CDN. The overall clock routing of SPLIT-IO repeaters occupies nearly 1.22% of the total chip area with floor plan strategy-III. Alternatively, the overall clock routing of the conventional clock network occupies 0.96% of the total chip area. The overall area overhead of the SPLIT-IO clock network compared to the conventional clock network is, therefore, only 0.26% of the total chip area with floor plan strategy-III.

V. Postlayout Characterization

The novel and conventional CDNs are designed with identical criteria. Layouts of H-tree clock networks are drawn with Cadence Virtuoso using the design rule set of 45-nm CMOS technology. Metal layer 6 is used for interconnection between any two successive repeaters in a clock tree. Clock trees are compared for three different floor plan strategies with various supply voltages and clock frequencies at $T = 80$ °C.

A. Active Power Consumption

Active power consumption of the novel and conventional H-tree clock networks is listed in Table III. All the data are normalized with respect to the conventional 2-GHz CDN that operates at $V_{\rm DD} = 1$ V. The dynamic switching power consumption of SPLIT-IO clock tree is increased due to the higher parasitic capacitances of larger transistors and wires as compared to the conventional clock network. The overall active power consumption of the novel clock network is, therefore, 35.05%, 18.97%, and 17.18% higher than the conventional clock network with floor planning strategies I, II, and III, respectively, at $V_{\rm DD} = 1$ V and $f = 500$ MHz. Longer wires exhibit higher *RC* delays [2], thereby causing longer transition times at the intermediate input–output nodes of the SPLIT-IO repeaters along a buffered line. The difference of active power consumption between SPLIT-IO and conventional clock networks is higher with floor plan strategy-I due to higher short-circuit currents [24] produced by the repeaters connected with longer wires.

The active power consumption of the SPLIT-IO clock network is 83.13 mW at $V_{\rm DD} = 1$ V and $f = 2$ GHz with floor plan strategy-II. The active power consumption can be reduced by scaling the power supply voltage [6]. Both SPLIT-IO and conventional clock networks however fail to operate at 2 GHz with power supply voltages of 0.9 and 0.8 V due to lower device currents and longer wire delays with floor plan strategy-I. By scaling the power supply voltage to 0.8 V, the active power consumption of the 2-GHz SPLIT-IO clock network with floor plan strategy-III is reduced to 70.61 mW. Hence, the SPLIT-IO clock tree employing floor plan strategy-III can operate at a lower supply voltage ($V_{\rm DD} = 0.8$) while maintaining identical clock frequency (2 GHz) and consuming 15.06% lower power as compared with floor plan strategy-II at $V_{\rm DD} = 1$ V.

The signal transition times [1] at the leaves of 2-GHz SPLIT-IO clock tree are 32.08, 48.10, and 76.88 ps with power supply voltages of 1, 0.9, and 0.8 V, respectively, with floor plan strategy-II. Alternatively, with floor plan strategy-III,

TABLE III
COMPARISON OF NORMALIZED ACTIVE POWER CONSUMPTION OF CONVENTIONAL AND SPLIT-IO CLOCK TREES

Frequency		500MHz		1GHz		2GHz	
Circuit		SPLIT-IO	Conventional	SPLIT-IO	Conventional	SPLIT-IO	Conventional
V_{DD} = 0.8V	Floor plan-I	0.082#	0.062#	0.144#	0.108#	Fail*	Fail*
	Floor plan-II	0.125#	0.108#	0.222#	0.191#	0.407#	0.352#
	Floor plan-III	0.171	0.154	0.330	0.294	0.629	0.572
V_{DD} = 0.9V	Floor plan-I	0.107#	0.081#	0.198#	0.148#	Fail*	Fail*
	Floor plan-II	0.161	0.141	0.287	0.246	0.563	0.471
	Floor plan-III	0.262	0.231	0.467	0.407	0.889	0.775
V_{DD} = 1.0V	Floor plan-I	0.131	0.097	0.259	0.187	0.492	0.354
	Floor plan-II	0.207	0.174	0.386	0.324	0.741	0.611
	Floor plan-III	0.341	0.291	0.609	0.513	1.184	1

*Fail: clock network fails to function (post layout simulation at 80°C).
Clock network is functional. However, the network does not satisfy the transition time (slew rate) requirement at the leaves.

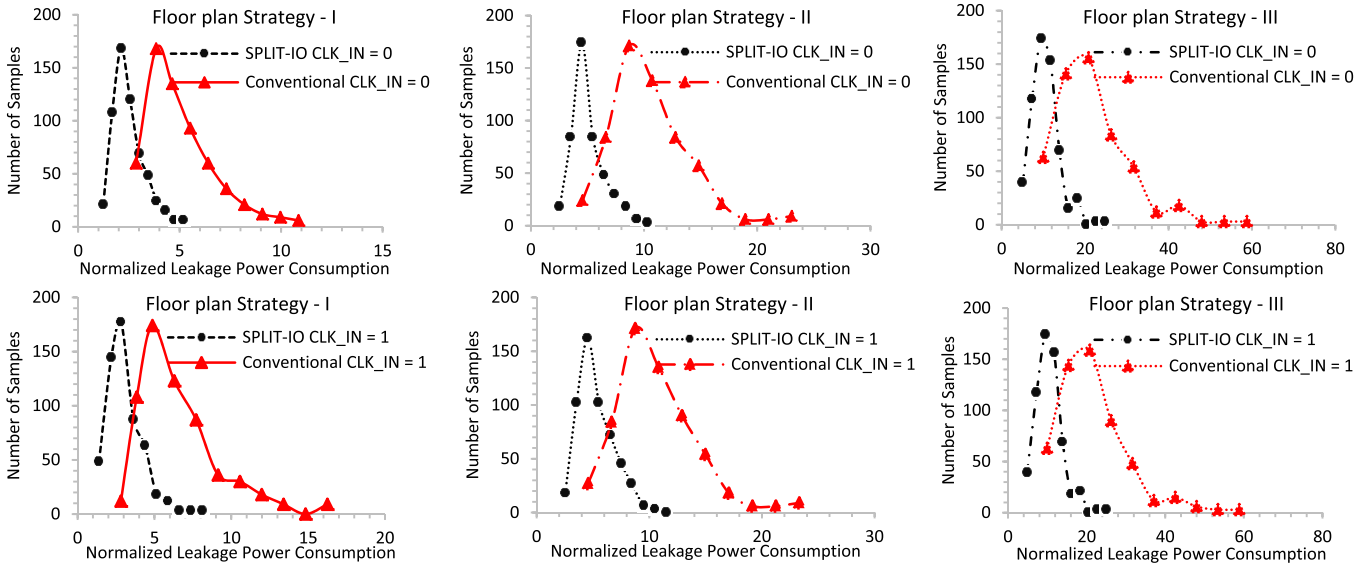

Fig. 8. Comparison of statistical leakage power consumption of conventional and SPLIT-IO clock trees for various floor plan strategies (postlayout simulation at 80 °C and $V_{DD} = 1$ V). The entire clock tree is assumed to be inactive (the whole clock tree is gated).

the signal transition times at the leaves of the 2-GHz SPLIT-IO clock tree are 22.17, 31.09, and 49.04 ps with power supply voltages of 1, 0.9, and 0.8 V, respectively. The transition time constraint (≤10% of clock duration) at the leaves of both the SPLIT-IO and conventional clock trees is not satisfied at $V_{DD} = 0.8$ V and $f = 2$ GHz with floor plan strategy-II. Alternatively, by using the floor plan strategy-III with $V_{DD} = 0.8$ V, the target transition time is satisfied at the leaves while also reducing the active power consumption overhead of the SPLIT-IO clock tree. For $V_{DD} = 0.8$ V and 2-GHz switching frequency, the difference in active power consumption between SPLIT-IO and conventional networks is 9.96% with strategy-III.

B. Subthreshold Leakage Currents

The clock signal is gated to reduce the dynamic switching power consumption when the clocked elements are idle in a synchronous integrated circuit. The power consumed by a gated CDN is primarily due to the subthreshold leakage currents as discussed in Section II.

The subthreshold leakage currents that are produced by the repeaters are determined by the total effective width and threshold voltages of the transistors that are cutoff [5]. The subthreshold leakage current that is produced by a MOSFET is exponentially reduced with a higher threshold voltage [5], [11]. The leakage power consumption is also dependent on the voltage level of the gated global clock signal.

In the repeater stages where the inputs are low, the SVT device N_1 with smaller width produces approximately 68.21% lower leakage current in a SPLIT-IO repeater as compared to the SVT device N_0 with larger width in an inverter-based repeater with $V_{DD} = 1$ V. Furthermore, the leakage current that is produced by the smaller HVT device N_2 is reduced by 84.43% in the SPLIT-IO repeater as

TABLE IV

COMPARISON OF NORMALIZED LEAKAGE POWER CONSUMPTION FOR CONVENTIONAL AND SPLIT-IO CLOCK TREES

Circuit		CLK_IN = 0		CLK_IN = 1	
		SPLIT-IO	Conventional	SPLIT-IO	Conventional
V_{DD} = 0.8V	Floor plan I	0.068	0.137	0.077	0.166
	Floor plan II	0.146	0.296	0.146	0.296
	Floor plan III	0.290	0.589	0.290	0.591
V_{DD} = 0.9V	Floor plan I	0.088	0.177	0.104	0.214
	Floor plan II	0.192	0.404	0.192	0.405
	Floor plan III	0.366	0.781	0.367	0.782
V_{DD} = 1.0V	Floor plan I	0.108	0.245	0.123	0.279
	Floor plan II	0.228	0.509	0.233	0.510
	Floor plan III	0.456	0.999	0.457	1

*Post layout simulation at T = 80°C.

compared to the larger SVT device N_0 in the inverter-based repeater. Alternatively, in the repeater stages where the inputs are high, the smaller SVT device P_2 produces approximately 68.66% lower leakage current in a SPLIT-IO repeater as compared to the larger SVT device P_0 in an inverter-based repeater. The leakage current that is produced by the smaller HVT device P_1 in the SPLIT-IO repeater is reduced by 85.14% as compared to the larger SVT device P_0 in the inverter-based repeater with $V_{DD} = 1$ V. The standby leakage power consumed by the conventional clock tree is, therefore, approximately 2.27× the SPLIT-IO clock tree with floor planning strategy-I for both clock gating scenarios (CLK_IN = "0" or "1") at $V_{DD} = 1$ V. At $V_{DD} = 0.9$ V, the leakage power consumption of conventional H-tree is 2.06×, 2.11×, and 2.13× the leakage power consumption of SPLIT-IO H-tree for floor planning strategies I, II, and III, respectively (CLK_IN = "1"), as listed in Table IV.

To observe the impact of process variations [12], [22] on leakage power consumption, statistical analysis is carried out with 500 Monte Carlo simulations. The three standard deviations (SDs) of device effective channel length (L_{eff}), physical oxide thickness (t_{ox}), threshold voltage (V_t), and wire width are 30%, 20%, 15%, and 25%, respectively, of the mean values. The variations of the supply voltage are ±5%.

The mean of the statistical leakage power consumption of conventional H-tree is 1.76× to 2.20× the SPLIT-IO clock tree depending on the clock gating scenario (high or low) at $V_{DD} = 1$ V. Furthermore, the leakage spread (SD) of the conventional clock tree is 1.58× to 3.81× the novel CDN. The upper tail end of leakage power distribution (maximum leakage power consumption) of conventional H-tree is 2.09× to 2.37× the SPLIT-IO clock tree when the clock is gated low (CLK_IN = "0") as shown in Fig. 8. Alternatively, when the CLK_IN is gated high, the upper tail end of leakage power distribution of conventional H-tree is 1.99× to 2.35×

TABLE V

MEAN AND SD OF STATISTICAL LEAKAGE POWER CONSUMPTION

Circuit	Parameter	SPLIT-IO		Conventional	
	CLK_IN	Mean (μW)	SD (μW)	Mean (μW)	SD (μW)
Floor plan I	"0"	2.56	0.76	5.56	1.73
	"1"	3.25	1.01	7.16	3.85
Floor plan II	"0"	5.82	1.74	10.25	2.75
	"1"	5.83	1.75	10.29	2.78
Floor plan III	"0"	10.95	2.88	23.91	9.61
	"1"	11.46	2.87	24.67	10.43

*Post layout simulation at V_{DD} = 1V and T = 80°C.

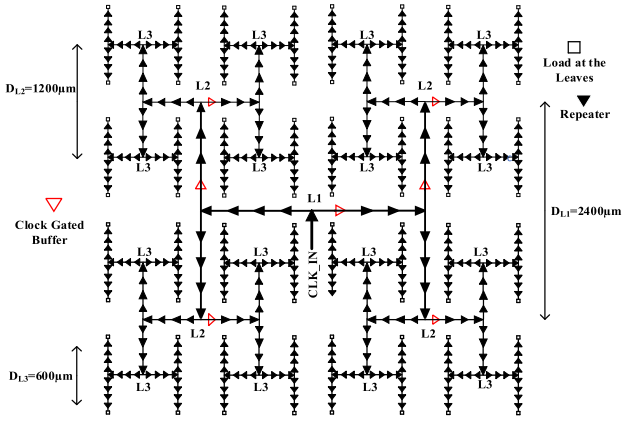

Fig. 9. Generic floor plan of a three-level H-tree CDN with clock gated control buffer circuits. The wire segments in level 1, level 2, and level 3 are L1, L2, and L3, respectively.

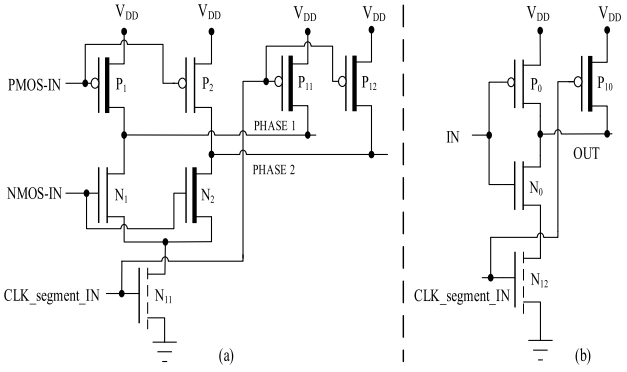

Fig. 10. Buffers with built-in clock-gating capability. (a) Proposed SPLIT-IO cell with clock gating control signal. (b) Conventional buffer with clock gating control signal. Thin dashed line in the channel area: LVT transistor.

the SPLIT-IO CDN. The clock tree with SPLIT-IO repeaters, therefore, significantly reduces the leakage power consumption while also displaying less sensitivity to process variations as compared to the conventional clock tree as listed in Table V.

C. Energy Consumption—Partially Active Networks With Local Clock Gating

The influence of leakage currents on the overall energy consumption of active clock trees is elucidated in this section.

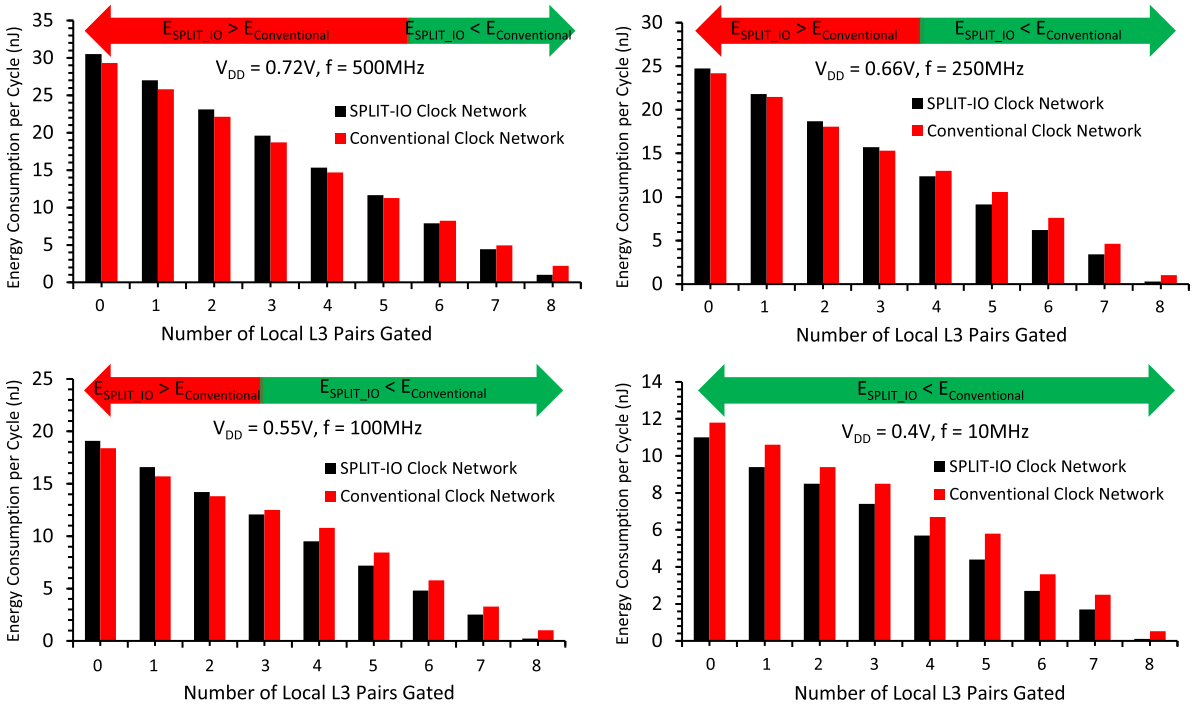

Fig. 11. Comparison of the total energy consumption of conventional and SPLIT-IO clock trees for various local clock gating scenarios at different power supply voltages and frequencies with floor plan strategy-III (postlayout simulation at 80 °C).

At high clock frequencies, the overall energy consumption per cycle is primarily due to the switching activity of buffers and wires. As the supply voltage and frequency are scaled, however, dynamic switching energy consumption is reduced. Alternatively, the leakage energy consumption per cycle is increased due to the increased clock period with supply voltage scaling [7], [26], [27]. In the low voltage and low-frequency regimes, therefore, the leakage currents may dominate the total energy consumption of an active CDN.

In processors such as the ARM cortex A-54 [25], most of the circuit blocks on the chip tend to be idle/unused during the normal operation. Local clock gating is therefore a useful strategy for lowering the energy consumption of the processor. Any segment of a clock network can be gated locally with the help of selectively placed control buffers with clock gating capability. The placement of clock gated control buffers that replace the SPLIT-IO or inverter-based buffers in a clock network is illustrated with a representative example in Fig. 9 (assuming floor plan strategy-III). The clock networks are composed of 16 L3 segments. L3 segments are assumed to be gated in pairs in this demonstration. The number of clock-gated L3 pairs considered in this example is $1, 2, 3, \ldots$, and 8: 1 indicates one L3 pair is gated locally, 2 indicates two L3 pairs are gated locally, . . ., and 8 indicates the entire clock network is gated (CLK_IN = 1).

The modified SPLIT-IO and conventional buffers with additional inputs that allow the local clock gating are shown in Fig. 10. The local segments of a clock network are gated whenever the CLK_segment_IN signal is low. The clock-gated buffer output is maintained at V_{DD}, thereby blocking the propagation of the incoming clock signal further down the clock tree. The clock is thereby gated high (i.e., CLK_segment_IN = 0) in the inactive segments of the clock tree.

To demonstrate the influence of the suppressed leakage currents in reducing the overall energy consumption with the proposed SPLIT-IO buffers under various clock gating scenarios, both conventional and SPLIT-IO clock networks with floor plan strategy-III are simulated at various operating voltages and frequencies. At $V_{DD} = 1$ V and for operating frequencies higher than 1 GHz, the total energy consumed by SPLIT-IO clock tree is higher than the conventional clock network for any number of L3 pairs locally clock gated, unless the entire clock network is inactive and gated as discussed in Section V-B.

The overall energy consumption of the SPLIT-IO clock tree is lower as compared to the conventional clock tree if less than 25% of the clock tree is active at $f = 500$ MHz and $V_{DD} = 0.72$ V (minimum supply voltage required for operation at 500 MHz) as shown in Fig. 11. At $f = 250$ MHz and $V_{DD} = 0.66$ V (minimum supply voltage required for operation at 250 MHz), the overall energy consumption of SPLIT-IO clock tree is lower than the conventional clock tree if less than 50% of the clock tree is active. Alternatively, at $f = 100$ MHz and $V_{DD} = 0.55$ V (minimum supply voltage required for operation at 100 MHz), the overall energy consumption of SPLIT-IO clock tree is lower than the conventional clock tree if less than 63% of the clock tree is active. When the operating frequency and supply voltage are further scaled down to $f = 10$ MHz and $V_{DD} = 0.4$ V, the overall energy consumption of SPLIT-IO clock tree is lower than the conventional clock network even with no local clock gating. In other words, the total energy consumption of the SPLIT-IO

clock tree is lower due to the suppressed leakage currents as compared to the conventional clock tree even if the entire clock tree is active at $V_{DD} = 0.4$ V.

The amount of local clock gating that is required for providing net energy savings with the SPLIT-IO network is reduced with power supply voltage and frequency scaling due to significant reduction of leakage currents with the SPLIT-IO repeaters as compared to the conventional repeaters. The proposed clock network is therefore attractive for achieving enhanced energy-efficiency, particularly in low-voltage and low-frequency applications [25].

VI. Conclusion

A novel H-tree CDN with dual-threshold voltage SPLIT-IO repeaters is presented in this paper for achieving lower leakage power consumption without degrading the clock frequency and signal slew rate as compared to a standard CDN. Leakage currents are suppressed by employing smaller dual-threshold-voltage transistors in the new SPLIT-IO repeaters. An analytical expression is derived to optimize the sizes of repeaters for achieving the minimum propagation delay. Three floor planning strategies are discussed for both conventional and SPLIT-IO-based CDNs.

The mean standby leakage power consumption of the conventional H-tree is 76.12%–120.31% higher than the proposed CDN with SPLIT-IO repeaters considering the process parameter variations at 1 V. The spread of standby leakage power consumption of the conventional clock tree due to process parameter variations is 58.04%–281.18% wider than the proposed SPLIT-IO network. Furthermore, the upper tail end of leakage power distribution (maximum leakage power consumption) of conventional H-tree is 99.82%–137.69% higher than the SPLIT-IO clock tree operating at 1 V. Hence, a clock tree employing SPLIT-IO repeaters produces much smaller leakage currents and displays weaker sensitivity to process fluctuations as compared to the conventional clock tree where standard inverters are used as repeaters. The total energy consumed by the SPLIT-IO clock network is 4.11%–55.12% lower as compared to the static CMOS inverter-based clock tree if less than 25% of the network is active at $f = 500$ MHz and $V_{DD} = 0.72$ V. The amount of local clock gating that is required for providing net energy savings with the proposed SPLIT-IO buffers is reduced with power supply voltage and frequency scaling in partially active CDNs. The total energy consumption of the SPLIT-IO clock tree is 6.78% lower than the conventional clock tree even if the entire network is active with a clock frequency of 10 MHz and a supply voltage of 0.4 V.

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