Design of Defect and Fault-Tolerant Nonvolatile Spintronic Flip-Flops

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***Abstract*— With technology down scaling, static power has become one of the biggest challenges in a *system on chip*. Normally off computing using nonvolatile (NV) sequential elements is a promising solution to address this challenge. Recently, many NV shadow flip-flop architectures have been introduced in which *magnetic tunnel junction* (MTJ) cells are employed as backup storing elements. Due to the emerging fabrication processes of magnetic layers, MTJs are more susceptible to manufacturing defects than their CMOS counterparts. Moreover, unlike memory arrays that can effectively be repaired with well-established memory repair and coding schemes, flip-flops scattered in the layout are more difficult to repair. Therefore, without effective defect and fault tolerance for NV flip-flops, the manufacturing yield will be affected severely. In this paper, we propose a *fault-tolerant NV latch* (FTNV-L) design, in which several MTJ cells are arranged in such a way that it is resilient to various MTJ faults. The simulation results show that our proposed FTNV-L can effectively tolerate all single MTJ faults with a considerably lower overhead than traditional approaches.**

***Index Terms*— Fault tolerant, flip-flop, magnetic tunnel junction (MTJ) open defect, MTJ short defect, nonvolatile (NV) memory faults, process variation, spin-transfer torque (STT), spintronics, stuck at AP, stuck at P, temperature, triple modular redundancy (3MR), tunnel magnetoresistance (TMR).**

I. Introduction

With the advancements in technology scaling, the excessive leakage power of CMOS devices becomes a major design issue [1], [2]. Therefore, nonvolatile (NV) magnetic memories using spintronic technologies such as *spin-transfer torque (STT)* and *spin orbit torque* are gaining popularity. This is due to their various advantageous features such as high endurance, scalability, high density, low access latency, soft error immunity and CMOS compatibility [3]–[8]. In these technologies, *magnetic tunnel junction* (MTJ) cells are used as storing devices, which store the logic value as resistance states. These storing devices can also be employed for flip-flop designs in a low-power *system on chip* (SoC). Therefore, many NV shadow flip-flop architectures have recently been introduced that exploit the normally off and instant-on attributes of MTJs [9]–[13]. However, a single MTJ failure in such designs can lead to a complete breakdown of the normally off capabilities.

The fabrication of the magnetic layers to implement MTJ cells is more complex than that of conventional CMOS, since it is a new process based on new materials. Therefore, it is expected that magnetic layers are more prone to manufacturing defects than CMOS layers [14]–[18]. For instance, there is a possibility of a *barrier short* during the ion beam etching process [19]. As a consequence, the affected MTJs have a very low resistance value [20]. On the contrary, MTJ cells exhibit an extremely high resistance for an *open defect*. In addition, the magnetic orientation of the MTJ cells can be fixed to a specific magnetization configuration, meaning that their magnetic orientation and thus their resistances cannot be changed [21]–[23]. This may happen permanently because of manufacturing defects in the magnetic layers or due to loss of margin in the CMOS support circuitry, such as reduced switching current or duration [21]. All these defects can severely hurt the manufacturing yield of these emerging technologies and prevent their widespread adoption.

In order to render manufacturing defects, memories are usually equipped with redundancies and error detection/correction mechanisms [22]. However, these techniques are inapplicable to flip-flop designs, because flip-flops are scattered widely in the SoC layout as individual cells. Nevertheless, in flip-flop designs, these faults can be addressed using traditional *triple modular redundancy* (3MR),[1] in which the shadow latch component is triplicated, and the final output is generated based on a voting mechanism. In fact, it incurs huge area, energy, and latency costs. Therefore, it is a decisive need to have a cost-effective solution to deal with MTJ faults for overall yield and energy efficiency.

In this paper, we propose a novel shadow flip-flop architecture, in which we design a generic *fault-tolerant NV latch* (FTNV-L) to address the aforementioned faults in MTJ cells. In our proposed FTNV-L design, several MTJ cells are structured in such a way that it can easily tolerate all single MTJ faults within a flip-flop.

A preliminary version of this work was published in [24], in which the basic implementation of FTNV-L was discussed. In this paper, we extend our work with a detailed process variation analysis for our proposed FTNV-L design. Moreover, we demonstrate implications on MTJ resistance differences

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[1] To distinguish between tunnel magnetoresistance (TMR), we refer to triple modular redundancy as 3MR.

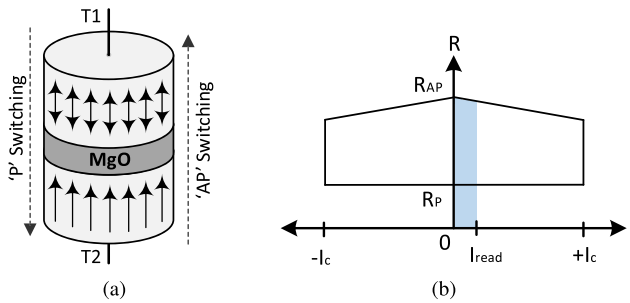


Fig. 1. MTJ device and its R–I characteristics. (a) MTJ device. (b) R–I characteristics.

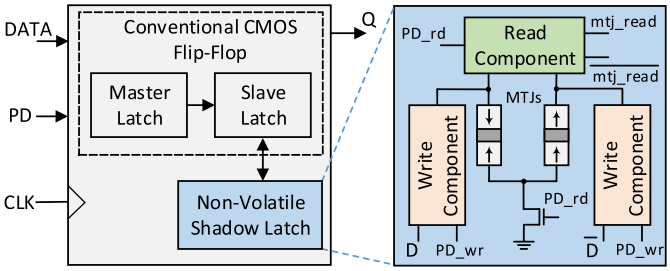


Fig. 2. Overview of shadow NV flip-flop architecture.

(also known as TMR) and read latency for our proposed design for various operating temperatures. In addition, we also present an algorithm to determine the minimum required TMR and resistance values for the MTJ cells to guarantee a fault-free functionality in the presence of various MTJ defects.

Our overall contributions for this paper are as follows.

1) We design an FTNV-L for the shadow architecture and analyze its functionality in the presence of various MTJ defects.
2) We develop an algorithm to determine the TMR and resistance values for MTJs to achieve the minimum required effective resistance difference to generate a correct output in the presence of any single fault.
3) We perform a process variation analysis for our proposed design for each MTJ fault case.
4) We demonstrate the variation of TMR and read latency with respect to different operating temperatures.
5) We present a comprehensive comparison of our proposed design with the 3MR approach.

The simulation results demonstrate that our proposed FTNV-L design delivers the required resistance differences in the presence of any single fault to guarantee a fault-free functionality. Moreover, it has almost the same performance and energy for both backup and restore processes as a standard NV flip-flop. In addition, adding MTJ cells has a minimal impact on the overall flip-flop area, as they are fabricated in different layers.

The remainder of this paper is organized as follows. In Section II, the basics of the STT technology are discussed. Section III explains our proposed FTNV-L design, followed by the experimental results in Section IV. Finally, Section V concludes this paper.

II. Background

A. Spin-Transfer Torque

The MTJ cell, which is a storing device, consists of two ferromagnetic layers separated by a thin barrier oxide. One of the ferromagnetic layers, whose magnetic orientation is always fixed, is known as the *referenced layer* (RL), whereas the magnetic orientation of the other layer can be freely rotated, which is termed as the *free layer* (FL). An MTJ cell stores data as a resistance state. When the magnetic orientation of the two ferromagnetic layers is parallel to each other ("P" configuration), it exhibits a low resistance value. Otherwise, it has a high resistance value, when the magnetic orientation of those two layers are antiparallel to each other ("AP" configuration).

The MTJ cell works on two principles: 1) STT effect to store a value in the MTJ cell and 2) TMR effect to read out a value from the MTJ cell. The STT effect, which is responsible for the magnetic switching in FL, is accomplished by passing a current through the MTJ cell. Here, the magnetic switching happens when the applied current value is more than the critical current (I_c), as described in Fig. 1(b). For instance, if the current flows from the FL to RL for a sufficient duration, the magnetization of the MTJ cell switches to the "P" state. On the other hand, the magnetization of the MTJ cell switches to the "AP" state, if the current flows from the RL to FL for a sufficient duration. The TMR effect will be explained later in detail.

B. Overview of Nonvolatile Flip-Flops

A shadow flip-flop architecture using MTJ-based NV storing devices is very effective for leakage power reduction. This is due to the fact that by adopting these designs, the entire logic core can be power gated, unlike for conventional CMOS-based flip-flops. The block diagram of a typical shadow flip-flop architecture is shown in Fig. 2. It consists of three components, namely, *master latch, slave latch,* and *NV shadow latch*. Here, the master and slave latches are the same as in conventional CMOS flip-flop design, and the NV shadow latch consists of two MTJs as well as read and write components [9]–[13]. During power down, the data are stored in the shadow latch before going into the sleep mode, and they are read and restored into the slave latch during wakeup. This operation is stimulated when the "PD" pin is activated and once when the data are stored in the NV latch, the power supply is disconnected. On the other hand, during wakeup, the NV shadow latch content is read and restored into the slave latch, so that the normal operation can be resumed. The "*PD_rd*" and "*PD_wr*" signals, which are generated using the "PD" pin, are employed to activate the read and store operations, respectively. The two MTJs should always store the opposite magnetization, which assists the read process by sensing the resistance differences. If any one of the MTJs is faulty, the entire shadow latch component cannot be used in the given architecture. Hence, our proposed shadow latch component is designed in such a way that it is capable of delivering the correct output in the presence of a single faulty MTJ within each flip-flop.

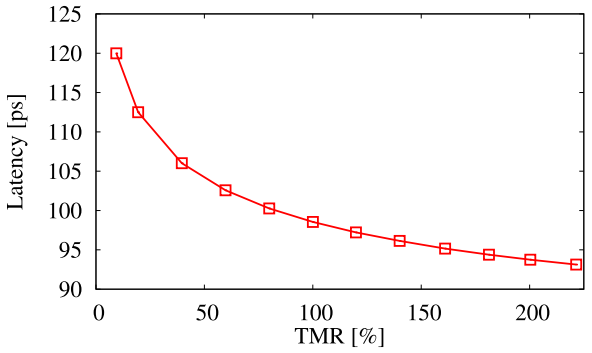


Fig. 3. Read latency for various TMR values (for typical process corner and temperature of 27 °C; see Table I for more setup information).

C. MTJ Read and Tunnel Magnetoresistance

The MTJ read is performed by passing a small amount of current through the MTJ layer stacks. It is carried out using a differential amplifier, in which the resistance of the MTJ is sensed and compared with a reference value to generate an output. The relative difference between the two resistance states of the MTJ cell plays a vital role for the output generation, which relies on the TMR value. The TMR of an MTJ cell is defined as [25]

$$\text{TMR}(\%) = \frac{R_{AP} - R_P}{R_P} \times 100 \tag{1}$$

where R_{AP} and R_P are the resistances in the "AP" and "P" magnetization states, respectively. The TMR value is highly dependent on the property of the barrier oxide layer of the MTJ cell [26]. High TMR values are always desirable for fast and reliable read. Furthermore, the read latency exponentially decreases with an increase in TMR, as shown in Fig. 3. Please note that a high TMR value for an MTJ cell also requires a high energy to switch its magnetization.

In general, flip-flop designs can achieve the same performance as memories with less than half of its TMR value. This is because in memories, the reference values are always considered to be the middle value of the two resistances [27]–[29] and its bitline is also associated with huge parasitics. However, in a shadow flip-flop architecture, as described earlier, there are two MTJs that always store opposite values. Hence, in a self-referencing scheme can be used for read operation. This means that flip-flops can attain double the sensing margin compared with those in memories. Furthermore, negligible parasitics are typically associated with these flip-flop designs compared with the bitlines in memories. Hence, in flip-flops, a low TMR value (even less than 10%) can easily deliver correct output values; nevertheless, the read latency is increased.

D. Defects in MTJs and Fault Modeling

The MTJ device uses different materials and processes for manufacturing compared with CMOS. Due to the complexity of these fabrication processes and the interdependency of magnetic materials, MTJ cells are subject to various and new failure mechanisms [14], [19]–[22]. For instance, during the ion beam etching process, due to sputtering effects, the sputtered atoms redeposit at the MTJ sidewall leading to a barrier short [19]. As a consequence, the isolation of the ferromagnetic layers is damaged, resulting in a very low resistance value [20]. In this case, although current can flow through the device, the cell no longer behaves as an MTJ cell. On the other hand, an MTJ cell can also have an open connection due to internal damage, which delivers a very high resistance value. As a result, current cannot flow through the device because of a discontinuity in the design.

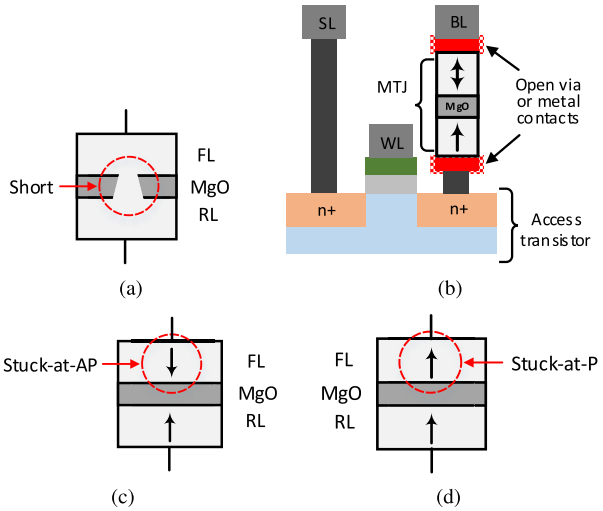


Fig. 4. Classification of MTJ fault models. (a) Short. (b) Open. (c) Stuck-at-AP. (d) Stuck-at-P.

There are some cases where the MTJ cell resistance values are not so severely affected as in open and short faults; however, their values can easily influence the sense amplifier so that an incorrect output can be generated. For instance, during fabrication, the magnetization of the FL can be permanently fixed to either "P" or "AP" configuration [23]. Another possibility is that the switching margin and the current value are not sufficient enough to flip the magnetization of an MTJ cell [21]. This is due to defects or the impact of process variation in the CMOS devices for the read/write circuitries.

In addition to manufacturing defects, MTJs are also vulnerable to runtime failures. For instance, the magnetization of an MTJ cell that can accidentally switch during a read operation is termed as *read disturb* [22], [30]. Moreover, *retention failures* also occur randomly that can alter an MTJ cell magnetization after a certain duration of time [22]. Another random fault is back hopping or reversion, in which the state of the magnetization reverses, if it overwrites the already stored value in the MTJ [31], [32].

We can broadly classify all these MTJ defects into the following four fault models (as illustrated in Fig. 4).

1) *Short Fault:* The two ferromagnetic layers, FL and RL, are connected.
2) *Open Fault:* Discontinuity in the device.
3) *Stuck-at-P Fault:* MTJ magnetization is permanently or temporally locked to the "P" state.
4) *Stuck-at-AP Fault:* MTJ magnetization is permanently or temporally locked to the "AP" state.

E. Motivation

Nowadays, the static power dominates the total power consumption in an SoC design. Moreover, it is further exacerbated with the technology downscaling and due to high performance requirements. *Power gating* is the most effective methodology for the reduction of static power consumption, in which the power supply for the idle design blocks is disconnected. In this method, the conventional CMOS-based flip-flop designs, however, are not adequate as they always require a retention supply. In addition, the conventional CMOS *save and restore* scheme [33], where the content of the flip-flop is stored in memories during power down and is restored during wakeup, contributes to severe delay and routing overheads. Hence, MTJ-based NV flip-flop designs are becoming popular as the entire logic core can be power gated, and the data backup storage can be done locally for each flip-flop [9], [13], [34]. This way, the state restoration after power-OFF cycles becomes very fast and low cost. As explained in Section II-B, these flip-flops are very efficient for static power reduction, while maintaining the same performance for normal operation as conventional CMOS flip-flops. Nevertheless, due to several MTJ defects, as mentioned previously, the shadow latch component either can fail completely (loss of nonvolatility feature) or may deliver incorrect values (loss of data integrity).

There are very effective solutions for defect and fault tolerance in array-based memories, such as main or cache memories based on error correction mechanisms [22], like row/column redundancy and error detection/correction codes, and built-in repair [35]. However, these approaches are not applicable to flip-flop designs because flip-flops are placed as individual standard cells in the SoC layout. This means, either failures in the MTJ cells of flip-flops lead to a very low manufacturing yield of the SoC or benefits of the leakage reduction cannot be utilized. Some techniques have arranged several NV components to improve the read signal margin [36]–[38]; nevertheless, the defects are ignored. For instance, these techniques cannot work if any one of the storing devices has an open defect. In [39], a robust flip-flop design is proposed to target soft error due to radiations, which targets only CMOS transistors and not MTJs. Moreover, it cannot address manufacturing defects. A traditional solution to resolve this issue is 3MR for the shadow latch. In this design, in total three shadow latch components are employed and the output is generated based on a voting system. With this approach, although one fault per flip-flop can be tolerated, it incurs overall huge area, energy, and performance costs.

In contrast, we provide a cost-effective solution, in which we arrange several MTJ cells in such a way that it can easily tolerate any single fault in a flip-flop.

III. Proposed Fault Tolerant Nonvolatile Latch

This section presents our proposed fault tolerant shadow latch design using redundant MTJ cells. In Section III-A, we explain the implementation of our proposed FTNV-L design. Later, Section III-B describes an algorithm to determine the required TMR and resistance values for our design.

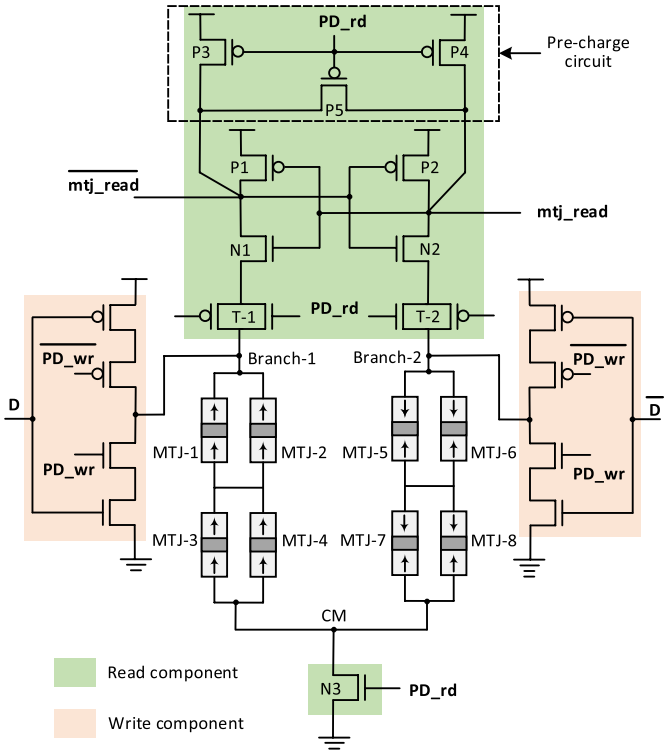


Fig. 5. Schematic of proposed FTNV-L design.

A. Proposed FTNV-L Architecture

As mentioned before, the manufacturing defects in MTJ cells are so severe that they can easily ruin the leakage benefits of the NV latch, and the existing solution is not effective. Therefore, we propose a low-cost solution using a novel fault tolerant MTJ-based latch design that can withstand various defects and deliver a correct output. The implementation details of our proposed latch design, along with its functionality in the presence of all possible faults, are discussed next.

The circuit diagram for our proposed FTNV-L design is shown in Fig. 5. It primarily consists of three components, namely, *write*, *read*, and *MTJ cell arrangements*. The purpose of the write component is to store the content of the conventional CMOS flip-flop in the MTJ cells during power down. This can be achieved by establishing a bidirectional current path such that the switching current flows through each MTJ cell. To assure the magnetic switching, the write component has to be designed in such a way that a sufficient amount of switching current for a required duration can flow through each MTJ. This current value is adjusted with the transistor widths in the write components, whereas its duration is synchronized with the "PD_wr" period. Note that the main requirement of this write process is that the two branches (i.e., *Branch-1 and Branch-2*) should always have a set of MTJs with opposite magnetizations. This design creates a self-referenced structure, which is necessary for a proper read operation.

The read component of the design is composed of a precharge circuit, a pair of back-to-back connected inverters, and a tail transistor. The purpose of the precharge circuit is to provide an equipotential at the output nodes (read_mtj and $\overline{\text{read\_mtj}}$) before the actual read is started. In our

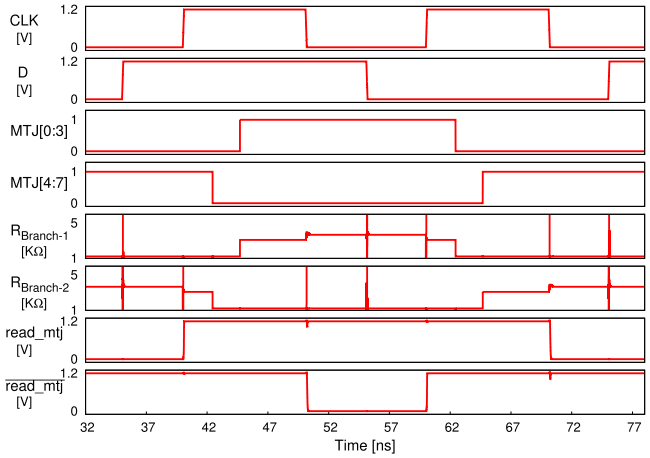


Fig. 6. Waveform to demonstrate the fault-free functionility of the proposed FTNV-L design (for typical process corner and room temperature; see Table I for more setup information).

implementation, read is performed with the activation of the "PD_rd." During the read process, the precharge circuit is deactivated and the two back-to-back connected inverters are coupled with the two branches of the MTJ sets, since the transmission gates T1 and T2 are ON. Additionally, the tail transistor "N3" is also ON at the same time. Therefore, a current path is established and the sensing process begins. During this sensing process, one of the output nodes goes to a low steady state, while the other remains at a high state. The two back-to-back connected inverters develop a positive feedback loop that accelerates the process of stabilizing the two output nodes.

The waveform illustration of the FTNV-L design is shown in Fig. 6. Here, the read output and the switching behavior of each MTJ along with its corresponding effective resistance value for each branch are shown. Read is performed at the negative level of "CLK," where the resistance difference between two branches is important to deliver the correct output. We have obtained this waveform from real simulations; hence, sometimes effective resistances have glitches when current/voltage around MTJs are changing.

The arrangement of the MTJ cells is one of the key components in our design implementation. All MTJs in each branch have the same magnetization, and as mentioned previously, the MTJs in those two branches always have the opposite magnetization. The branch in which all MTJs are in "P" and "AP" states are referred as *branch-P* and *branch-AP*, respectively. Each branch has a serial connection of the two parallel connected MTJs. This type of arrangement serves two purposes in FTNV-L design: 1) the parallel connection addresses short and open faults and 2) the serial connections are to increase the *ratio of the effective resistance difference* between the two branches, which we named *equivalent TMR* (TMR_{eq}). In other words, the flip-flop design has to meet the minimum TMR_{eq} requirement during the read operation to generate the correct output. Thus, the equivalent resistance for branch-P is given by the following equation:

$$R_{eq-P} = \frac{R_{P1} \times R_{P2}}{R_{P1} + R_{P2}} + \frac{R_{P3} \times R_{P4}}{R_{P3} + R_{P4}} \tag{2}$$

where R_P is the resistance value of the corresponding MTJ that has "P" magnetization. Similarly, the equivalent resistance for AP is

$$R_{eq-AP} = \frac{R_{AP1} \times R_{AP2}}{R_{AP1} + R_{AP2}} + \frac{R_{AP3} \times R_{AP4}}{R_{AP3} + R_{AP4}} \tag{3}$$

where R_{AP} is the resistance of the corresponding MTJ that has "AP" magnetization. Using the above two equations, TMR_{eq} is defined as

$$TMR_{eq}(\%) = \frac{R_{eq-AP} - R_{eq-P}}{R_{eq-P}} \times 100. \tag{4}$$

If one MTJ cell has a permanent or temporal defect, the equivalent resistance changes based on the fault type, as discussed next.

1) Short Fault: When one of the MTJs has a short fault, a relatively high current flows though that defective MTJ. Consequently, the MTJ that is in parallel to the shorted one is bypassed for both read and write operations. Hence, the equivalent resistance for both "P" and "AP" is

$$R_{eq-short\{P,AP\}} = \frac{R_{eq\{P,AP\}}}{2} \tag{5}$$

where $R_{eq\{P,AP\}}$ is the equivalent resistance of either branch-P or branch-AP.

2) Open Fault: When one of the MTJs is open, no current flows through that MTJ. Unlike for shorts, the MTJ that is in parallel to the defective MTJ is usable and it becomes in series with the other two parallel connected MTJs. In this case, the equivalent resistance for both "P" and "AP" configurations is

$$R_{eq-open\{P,AP\}} = \frac{R_{eq\{P,AP\}}}{2} + R_{\{P,AP\}} \tag{6}$$

where $R_{P,AP}$ is the resistance of a single MTJ in either "P" or "AP."

3) Stuck-at-P: When one of the MTJ cells is stuck at the "P" configuration, then only the "AP" branch is affected. Therefore, the equivalent resistance in branch-P is as follows:

$$R_{eq-stuck-at-P} = \frac{R_{AP}}{2} + \frac{R_P \times R_{AP}}{R_P + R_{AP}} \tag{7}$$

where R_P and R_{AP} are the resistances of the MTJs when they are in "P" and "AP" configurations, respectively.

4) Stuck-at-AP Fault: When one of the MTJ cells is stuck at the "AP" configuration, then only the branch-P is affected. Therefore, the equivalent resistance in branch-AP is as follows:

$$R_{eq-stuck-at-AP} = \frac{R_P}{2} + \frac{R_{AP} \times R_P}{R_{AP} + R_P}. \tag{8}$$

All aforementioned faults with their effective resistances are demonstrated in Fig. 7. When the faulty MTJ is in branch-AP, the short fault has the worst effective resistance, which in turn results in the worst TMR_{eq} for that fault. On the other hand, when the faulty MTJ is in branch-P, the open fault becomes critical from TMR_{eq} point of view, compared with all other faults. For more details, the reader is referred to Section IV-B.

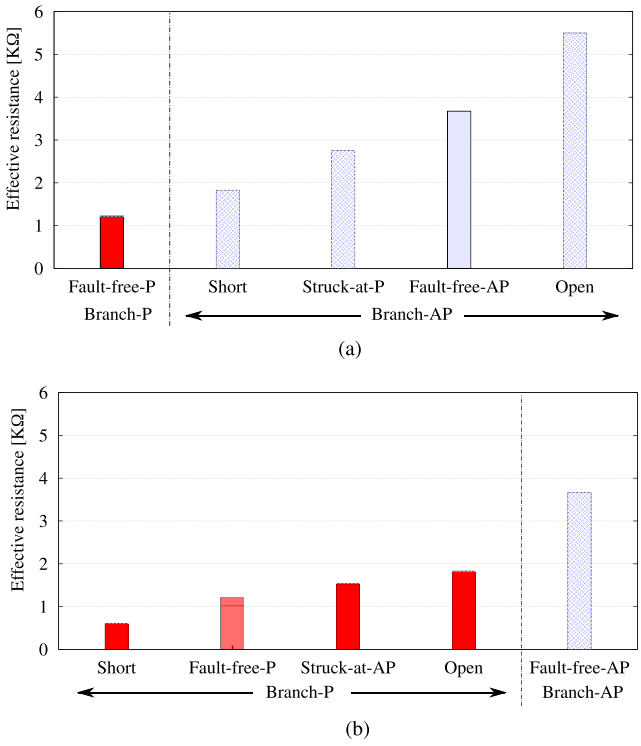


Fig. 7. Branchwise demonstration of effective resistances for MTJ faults. (a) Faulty MTJ of branch-AP. (b) Faulty MTJ of branch-P.

Algorithm 1 Algorithm to Determine TMR and Resistance Values for the MTJ Device

Input R_{min}, R_{max}, TMR_{min}, TMR_{max}, R_{array}, $TMR_{eq\_acceptable}$, R_{step}, TMR_{step}
Result TMR_{MTJ}, R_{MTJ};
For TMR_{MTJ} **from** TMR_{min} **to** TMR_{max} **in** TMR_{step} **do**
  For R_{MTJ} **from** R_{min} **to** R_{max} **in** R_{step} **do**
    R_P = R_{MTJ};
    R_{AP} = R_{MTJ} * (1 + TMR_{MTJ});
    Obtain the equivalent resistances for all four fault cases using Eq (5), (6), (7), and (8);
    Obtain the TMR_{eq} in each cases;
    if (TMR_{eq} of {Open && Short && Stuck-at-AP && Stuck-at-P} $\geq TMR_{eq\_acceptable}$) **do**
      return TMR_{MTJ};
      R_{array} collects corresponding resistance values ;
    done
  done
done
return R_{MTJ} from R_{array} that supports MTJ design parameters;

B. Algorithm to Obtain TMR and Resistance Values

The TMR and resistance values for any MTJ device have to be fixed beforehand at device level prior to the circuit design implementations. In general, high TMR is always preferable for the read; however, it has some limitations due to materials and tradeoff with device parameters such as switching energy and thermal stability. Therefore, a methodology is needed to obtain a minimum TMR of a single MTJ with a design-suited resistance value, which can tolerate all aforementioned MTJ faults in the design.

To obtain the TMR and resistance values for each MTJ, a generic algorithm is developed, as shown in Algorithm 1. As inputs, we consider the range of TMR and resistance values

TABLE I
CIRCUIT-LEVEL SETUP

Parameters	Value
VDD and Temperature	1.2 V and 27 °C
CMOS Technology	TSMC 65 nm GP
Thermal stability factor	60
Free/Oxide layer thickness	1.84/1.48 nm
RA	6.145 $\Omega\mu m^2$
TMR @ 0 V	200 %
'AP'/'P' resistance	3.6 KΩ/1.2 KΩ

that can be supported at technology level. In general, the TMR value can easily reach more than 600% depending on the oxide layer thickness and area of the device [40]. In addition, the minimal acceptable TMR_{eq}, which can generate the correct output during read, is also part of the input parameters. Here, TMR and resistance values are varied by a specific step size. For each TMR and resistance values, the effective resistance and TMR_{eq} are obtained for every fault type using (5)–(8). If the obtained TMR_{eq} is equal to or more than the acceptable TMR_{eq} value, we store the corresponding resistance values in an array, so that an optimum value, based on the device tradeoffs, can be picked. Note that the range of the input TMR values can be further increased by adding another set of parallel MTJs for both branches in the design. In that case, the read and write components have to be designed accordingly. Moreover, if the write drivers are not able to provide sufficient current in such cases, it is also possible to add multiple drivers at an intermediate stage of the design. Another possibility is to use a high supply voltage to pass a high switching current.

IV. EXPERIMENTAL SETUP AND RESULTS

We performed a circuit-level analysis in order to evaluate the efficiency of our proposed FTNV-L design. The simulation setup is discussed first, followed by the circuit-level results. In the end, a comparison of our proposed technique with 3MR is performed.

A. Simulation Setup

For the circuit design implementation, we employed the MTJ model presented in [41], and the other design parameters for the simulations are depicted in Table I. Here, our MTJ model is tuned for the TMR and resistance values specified in Table I, which are determined using (5)–(8), with the assumption of an acceptable TMR_{eq} of 50%. We have used the Cadence Spectre tool for circuit simulations.

The resistance value associated with each MTJ is obtained by measuring the current value and voltage across its terminals. Furthermore, to obtain a setup for the defective MTJ cell, we employed a resistance device to replace the MTJ in the design. For instance, a low (around 5 Ω) and a high (around 5 MΩ) resistances are connected to demonstrate the short and open faults, receptively. Similarly, to show the stuck-at-P and stuck-at-AP behaviors in the design, a resistance value equivalent of R_P and R_{AP} is connected, respectively. Please note that only one resistance at a time is connected, as our design targets a single fault per latch.

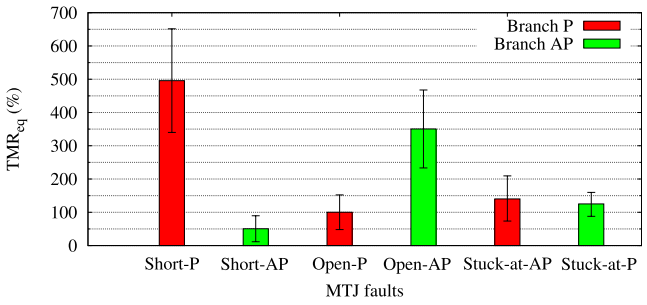


Fig. 8. TMR values in the presence of various faults.

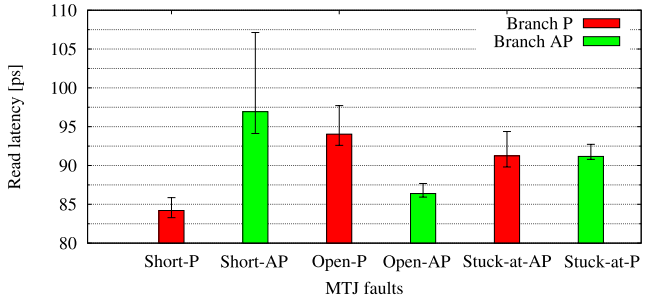


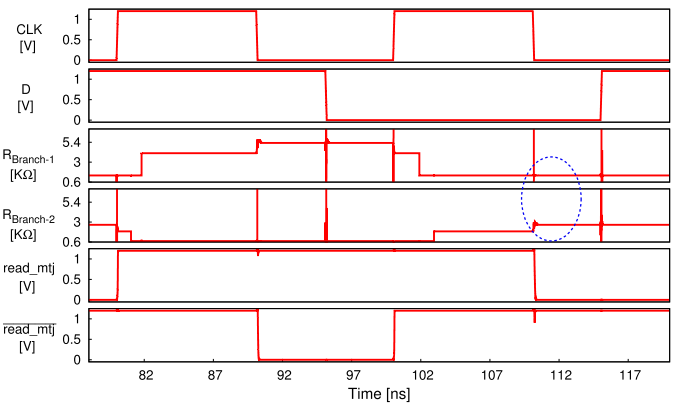
Fig. 9. Read latency values in the presence of various faults.

For process variation, we have considered MTJ and CMOS components separately as these two are different fabrication technologies. For MTJ components, we used the statistical Monte Carlo model that includes variation in terms of TMR and the product of *resistance and area*. On the other hand, for CMOS components, we used the statistical model provided by TSMC.

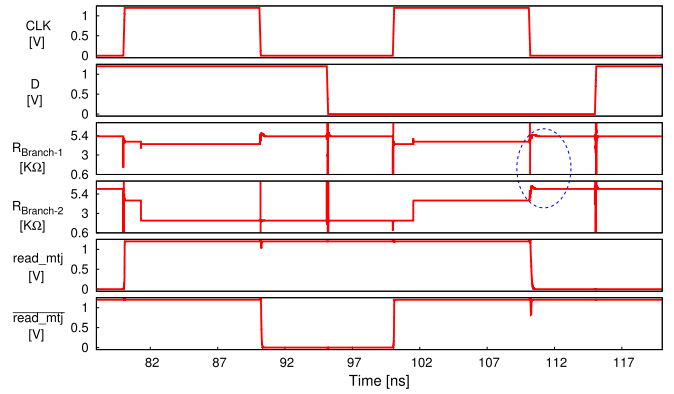
B. Circuit Functionality Analysis

The TMR value is very sensitive to MTJ defects, which in turn influences the functionality of the design. In our proposed design, we have performed a detailed TMR_{eq} analysis and the results for both branch-P and branch-AP are demonstrated in Fig. 8. These TMR_{eq} values influence the delay of the restore (read latency) operation of the FTNV-L, as demonstrated in Fig. 9. As shown in Fig. 9, the worst TMR_{eq} value is obtained for open and short faults in branch-P and branch-AP, respectively. The range of process corner variations in our TMR_{eq} and read latency results are shown with error bars. The functionality of the FTNV-L design in the presence of the short-AP and open-P faults is demonstrated in Fig. 10. In Fig. 10(a) and (b), the read outputs and effective resistances for both branches are shown. Here, Fig. 10(a) and (b) shows the low TMR values (marked by the blue circles) during the read operation. The low TMR value is for the low resistance and high resistance value range for the short-AP and open-P faults, as described in Fig. 10(a) and (b), respectively. The reason for low TMR_{eq} for short-AP fault is that the effective resistance of branch-AP becomes low, close to that of the branch-P, due to an MTJ short. Similarly, in the case of an open-P fault, the effective resistance of branch-P becomes high, close to that of the branch-AP, due to an MTJ open. However, these low TMR values are still good enough to read the output correctly.

On the other hand, in the presence of short-P and open-AP faults, the TMR_{eq} value is high, even more than that of a



(a)



(b)

Fig. 10. Functionality of FTNV-L in the presence of (a) short-AP and (b) open-AP faults (for typical process corner and temperature of 27 °C; see Table I for the setup information). The blue dotted circle indicates the worst resistance differences during read for corresponding fault cases.

fault-free MTJ cell. This is because the faulty MTJs in these two cases are additive to the resistance differences, which further increases the overall effective resistance. Moreover, the TMR_{eq} value for both stuck-at faults is slightly less than that of the TMR value of an MTJ. Since the read latency is inversely proportional to the TMR_{eq} value, short-P has the lowest and short-AP has the highest delay.

For write operation, the voltage drop due to the series–parallel connections of MTJs for our proposed design is similar to the standard latch design. This is because the overall effective resistances between the two write drivers are the same [see (2) and (3)]. However, in our proposed design, the write current is divided into two branches because of the parallel connections of the MTJs. To compensate for this, the write drivers of our proposed design are strengthened (3.4×) to deliver more switching current (around 2×) compared with the standard design. In our proposed design, the write drivers are delivering high enough current in the presence of any faults to ensure the necessary switching.

C. Process Variation Analysis

Similar to CMOS fabrication, the MTJ cell manufacturing and measurement processes also exhibit variations. In other words, due to manufacturing process, the MTJ critical dimensions such as surface area, oxide thickness, and size of the

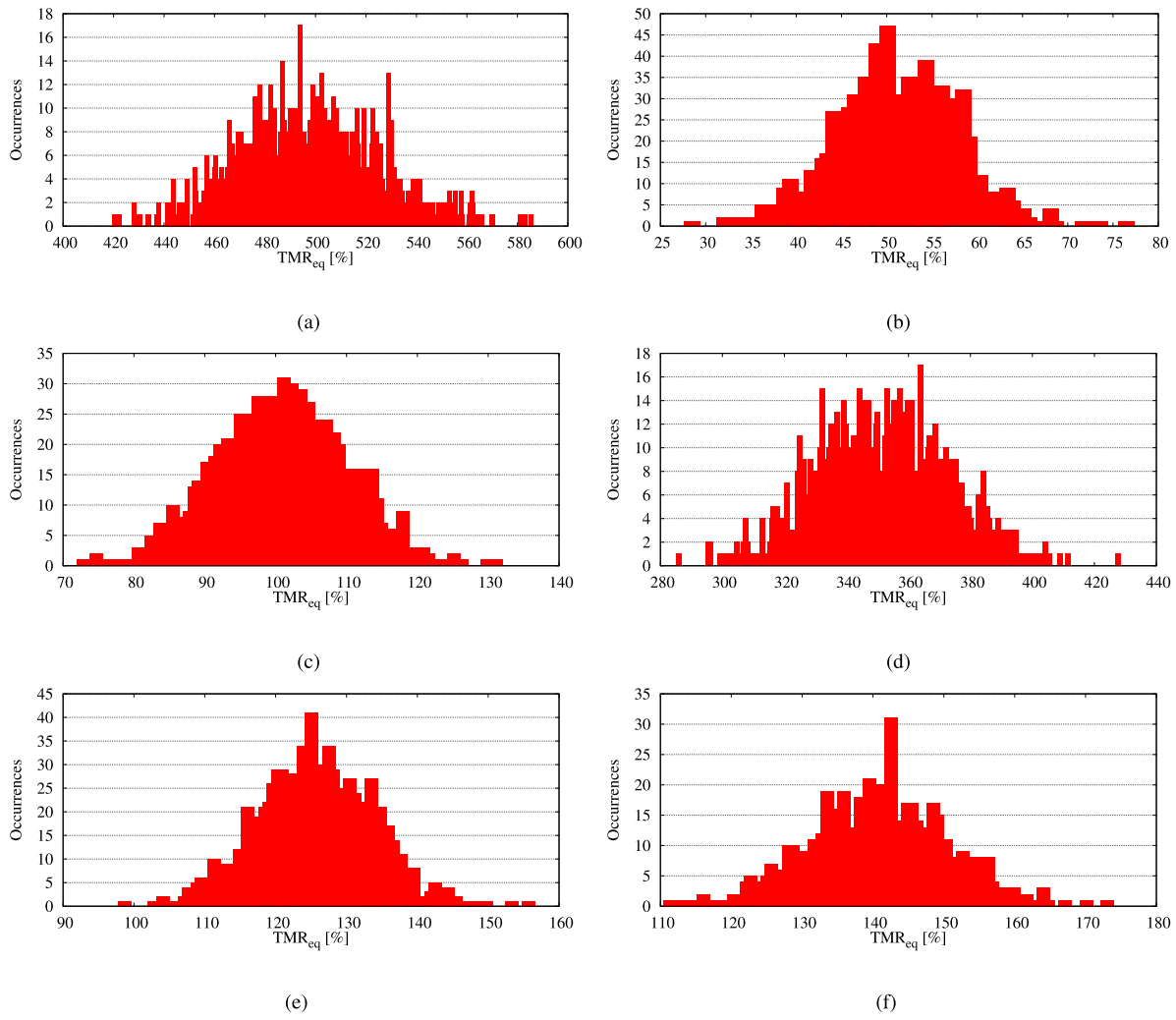


Fig. 11. Impact of process variation (1000 Monte Carlo simulations) on the effective TMR values for each fault. (a) Short-P. (b) Short-AP. (c) Open-P. (d) Open-AP. (e) Stuck-at-P. (f) Stuck-at-AP.

FL are not the same. In general, the read latency of an NV latch is influenced by process variation in two ways.

1) The resistance of the MTJ cell varies with process variation, affecting the read current and in turn the read latency.
2) Process variation affects the resistance difference (TMR), resulting in variation in the read latency, i.e., higher the TMR, lower the read latency and vice-versa (see Fig. 3).

Moreover, also CMOS variation affects the read by changing the read current mostly due to the transistor threshold variations. In order to perform a process variation analysis for our proposed FTNV-L architecture, we have run Monte Carlo simulations for the effective TMR value (TMR_{eq}). The histogram results for all faults for 1000 samples are depicted in Fig. 11. As illustrated in Fig. 11, TMR_{eq} variations for all fault cases show normal distribution. The short-P and open-AP faults can have a very high overall TMR_{eq} value as described earlier. For instance, the TMR_{eq} value for short-P fault can reach upto 586%. However, these two fault cases have much wider distributions as shown in Fig. 11(a) and (d). Here, the σ value for the TMR_{eq} value for these two faults is more than 20. On the contrary, all other fault cases have relatively narrow distribution with σ value less than 10. The short-AP fault, which has the lowest TMR value among all faults, has the lowest σ value (less than 7). The reason for this behavior is that the effective resistances in both branches in short-AP are varying mostly in the same direction. In other words, the difference in the variation of the two set of resistances of the two branches is less (around 2×), resulting in low TMR variations. Nevertheless, this difference is significant for short-P where the effective high resistance value can vary more than 5× compared with the low resistance branch value. Despite the low TMR variations for short-AP fault, the TMR_{eq} value can go as low as 29%. With this TMR value, as explained earlier, the data integrity can be maintained, but the read latency is increased significantly (can reach up to 105 ps).

D. Variations Due to Different Operating Temperature

The TMR value of an MTJ device varies with the operating temperature, as the MTJ resistances are sensitive to temperature. Therefore, in order to evaluate the efficiency of our

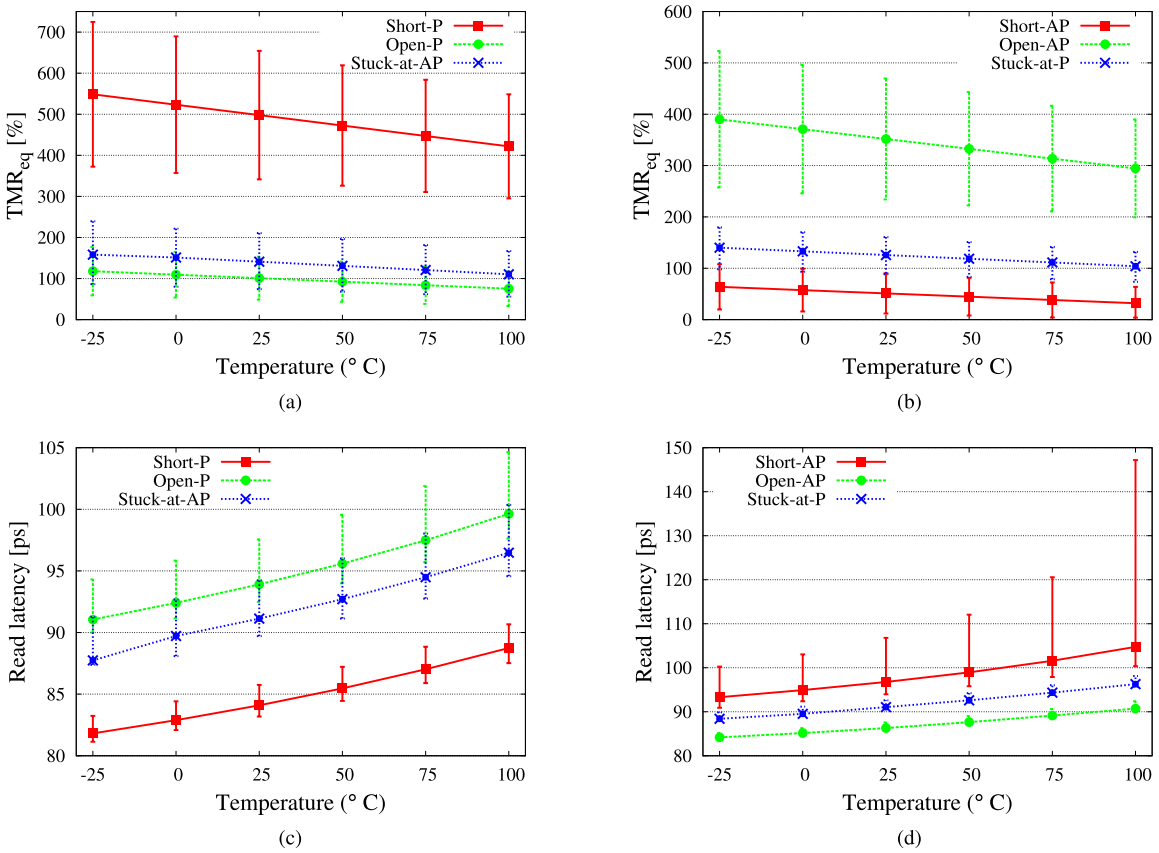


Fig. 12. TMR and read latency variations for various MTJ faults with respect to operating temperature. (a) Branch-P. (b) Branch-AP. (c) Branch-P. (d) Branch-AP.

proposed FTNV-L design for various operating temperatures, we have performed TMR and read latency analysis for all faults at different temperatures. The results are extracted for both branch-P and branch-AP for a range of temperature values as illustrated in Fig. 12. As shown in Fig. 12(a) and (b), the TMR value decreases in each fault case with the increase in temperature. This rate of TMR declination with the increase in temperature is high for short-P and open-AP compared with the other faults. In addition, the range of TMR variations due to process variation is also high for these two fault cases. Nevertheless, the TMR_{eq} value remains significantly high at 100 °C. On the other hand, the open-P and short-AP faults, which have the worst case TMR values for "branch-P" and "branch-AP," respectively, demonstrate relatively less TMR declination rate and variations with the increase in temperature value. Furthermore, the TMR value of the short-AP fault can reach as low as less than 5% at 100 °C. The TMR variations for each fault case influence the read latency, as illustrated in Fig. 12(c) and (d). Short-P and open-AP, which have best TMR values, result in a very low read latency (less than 93 ps). On the contrary, the short-AP fault, which has the worst TMR value among all faults at 100 °C, can have very high read latency (upto 150 ps).

Overall, using our proposed FTNV-L architecture, the flip-flop functionality remains intact, since it is able to deliver a good enough TMR_{eq} value for all fault cases in the presence of process variation at different operating temperatures. In some cases, such as short-AP and open-P, the TMR_{eq} value found to be considerably low results in a high wakeup delay. However, this increase in wakeup delay is very low compared with the power-down durations. Hence, it has an overall negligible impact on the overall performance of the system. Beside this, in case the two read states are not distinguishable due to extreme variation conditions, the TMR value of individual MTJs can be increased (see Algorithm 1). If the TMR value of individual MTJs has already reached to its maximum due to the material or write current limitations, then another set of two parallel MTJs can be connected to the given structure to further increase the effective TMR value.

E. Area Analysis

In addition to the design parameters, we conducted an area analysis for our proposed FTNV-L design. Compared with the standard latch design, the only components added in our proposed design is the replacement of the two MTJs with the eight parallel/serial connected MTJs (see Figs. 2 and 5). Nevertheless, in general, MTJs are fabricated in another layer [42], and additionally, flip-flops are widely distributed all over the logic core unlike memory bitcells. Therefore, there would be no placement restrictions for MTJs for flip-flop designs as those can be easily placed above CMOS device layers, as illustrated in Fig. 13. The area of CMOS layers that also includes the conventional flip-flop design (i.e., $X * Y$) is significantly more than the area of the magnetic layer (i.e., $X' * Y'$). Therefore, the area of the CMOS layer eventually contributes to the total area of the flip-flop design.

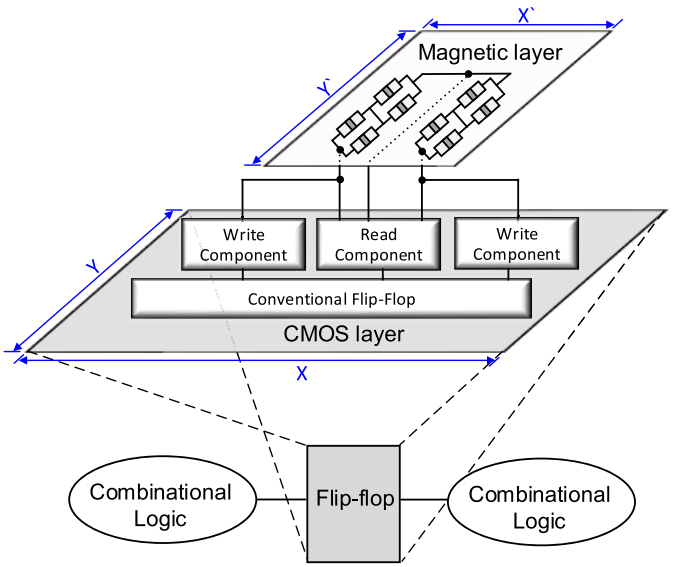


Fig. 13. Demonstration of magnetic and CMOS layers for area analysis (area of magnetic layer < area of CMOS layer).

In case the magnetic layer area is more than the CMOS part of the flip-flop, e.g., the MTJs are placed in a more relaxed manner or any other manufacturing constraints, they can be placed above the neighboring combinational logic cells as well, i.e., without impacting the chip area. Please note that the MTJ via sizes are negligible compared with the area of the CMOS layer. Due to this fact, the effective area of our proposed FTNV-L design remains the same as that of the standard latch design. However, the parallel/serial structure of MTJs in our proposed design requires an increased write current (around 2×) to ensure the switching in each MTJ. Therefore, the drive strength of the write component has to be increased by 3.4× compared with the standard latch design, which is, however, negligible in a custom layout design for a flip-flop.

F. Comparison With Triple Modular Redundancy

To illustrate the advantages of our proposed FTNV-L design, we compare it with a standard latch as well as 3MR. For the standard NV latch implementation, we use only two MTJs, one per each branch. For the 3MR implementation, we employ three standard NV latch designs with a voting circuit. The results of comparison for the three designs for a normal operation are summarized in Table II.

As specified in Table II, the TMR_{eq} value for each design is the same for the normal operation when fault-free MTJs are considered. However, in the presence of defective MTJs, the standard latch design is not functional at all, whereas our proposed FTNV-L design and 3MR are able to generate a fault-free output. Both of these designs can address a single MTJ fault per latch, but the 3MR has huge overhead because it uses three sets of standard NV latch designs and a voter circuit. For instance, compared with FTNV-L, the 3MR design has around 2× and 3× overheads for the read latency and energy, respectively. Here, the read operation means that the MTJ values are sensed in an NV shadow latch (during wakeup) and restored back to the normal flip-flop. The voter circuit in 3MR adds 120 ps to the delay and consumes a 6.4-fJ energy during restore. In the store operation, the flip-flop data are written into the NV shadow latch during the power-down mode. The storing delay is the same for those three designs because the three sets of MTJs in 3MR design can be written in parallel. However, similar to read, it has around 3× more energy as it requires total three sets of MTJ to switch its magnetization.

TABLE II
COMPARISON OF STANDARD LATCH AND 3MR DESIGN WITH PROPOSED FTNV-L DESIGN

Parameters	Standard NV Latch	3MR	Proposed FTNV-L
TMR_{eq} (%)	200	200	200
Read Latency (ps)	83	203	89
Read Energy (fJ)	12	42	15
Store delay (ps)	4056	4056	4065
Store energy (fJ)	390	1170	366
Leakage (nW)	37	155	97
Transistor count	16	72	16 †
MTJ count	2	6	8

†:TRANSISTOR WIDTH ARE INCREASED BY 3.4 X COMPARED TO STANDARD NV-LATCH

On the other hand, our proposed FTNV-L has almost similar results in comparison with the standard NV latch design. For instance, the backup energy for an NV latch is dominated by the write current as a continuous constant current requires to flow through the MTJs for a certain duration to switch their magnetizations. The equivalent resistance of our proposed design is also high because of the serial–parallel MTJ connections. To be more precise, the equivalent resistance of each branch for our proposed design becomes twice that of the standard design [see 2 and 3)]. Therefore, we need to pass an increased current for our proposed design in order to equalize the switching latency to that of the standard latch design. To achieve that, the drive strength of the write components is increased by 3.4× in the FTNV-L design compared with that of the standard NV latch design. Since similar write currents flow in both designs, the write energies are comparable. On the other hand, we are dealing at the processional switching regime where the switching current can vary significantly for almost the same latency. Due to this, in an automated simulated environment, with our proposed design, we could able to attain the same latency with a slightly lower current value, and hence we have a lower total energy compared with the standard latch design. Moreover, the increase in the width of transistors in the write component results in high leakage compared with the standard NV latch design, as illustrated in Table II. Please note that the leakage due to the read component for our proposed design remains the same as that for the standard latch design. Similar to the previous cases, the 3MR design has a high leakage due to more circuitry components as described before.

V. CONCLUSION

Nowadays, spintronic-based shadow latches are gaining attention as these are highly beneficial for leakage reduction.

This is because the storing devices of these latches, which are MTJ cells, have attractive attributes such as zero leakage and high access speed. Consequently, these latches very effective for instant-on/normally off computing in an SoC. However, these MTJ cells are highly susceptible to several manufacturing defects such as short oxide, open vias, and magnetic orientation of the FL does not switch. Due to this, the yield of the design is affected since a single defect in a flip-flop can lead to the failure of the entire backup strategy. Therefore, we proposed an FTNV-L, in which MTJs are serially and parallelly connected in a unique way to tolerate MTJ related faults. We have demonstrated the functionality of our proposed design in the presence of all MTJ faults under the influence of process variation and operating temperature. In addition, using the FTNV-L design, any single fault per latch can be tolerated at much reduced costs compared with the traditional solution based on 3MR.

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