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Phase Shifted Carrier Based Synchronized Sinusoidal PWM Techniques for Cascaded H-Bridge Multi Level Inverter

Saroj Kumar Sahoo, *Student Member, IEEE*, and Tanmoy Bhattacharya, *Member IEEE*

***Abstract*— This paper analyses synchronization strategy for cascaded H-Bridge multi level inverter (CHBMLI) topologies with carrier based sinusoidal phase shifted pulse width modulation (PSPWM) technique. In PSPWM technique a separate carrier is used for each H-Bridge (HB). The carriers are generally phase shifted from each other by π/x rad (x=No. of H-Bridges) for unipolar PWM. With the carrier frequency being an integer (odd/even) multiple of the fundamental frequency, it is observed that, the positions of zero crossings of the carriers with respect to the zero crossings of voltage references play an important role for maintaining quarter wave symmetry among multi level inverter (MLI) pole voltage waveforms. This paper analytically shows the conditions for half wave symmetry and quarter wave symmetry and experimentally verifies those conditions for PSPWM technique with a five level CHBMLI laboratory prototype.**

***Index Terms*—cascaded H-Bridge multilevel inverter, phase shifted carrier based PWM, synchronous PWM, half wave symmetry, quarter wave symmetry.**

I. INTRODUCTION

With the increasing demand of medium voltage and high power drives, the use of multilevel inverters is gradually becoming more and more important. This is due to reduced voltage stress on semiconductor devices, reduced harmonics in inverter output voltage and lesser electromagnetic interferences. For medium voltage and high power applications, the switching frequency and device ratings are limited [1]-[3]. Increasing the power rating by minimizing the switching frequency, while still maintaining reasonable power quality is an important requirement and a persistent challenge [2]-[3]. Hence, the use of multilevel inverters suitably distributes the stress among the semiconductor switches. Among the different multilevel inverter topologies, the cascaded H-Bridge (CHB) topology is a preferred choice for medium voltage drives for its modularity and this is also the target converter for the proposed PWM technique in this paper.

In high power and medium voltage applications, the power converters operate at low switching frequency. This is very well defined in the literature as low pulse ratio operation of the converters. The applications consist of traction drives (both VSI and CSI fed drives), grid applications (as bi-directional converters, active power filters) etc. As the pulse ratio is less in these power converters, lower order harmonics including sub-harmonics are introduced in line currents resulting in higher total harmonic distortion (THD). Hence, synchronization among PWM voltages is necessary. Along with synchronization, the PWM voltage should maintain half wave, quarter wave and three phase symmetries [4]-[5]. Reference [6] shows the advantages of maintaining the above waveform symmetries. The synchronization ensures the PWM voltage is free from the sub-harmonics. Three phase symmetry among the PWM voltages ensures the fundamental and the harmonics are balanced and also free from dc offset. Moreover, three phase symmetry also ensures that, the triplen harmonics are in phase and appear as zero sequence voltage with the advantage of not contributing to the ripple current. Half wave symmetry ensures the PWM voltages are free from even order harmonics. Although quarter wave symmetry does not eliminate any harmonics, it ensures that the existing fundamental and harmonics have only sine component and eliminates the possibility of phase error between the reference and the fundamental output voltage. Reference [7] proposes an optimal PWM scheme for two level inverters to reduce current harmonics with offline calculations of switching pattern. This optimized PWM strategy can also be extended to multi level inverters. Reference [8] shows the application of synchronized optimal PWM technique for a cascaded nine level inverter, where the average device switching frequency is limited to rated fundamental frequency. Reference [9] compares the performances of five level and seven level NPC inverters with synchronous optimal PWM technique. But, the synchronized optimal PWM technique is an offline calculation based technique. The switching angles are pre-calculated assuming steady state condition and this requires storage of large data for better accuracy. Reference [10] proposes a trajectory tracking control for three level NPC with synchronous optimal PWM technique. Reference [11] proposes the model predictive pulse pattern control for a five level NPC inverter with optimized PWM technique.

Selective harmonic elimination and selective harmonic mitigation PWM techniques are the other alternatives. Reference [12] shows the application of SHEPWM technique for cascade multi level inverters, whereas [13] shows the use of SHMPWM technique. But they are also offline calculation based PWM technique and require lookup tables for implementation, hence the more microcontroller memory space. References [14]-[16] show the application of online harmonic compensation scheme to improve the existing SHEPWM technique for high power converters. These references mainly focus on grid connected high power converters (i.e. current source rectifiers).

All the above multi level inverter PWM techniques (SOPWM, SHEPWM and SHMPWM Techniques, leaving online harmonic compensation scheme) are based on offline calculations. The calculation complexity increases with

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increase in number of voltage levels or increase in the number of commutation angles at lower modulation indexes. But the carrier based PWM techniques are independent of motor parameters, independent of optimization and does not require offline calculation or look-up tables to generate firing angles. Hence, carrier based PWM technique is well suited to multi level inverters although the harmonic contents of the inverter output pole voltage are not optimized. Two carrier based PWM techniques are available in literature for MLIs. They are:- (i) Level shifted PWM technique (LSPWM technique) (ii) Phase shifted PWM technique (PSPWM technique). But, the major challenge for the carrier based PWM techniques for MLIs is to position the zero crossings of carriers' with respect to the zero crossings of voltage references so that different symmetries among pole voltage waveforms can be maintained. For two-level inverters, synchronization with different symmetries is achievable if the zero crossings of the carrier matches with the zero crossings of the voltage references and the ratio 'p' ($p=f_c/f_s$ where f_c= carrier frequency and f_s=voltage reference frequency) is maintained to be an odd integer (multiple of 3). The carrier synchronization with the voltage references is sufficient for the Level Shifted PWM (LSPWM) technique for CHBMLIs, as only one synchronous carrier is sufficient to implement different voltage levels [17]. Hence, the pole voltage maintains all the basic properties of an ideal synchronous PWM technique. But, the power distribution and average device switching frequencies of different H-Bridges are different.

But this scenario is completely different for the PSPWM technique, as multiple phase shifted synchronous carriers are used for different H-Bridges. So, it is impossible to match the zero crossings of each carrier with the voltage reference zero crossings. Hence, the positions of the zero crossings of voltage references with respect to the zero crossings of carriers play an important role for maintaining different basic properties of an ideal synchronous PWM, as stated in the previous paragraph. This paper mainly deals with the analytical studies for maintaining half wave symmetry and quarter wave symmetry among CHBMLI pole voltage waveform with synchronous sinusoidal PSPWM technique. The carriers used for the analysis in this paper are generated from the instantaneous voltage references, as in [17]-[19] and always maintain an integer ratio p.

This paper is arranged as follows. Section II deals with the analytical explanation for PSPWM technique to maintain synchronization, three phase symmetry, half wave symmetry and quarter wave symmetry among CHBMLI pole voltage waveforms. Experimental results are given in section III and the paper is concluded in Section IV.

II. Conditions Of Phase Shifted Synchronous Pwm For Chbmli

The unipolar PWM technique is used for generating gate pulses for each H-Bridge. The H-Bridge pole voltage varies between 0 to $+V_{dc}$ when the sign of the voltage reference is positive and varies between 0 to $-V_{dc}$ when the sign of the voltage reference is negative (where V_{dc} is the input DC link voltage of the H-Bridge). For implementing unipolar PWM in an H-Bridge1 (Fig.1.(a)), a positive voltage reference R_1 is used to generate gate pulses for switches S_{11} and S_{12} of leg1 and a negative voltage reference R_2 is used to generate gate pulses for switches S_{13} and S_{14} of leg2. A common carrier C_{HB1} is used for both the legs in order to generate gate pulses. The resultant output pole voltage V_{HB1} is the algebraic summation of individual leg voltages i.e. $V_{HB1}=V_{HBL1}-V_{HBL2}$.

A. Verification of Synchronization

The synchronization between voltage reference and fundamental component of inverter output pole voltage can be maintained if the synchronous carrier frequency is n (n being any integer) times the voltage reference frequency. By maintaining the above condition the intersection points between the carrier and the voltage reference (i.e. in a fundamental cycle of the voltage reference) repeat after 2πrad (i.e. the next consecutive fundamental cycle of the voltage reference), hence synchronization is maintained.

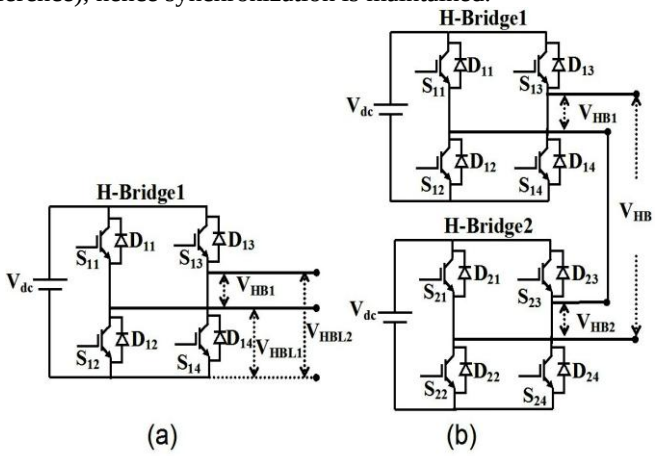

Fig. 1. (a) Single H-Bridge ; (b) Double cascaded H-Bridges.

B. Verification of Three Phase Symmetry & Half Wave Symmetry

With synchronous carriers having 3n times the fundamental frequency (n being any integer) being used for the PSPWM technique, three phase symmetry is always maintained among individual H-Bridge output pole voltage waveforms. Also, from Fig.2.(a) it can be observed that, for an odd integer ratio between the carrier and fundamental frequency, the region from πrad to 2πrad is equivalent to a mirror image of the region from 0rad to πrad with respect to x-axis(θ). Hence, the intersection points C_1 to C_6 are the mirror images of points from C_7 to C_{12} respectively. In fact, for an odd integer ratio, individual pole voltages of both the legs (V_{HBL1} and V_{HBL2}) of one H-bridge maintain half wave symmetry and hence their difference also maintains half wave symmetry. If the ratio is even then, individual pole voltages of both the legs (V_{HBL1} and V_{HBL2}) do not maintain half wave symmetry. But the waveform of V_{HBL1} from 0rad to πrad is an exact replica of V_{HBL2} from πrad to 2πrad and vice versa. Hence, their difference (i.e. $V_{HB1}= V_{HBL1}- V_{HBL2}$) maintains

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half wave symmetry. Hence, for an H-bridge, the half wave symmetry is satisfied for any carrier having its frequency equal to integer (odd/even) multiple of the fundamental frequency. Therefore, it can be concluded that the inverter pole voltage waveform maintains three phase and half wave symmetry for carriers having 3n times the fundamental frequency (n being any odd/even integer). It is therefore only necessary to determine the conditions for quarter wave symmetry in the inverter output pole voltage waveform.

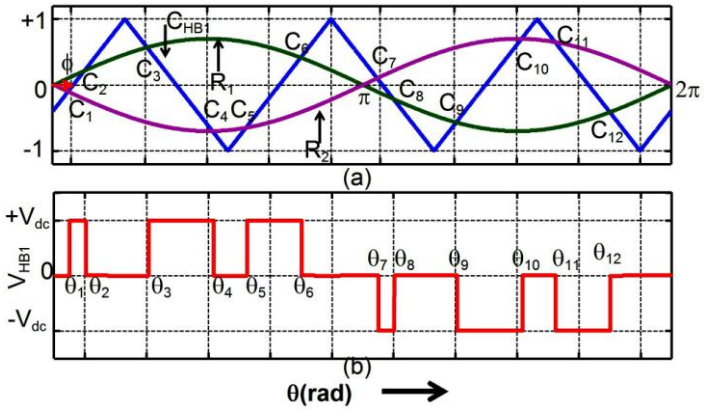

Fig. 2. (a) Carrier C_{HB1} lagging the normalized voltage references R_1 and R_2 by Φrad (f_c/f_s=3) ; (b) pole voltage V_{HB1}.

C. Determination of conditions for Quarter Wave Symmetry

1) Single H-Bridge

The quarter wave symmetry among pole voltage waveform of an H-Bridge (Fig.1.(a)) can be maintained, if the positive zero crossing of the voltage reference coincides with the positive zero crossing of the carrier. The normalized fundamental voltage references are sine waves with their amplitude less than or equal to one. The carriers are triangular waves with the magnitude of their positive and negative peak equal to one. Positive zero crossing means, the instantaneous values of these periodic waveforms have completed their negative half cycles and become zero before entering the positive half cycle. The carrier can be of two types. They are: - (i) In phase carrier (positive zero crossing of positive voltage reference coincides with the positive zero crossing of the carrier) (ii) Out of phase carrier (positive zero crossing of the positive voltage reference coincides with the negative zero crossing of the carrier). For carrier frequency being an odd multiple of the fundamental frequency, individual pole voltages of both the legs (V_{HBL1} and V_{HBL2}) maintain quarter wave symmetry ensuring quarter wave symmetry of the bridge output voltage V_{HB1}. For carrier frequency being an even multiple of the fundamental frequency, individual pole voltages of both the legs (V_{HBL1} and V_{HBL2}) do not maintain quarter wave symmetry. But their difference V_{HB1}= V_{HBL1}- V_{HBL2} maintains quarter wave symmetry.

If the carrier is phase delayed by π/2rad (where 2πrad is one carrier period), then the reverse phenomenon happens. Now, for carrier frequency being an even multiple of the fundamental frequency, individual pole voltages of both the legs (V_{HBL1} and V_{HBL2}) maintain quarter wave symmetry. Whereas, for carrier frequency being an odd multiple of the fundamental frequency, individual pole voltages of both the legs (V_{HBL1} and V_{HBL2}) do not maintain quarter wave symmetry. But their difference V_{HB1}= V_{HBL1}- V_{HBL2} maintains quarter wave symmetry. This can also be derived mathematically as shown in the following discussion. As a specific case, the carrier frequency is taken to be three times the fundamental frequency.

From Fig. 2, for maintaining quarter wave symmetry of the pole voltage waveform V_{HB1}, the constraint to be satisfied among voltage reference and carrier intersection points C_1 to C_6 is given by (1).

$$\theta_{7-l} = \pi - \theta_l \quad \text{for } l = 1, 2 \text{ and } 3 \qquad (1)$$

For l=1, the values of θ_1 and θ_6, at points C_1 and C_6 can be found out by equating the equations of voltage reference's and the carrier's. A small step is shown below to determine the equations of voltage references and carriers at points C_1 and C_6 with the help of the equations (2), (3), (4) and (5). Fig.3 shows the enlarged view of voltage references R_1 and R_2 along with carrier C_{HB1}. The point C_1 (whose trace is θ_1 along x-axis (θ)) is the intersection point between voltage reference R_2 and line AB which is one part of the carrier C_{HB1}.

The equation of the voltage reference at C_1 can be written as (2).

$$z_1 = -m\sin\theta_1 \qquad (2)$$

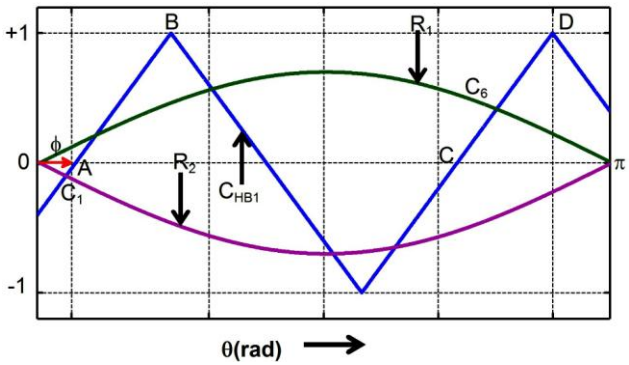

Fig. 3. Carrier C_{HB1} lagging the normalized voltage references R_1 and R_2 by Φrad (f_c/f_s=3).

The co-ordinates of the points A and B are (Φ, 0) and (Φ+π/6, 1) respectively. Hence, the equation of the line AB at point C_1 can be written as (3).

$$z_1 = \left(\frac{6}{\pi}\right)(\theta_1 - \phi) \qquad (3)$$

Similarly, the point C_6 is the intersection point between R_1 and line CD (which is a portion of carrier C_{HB1}).

The equation of the voltage reference at C_6 can be written as (4).

$$z_6 = m\sin\theta_6 \qquad (4)$$

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The co-ordinates of the points C and D are (2π/3+Φ, 0) and (Φ+5π/6, 1) respectively. Hence, the equation of the line CD at point C_6 can be written as (5).

$$z_6 = \left(\frac{6}{\pi}\right)\left(\theta_6 - \frac{2\pi}{3} - \phi\right) \quad (5)$$

Where z_1 & z_6 = y-axis values at points C_1 and C_6 respectively

m=modulation index of voltage references R_1 and R_2

From equations (2), (3), (4) and (5), the intersection angles θ_1 and θ_6 at points C_1 and C_6 can be found out by equating the equations of voltage references and carriers and can be written as (6) and (7) respectively.

$$-m\sin\theta_1 = \left(\frac{6}{\pi}\right)(\theta_1 - \phi) \quad (6)$$

$$m\sin\theta_6 = \left(\frac{6}{\pi}\right)\left(\theta_6 - \frac{2\pi}{3} - \phi\right) \quad (7)$$

Equation (7) can be modified as (8) by putting the constraint of quarter wave symmetry (2).

$$m\sin\theta_1 = \left(\frac{6}{\pi}\right)\left(\frac{\pi}{3} - \theta_1 - \phi\right) \quad (8)$$

By adding equations (6) and (8), the value of ϕ can be found as (9).

$$\phi = \pi/6\, rad \quad (9)$$

From equation (9) it can be observed that, the quarter wave symmetry of the pole voltage waveform V_{HB1} can be maintained if the zero crossing of the carrier lags the voltage reference zero crossing by π/6rad. Equation (9) gives the value of Φ in terms of the fundamental period of the voltage reference. If the value of Φ is expressed in terms of carrier period, then Φ should be equal to π/2rad for p=3. In a similar way the conditions for quarter wave symmetry at the other intersection points can also be derived and all of them arrive at the same conclusion. Similarly, when the zero crossing of the carrier leads the voltage reference zero crossing by an angle Φ=π/2rad, quarter wave symmetry among pole voltage waveform V_{HB1} in a single H-Bridge can be maintained.

Equation (9) shows the condition for quarter wave symmetry among pole voltage waveforms V_{HB1}, when p=3. For carriers having frequency p=3n (where n=1, 3, 5, 7, 9,……,etc.) times the fundamental frequency and with their zero crossings lagging the fundamental voltage reference zero crossings by Φrad, the condition for quarter wave symmetry among pole voltage waveform V_{HB1} can be found by using (10)-(14). Here, for quarter wave symmetry, the constraint is given by (10).

$$\theta_{6n+1-l} = \pi - \theta_l \quad \text{for } l = 1, 2, \ldots 3n \quad (10)$$

For l=1

$$-m\sin\theta_1 = \left(\frac{6n}{\pi}\right)(\theta_1 - \phi) \quad (11)$$

$$m\sin\theta_{6n} = \left(\frac{6n}{\pi}\right)\left\{\theta_{6n} - \phi - \frac{(3n-1)}{3n}\pi\right\} \quad (12)$$

By putting the constraint of quarter wave symmetry $\theta_{6n} = \pi - \theta_1$ in (12), one gets

$$m\sin\theta_1 = \left(\frac{6n}{\pi}\right)\left(\frac{\pi}{3n} - \theta_1 - \phi\right) \quad (13)$$

By adding (11) and (13), the value of ϕ can be found as (14).

$$\phi = \left(\frac{1}{3n}\right)\left(\frac{\pi}{2}\right) rad \quad (14)$$

Hence, by representing Φ in terms of carrier period, it can be concluded that, for maintaining quarter wave symmetry among pole voltage waveform V_{HB1}, the zero crossing of the carrier should lag the zero crossing of the voltage reference by π/2 rad.

In a similar way, conditions for quarter wave symmetry can be analytically derived for an even integer ratio of carrier and fundamental frequency with zero carrier phase shift, odd integer ratio with zero carrier phase shift and even integer ratio with π/2 rad phase shift. Therefore, the conditions for maintaining quarter wave symmetry among pole voltage waveform V_{HB1} in a single H-Bridge can be summarized as below:-

I. The zero crossings of the voltage references should coincide with the zero crossings of the carrier.

II. The zero crossings of the carrier should be placed at ±π/2 rad with respect to the zero crossings of the voltage references (where 2π rad denotes one carrier period).

If we have only two H-Bridges per phase, then their individual carriers should be phase shifted from each other by π/2rad. One carrier can satisfy condition I and the other carrier can satisfy condition II as described above. The output voltage of both the H-Bridges will maintain quarter wave symmetry and hence their sum will also maintain quarter wave symmetry. But, as the number of cascaded H-Bridges increases (more than two) it is not possible to place all the zero crossings of carriers at 0rad or ±π/2rad with respect to the zero crossings of voltage references, as the phase difference between (π/x rad for x≥2 number of cascaded H-bridges) zero crossings of the carriers decreases. For two cascaded H-Bridges, the next section deals with the conditions for maintaining quarter wave symmetry among resultant pole voltage V_{HB}, where the zero crossings of the carriers are placed other than 0rad or ±π/2rad with respect to the voltage reference zero crossings.

2) Two Cascaded H-Bridges

For two cascaded H-Bridges (Fig.1.(b)), it is also possible to maintain quarter wave symmetry among the resultant pole voltage waveform V_{HB}, in spite of individual bridge voltage waveforms V_{HB1} and V_{HB2} not maintaining quarter wave symmetry. Two approaches are possible and pointed below. Both the approaches are analyzed in the coming sections.

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- Zero crossings of carriers C_{HB1} and C_{HB2} are placed on both sides of the zero crossing of carrier C^{ref1} (where C^{ref1} is a fictitious carrier whose zero crossings are in phase with the zero crossings of the voltage references R_1 and R_2).
- Zero crossings of carriers C_{HB1} and C_{HB2} are placed on both sides of the zero crossing of carrier C^{ref2} (where C^{ref2} is a fictitious carrier whose one positive or negative peak appears in the same instant as that of the zero crossings of the voltage references R_1 and R_2).

In other words, it can be stated that C^{ref1} satisfies condition I and C^{ref2} satisfies condition II. The carriers C_{HB1} and C_{HB2} are used for generating gate pulses of H-Bridge1 and H-Bbridge2 respectively in a double cascaded H-Bridge (Fig.1.(b)). The voltage reference R_1 is used for generating the gate pulses of S_{11}, S_{12}, S_{13} and S_{14}. The gate pulses of S_{13}, S_{14}, S_{23} and S_{24} are generated by voltage reference R_2. Fig.4 and Fig.5 show the voltage references, R_1 and R_2 along with carriers C_{HB1} and C_{HB2} with respect to the fictitious carriers C^{ref1} and C^{ref2} respectively.

a) Approach I

Fig.4 shows the case, where the zero crossing of carrier C_{HB1} leads the zero crossing of fictitious carrier C^{ref1} by $\Phi_1$rad, whereas the zero crossing of carrier C_{HB2} lags the zero crossing of C^{ref1} by $\Phi_2$rad for p=3. Fig.4.(b) shows that the resultant pole voltage V_{HB}, does not maintain quarter wave symmetry. In order to show the intersection points and intersection angles, only the half cycle of each waveform is shown in Fig.4. For maintaining quarter wave symmetry of the resulting pole voltage V_{HB}, the condition to be satisfied among voltage reference and carrier intersection points C_1 to C_{12} is given by (15).

$$\theta_{13-l} = \pi - \theta_l \quad \text{for } l\text{=1, 2, 3, 4, 5 and 6} \qquad (15)$$

For l=1, the values of θ_1 and θ_{12}, at points C_1 and C_{12} can be found out by equating the equations of voltage references and carriers and can be written as (16) and (17) respectively.

$$-m\sin\theta_1 = \left(\frac{6}{\pi}\right)(\theta_1 - \phi_2) \qquad (16)$$

$$-m\sin\theta_{12} = -\left(\frac{6}{\pi}\right)(\theta_{12} - \pi + \phi_1) \qquad (17)$$

Equation (17) can be modified as (18) by putting the condition of quarter wave symmetry (15).

$$m\sin\theta_1 = \left(\frac{6}{\pi}\right)(\phi_1 - \theta_1) \qquad (18)$$

By adding (16) and (18), the condition for quarter wave symmetry can be found out as (19).

$$\phi_1 = \phi_2 \qquad (19)$$

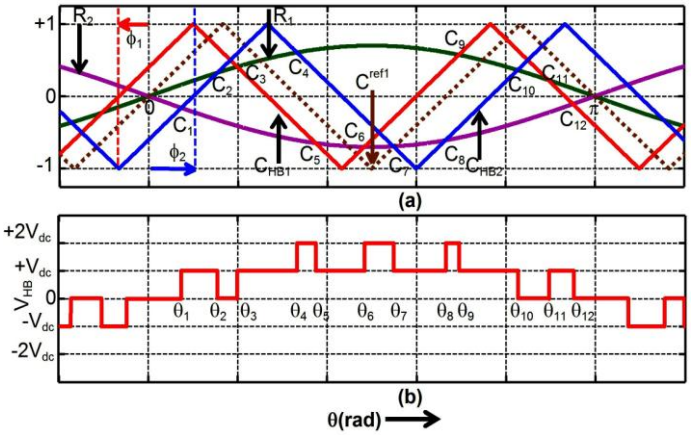

Fig. 4. (a) References R_1 and R_2 and Carriers C_{HB1} and C_{HB2} when C^{ref1} is in phase with voltage references (p=3); (b)V_{HB}.

From (19) it can be observed that, the quarter wave symmetry among resultant pole voltage waveform V_{HB} can be maintained if $\Phi_1 = \Phi_2$, i.e. the zero crossings of carriers C_{HB1} and C_{HB2} are placed equidistantly from the zero crossings of carrier C^{ref1}. In a similar way the conditions for quarter wave symmetry at the other intersection points can also be derived and each pair of intersection points will result in the condition of (19).

Equation (19) shows the condition for quarter wave symmetry among pole voltage waveform V_{HB}, when p=3. For carriers having frequency p=3n (where n=1, 2, 3, 4, 5, 6, 7, 8, 9, 10,……,etc.) times the fundamental frequency and with their zero crossings lagging and leading the zero crossing of C^{ref1} by $\Phi_1$rad and $\Phi_2$rad respectively, the condition for quarter wave symmetry among resultant pole voltage waveform V_{HB} can be found by using the above approaches (equations (16)-(19)) and the final conclusion is same as (19).

b) Approach II

In the second approach (Fig.5), the zero crossing of carrier C_{HB1} leads the zero crossing of carrier C^{ref2} by $\Phi_1$rad, whereas the zero crossing of carrier C_{HB2} lags the zero crossing of carrier C^{ref2} by $\Phi_2$rad for p=3. Fig.5.(b) shows that the resultant pole voltage V_{HB} does not maintain quarter wave symmetry. For maintaining quarter wave symmetry among resultant pole voltage waveform V_{HB}, the condition to be satisfied among voltage reference and carrier intersection points C_1 to C_{12} is given by (20).

$$\theta_{13-l} = \pi - \theta_l \quad \text{for } l\text{=1, 2, 3, 4, 5 and 6} \qquad (20)$$

For l=1, the values of θ_1 and θ_{12}, at points C_1 and C_{12} can be found out by equating the equations of voltage references and carriers and can be written as (21) and (22) respectively.

$$-m\sin\theta_1 = \left(\frac{6}{\pi}\right)\left(\theta_1 - \frac{\pi}{6} + \phi_1\right) \qquad (21)$$

$$m\sin\theta_{12} = \left(\frac{6}{\pi}\right)\left(\theta_{12} - \frac{5\pi}{6} - \phi_2\right) \qquad (22)$$

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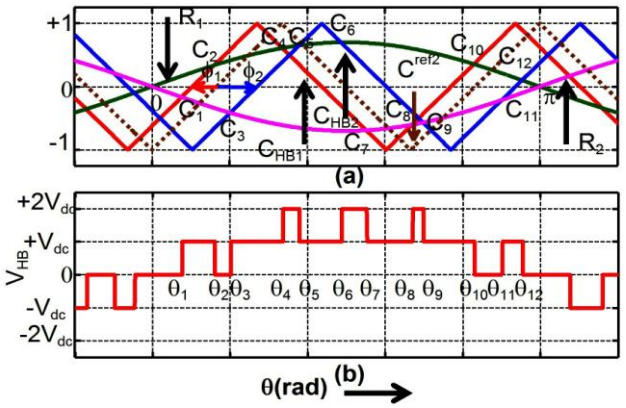

Fig. 5. (a) References R_1 and R_2 and Carriers C_{HB1} and C_{HB2} when C^{ref2} is $\pi/2$ rad lagging with respect to voltage references (p=3)); (b)V_{HB}.

By putting the condition of quarter wave symmetry (20) in (22), (22) can be simplified as (23).

$$m\sin\theta_1 = \left(\frac{6}{\pi}\right)\left(\frac{\pi}{6} - \theta_1 - \phi_2\right) \qquad (23)$$

By adding (21) and (23), the condition for quarter wave symmetry can be found out as (24).

$$\phi_1 = \phi_2 \qquad (24)$$

From (24) it can be observed that, here also the quarter wave symmetry among resultant pole voltage waveform V_{HB} can be maintained if $\Phi_1=\Phi_2$, i.e. the zero crossings of carriers C_{HB1} and C_{HB2} are equidistant from the zero crossing of carrier C^{ref2}. The condition of quarter wave symmetry can also be shown as $\Phi_1=\Phi_2$, if the zero crossing of carrier C^{ref2} lead $\pi/2$rad from the zero crossing of the voltage references. Same condition for quarter wave symmetry can be derived for carriers having frequency p=3n (where n=1, 2, 3, 4, 5, 6, 7, 8, 9, 10,……,etc.) times the fundamental frequency.

c) Conditions for quarter wave symmetry with x(≥2) numbers of cascaded H-Bridges

TABLE-I
Three Cascaded H-Bridges

Position of C_{HB1}	Position of C_{HB2}	Position of C_{HB3}
∓ π/3rad	0rad	± π/3rad
∓ π/6rad	± π/6rad	± π/2rad
∓ π/6rad	∓ π/2rad	∓ 5π/6rad
0rad	∓ π/3rad	∓ 2π/3rad

Zero crossing of voltage reference is placed at 0rad

From the previous discussions on quarter wave symmetry, it can be extended that there can be multiple approaches of maintaining quarter wave symmetry among the resultant pole voltage waveform. e.g. if there are two H-bridges, then one approach can be to put one carrier coinciding with C^{ref1} and the other carrier coinciding with C^{ref2}. Another approach can be to put two carriers such that one carrier leads C^{ref1} (or C^{ref2}) by $\pi/4$rad and the other carrier lags C^{ref1} (or C^{ref2}) by $\pi/4$rad. If there are three cascaded H-Bridges, then the possible approaches are given in the form of a table in TABLE-I. Hence, it is important to determine the general philosophy of placing the carriers with respect to the voltage reference to ensure quarter wave symmetry for a (2x+1) level cascaded H-Bridge multilevel inverter (x number of cascaded H-Bridges). The philosophy is analytically explained in this section. For this analysis, position of a carrier is defined by the position of the zero crossing of the carrier.

Case:-I (With one carrier being at 0^{th} position (0^{th} carrier), **k** numbers of carriers are present on the left hand side **(between points A and B)** and **(x-k-1)** numbers of carriers are present on the right hand side **(between points D and H)** of the 0^{th} carrier). It is to be noted that the zero crossing of voltage reference R coincides with the zero crossing of the carrier placed at 0^{th} position.

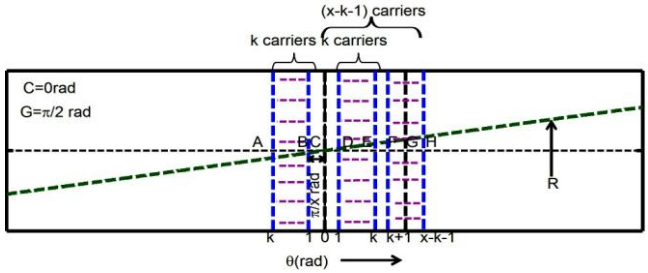

Fig. 6. Positive zero crossing (point C) of normalized voltage reference R coincides with the positive zero crossing (point C) of 0^{th} carrier.

Fig.6 shows the case:-I, where k numbers of carriers are present on the left hand side of 0^{th} carrier and (x-k-1) numbers of carriers are present on the right hand side of 0^{th} carrier. The zero crossings of each carrier are separated from each other by π/x rad. The positive zero crossing of the normalized voltage reference R coincides with the positive zero crossing of 0^{th} carrier. It can also be observed from Fig.6 that, equal numbers (k numbers) of carriers are present around point C between points A-B and D-E. Hence, the resultant output pole voltage waveform of the H-Bridges using these carriers maintains quarter wave symmetry. Also, the pole voltage output of the H-Bridge using 0^{th} carrier maintains quarter wave symmetry. Hence, for maintaining quarter wave symmetry among the resultant pole voltage waveform of x numbers of cascaded H-Bridges it should be shown that the positive zero crossings of $(k+1)^{th}$ and $(x-k-1)^{th}$ carriers (among (x-2k-1) carriers between points F-H) are present equidistantly from $\pi/2$rad (point G).

The distances between points G-F and H-G are calculated as (25) and (26).

$$FG = \frac{\pi}{2} - (k+1)*\left(\frac{\pi}{x}\right) = \left(\frac{x-2k-2}{2}\right)*\left(\frac{\pi}{x}\right) \qquad (25)$$

$$GH = (x-k-1)*\left(\frac{\pi}{x}\right) - \frac{\pi}{2} = \left(\frac{x-2k-2}{2}\right)*\left(\frac{\pi}{x}\right) \qquad (26)$$

Equations (25) and (26) show that the positive zero crossings of $(k+1)^{th}$ and $(x-k-1)^{th}$ carriers are placed equidistantly from $\pi/2$rad.

The above explanation can be extended to even/odd numbers of cascaded H-bridges. For an even number of cascaded H-Bridges one carrier is present at $\pi/2$rad and equal

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numbers of carriers are present on both sides of π/2rad. For an odd number of cascaded H-Bridges no carrier is present at π/2rad and equal numbers of carriers are present on both sides of π/2rad.

Case:-II (**k** numbers of carriers are present on the left hand side **(between points A and B)** and **(x-k)** numbers of carriers are present on the right hand side **(between points D and H)** of the point C (the mid-point of points B and D) and the positive zero crossing of voltage reference R coincides with point C). There is no 0^{th} carrier in this case.

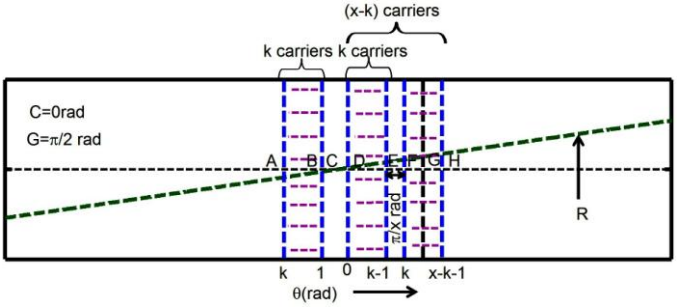

Fig. 7. Positive zero crossing (point C) of normalized pole voltage reference R is placed in between the positive zero crossings (points B and D of two adjacent carrier pairs).

Fig.7 shows the case:-II, where k numbers of carriers are present on the left hand side of point C and (x-k) numbers of carriers are present on the right hand side of point C. The zero crossings of each carrier are separated from each other by π/xrad. The positive zero crossing of the normalized voltage reference R coincides with the point C (mid-point of the two adjacent carriers). It also can be observed from Fig.7 that, equal numbers (k numbers) of carriers are present around point C between points A-B and D-E. Hence, the resultant output pole voltage waveform of the H-Bridges using these carriers maintains quarter wave symmetry. For maintaining quarter wave symmetry among the resultant pole voltage waveform of x numbers of cascaded H-Bridges it should be shown that the positive zero crossings of k^{th} and $(x-k)^{th}$ carriers (among n-2k carriers between points F and H) are present equidistantly from π/2rad (point G).

The distances between points G-F and H-G are calculated as (27) and (28).

$$FG = \frac{\pi}{2} - \left\{ k * \left(\frac{\pi}{x} \right) + \frac{\pi}{2x} \right\} = \left(\frac{x - 2k - 1}{2} \right) * \left(\frac{\pi}{x} \right) \quad (27)$$

$$GH = \left\{ (x - k - 1) * \left(\frac{\pi}{x} \right) + \frac{\pi}{2x} \right\} - \frac{\pi}{2} = \left(\frac{x - 2k - 1}{2} \right) * \left(\frac{\pi}{x} \right) \quad (28)$$

Equations (27) and (28) show that the positive zero crossings of k^{th} and $(x-k)^{th}$ carriers are placed equidistantly from π/2rad.

The above explanation can be extended to even/odd numbers of cascaded H-bridges. For an even number of cascaded H-Bridges no carrier is present at π/2rad and equal numbers of carriers are present on both sides of π/2rad. For an odd number of cascaded H-Bridges one carrier is present at π/2rad and equal numbers of carriers are present on both sides of π/2rad.

d) Generalized Condition for maintaining Quarter Wave Symmetry

TABLE-II

x Cascaded H-Bridge Multilevel Inverters. (There are x phase shifted carriers with π/x phase difference between any two adjacent carriers)

CONDITION FOR QUARTER WAVE SYMMETRY f_c/f_s=3n (where n=1,2,3,4,… etc.)	
1	Zero crossing of voltage reference coincides with zero crossing of any carrier
2	Zero crossing of voltage reference is placed at the mid-point between positive (or negative) zero crossings of any two adjacent carriers

TABLE-II summarizes the conditions to maintain quarter wave symmetry among resultant pole voltage waveform for x (x≥2) numbers of cascaded H-Bridge inverter. It is to be noted that, it is required to satisfy any one condition mentioned in Table II in order to maintain quarter wave symmetry. It is observed that if any one of these conditions is maintained, then leaving out the in-phase and π/2rad-phase carriers (if they exist), equal number of carriers will be placed on both sides of C^{ref1} (as shown in Fig. 4) or C^{ref2} (as shown in Fig. 5) or both.

e) Power distribution between each cell

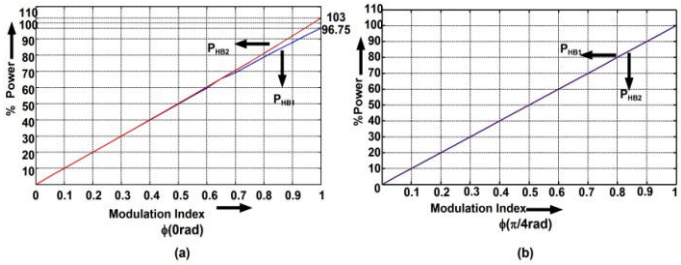

Fig. 8. Power distribution between each H-Bridge of a five level CHBMLI (a) Positive zero crossing of C_{HB1} coincides with the zero crossings of R_1 and R_2 and (b) Zero crossings of R_1 and R_2 are placed at ±π/4rad with respect to the zero crossings of C_{HB1} and C_{HB2} for p=3.

For PSPWM technique with a high switching frequency, each H-Bridge handles equal power. But when the ratio p becomes low, unequal power distribution occurs between the cascaded H-Bridges. The reason is, same current passes through each module. But, their instantaneous output voltage waveforms are different. Hence, the instantaneous power integrated over a complete fundamental cycle may result is different values. Fig.8 shows that, when the zero crossings of the voltage references coincide with the zero crossing of one of the carriers, condition of unequal distribution of power between the H-Bridges occur. But when the zero crossings of the voltage references are placed equidistantly between the zero crossings of the two carriers, then each H-Bridge shares equal power. It is to be noted that this is just a specific example. In a general x CHBMLIs unequal power distribution may happen for lesser value of p.

f) Fundamental displacement and harmonic distortion without maintaining QWS

In order to study the importance of maintaining QWS, with p=3, the angle Φ (distance between the zero crossing of

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voltage reference and the positive zero crossing of C_{HB1}) is varied in H-Bridge1 (Fig.1.(b)) from 0 rad to π/6rad (0rad to π/2rad in terms of carrier period). Hence, the positive zero crossing of C_{HB2} varies from π/6rad to π/3rad with respect to the fundamental reference (π/2 rad to π rad in terms of carrier period). Fig.9.(a) shows that, for a single H-bridge (H-bridge1), maximum phase displacement (α_{HB1}) occurs between the voltage reference and the fundamental of pole voltage for Φ=π/4rad (in terms of carrier period). At both the extreme ends, i.e. at Φ=0rad (Condition of QWS) and Φ=π/2rad (Condition of QWS) the phase displacements are zero. Similarly, the Fig.9.(b) shows at Φ=0rad (Condition of QWS), Φ=π/4rad (Condition of QWS) and Φ=π/2rad (Condition of QWS) the phase displacements are zero for the double cascaded H-Bridges. Fig.9 also shows that the phase displacement for a single HB is higher comparing to the double cascaded HBs. If the number of cascaded H-bridges are further increased, then the phase displacement reduces to lesser values and hence, for a very large number of cascaded H-bridge cells, with phase shifted carriers, phase displacement of the resultant pole voltage is negligible even without perfect quarter wave symmetry.

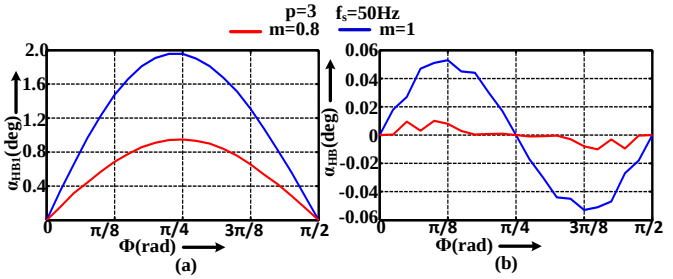

Fig. 9. Fundamental voltage displacements of (a) Single H-Bridge and (b) Double cascaded H-Bridges for p=3 , f_s=50Hz and with modulation indexes of 0.8 and 1.

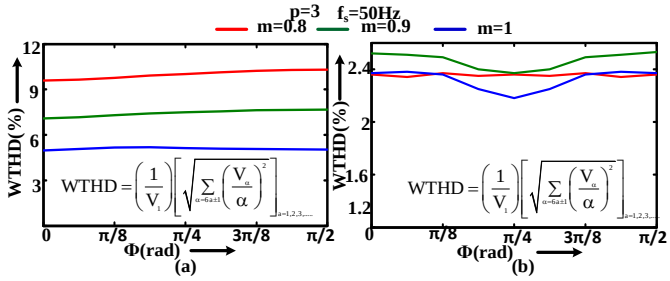

Fig. 10. WTHD (line voltage V_{RY}) variations w.r.t the variation of Φ for higher modulation indexes (0.8 t0 1) for (a) single H-Bridge and (b) double cascaded H-Bridges with p=3 , f_s=50Hz.

In order to check the variation of the harmonic profile of the line voltage with respect to the variation of Φ (distance between the zero crossing of voltage reference and the positive zero crossing of C_{HB1}), the WTHD plots for line voltage V_{RY}, are plotted in Fig.10 for a three level (single H-bridge) and five level (two cascaded H-bridges) CHBMLI, for three modulation indexes 0.8, 0.9 and 1, with p=3 and f_s=50Hz. For single H-bridge, the positions Φ = 0rad and π/2rad are the conditions for quarter wave symmetry whereas for two cascaded H-bridges, the positions 0rad, π/4rad and π/2rad are the conditions of maintaining QWS among pole voltage waveform. Here, it can be observed that for a single H-bridge, WTHD varies almost in a flat profile. For two cascaded H-bridges, for higher modulation indexes, minimum WTHD occurs at Φ=π/4rad (i.e. the zero crossing of voltage reference is placed at the midpoint of the zero crossings of two carriers) which is a valid condition for quarter wave symmetry. The improvement is of course too small for consideration in a practical situation.

The proposed PSPWM technique does not give a better harmonic voltage profile compared to the techniques proposed in [8], [20] and [21], as the gate pulses are generated without any harmonic minimization technique. References [8] and [21] show the applications of SOPWM technique, where the switching instants are calculated for minimizing certain voltage harmonics along with minimization of current distortion. Reference [20] calculates the switching instants by minimizing the required voltage harmonics along with the constraint of minimizing the pulsating torque. The proposed PSPWM technique does not claim to give reduced current or torque ripple. But it can be stated that with lower p and reduced number of H-Bridges the proposed PSPWM technique gives better performance compared to the traditional PSPWM technique (the zero crossings of voltage references can be put arbitrarily irrespective of zero crossings of the phase shifted carriers). Further, as the proposed technique is a carrier based scheme, synchronization in a highly dynamic situation like field oriented control can be achieved with much lesser computational complexity compared to the schemes of [8], [20], [21] etc. But, with the increase in the number of H-Bridges and p the harmonic profile is almost similar to a traditional PSPWM technique [22]-[25].

III. Experimental Results

The synchronization strategy for the CHBMLIs is verified with a three phase squirrel cage induction motor drive (parameters are given in APPENDIX) operated in open loop V/f mode, which is supplied from a five level three phase CHBMLI laboratory prototype. The dc-link voltage V_{dc} of each H-Bridge is maintained at 100V during the experiment to operate the motor at half of the rated voltage. Both the conditions for maintaining quarter wave symmetry in the resultant pole voltage patterns V_{HB}, as discussed in Section II, are tested experimentally. For experimental verification, the ratio p is kept at 3 in order to show the pole voltage pulse patterns clearly. Fig.11.(a) shows that the zero crossings of carrier C_{HB1} coincides with the zero crossings of voltage references R_1 and R_2. Fig.11.(b) shows that the individual bridge voltage waveforms V_{HB1} and V_{HB2} along with the resultant pole voltage waveform V_{HB} maintain half wave symmetry and quarter wave symmetry. Fig.11.(d) shows that the zero crossings of voltage references R_1 and R_2 are placed equidistantly in between the zero crossings of carrier C_{HB1} and C_{HB2}. Fig.11.(e) shows the individual bridge voltages V_{HB1} and V_{HB2} and resultant pole voltage V_{HB}. It can be observed that the individual bridge voltages maintain half wave symmetry, but not quarter wave symmetry, whereas the resultant pole

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voltage waveform maintains half wave symmetry and quarter wave symmetry. Fig.11.(c) and (f) show that the three phase symmetry is maintained among three phase pole voltage waveforms.

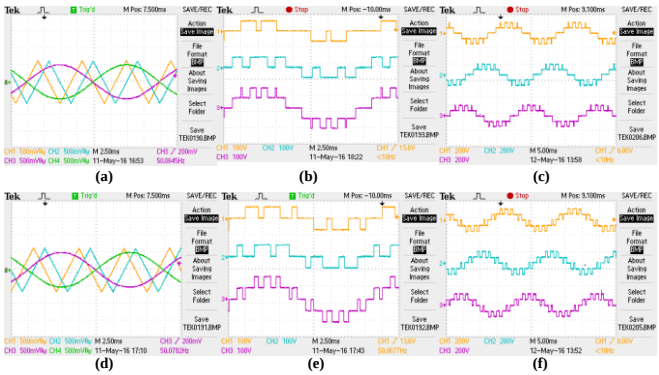

Fig. 11. (a) and (d) Ch.1:-C_{HB1}, Ch.2:-C_{HB2}, Ch.3:-R_1 and Ch.4:-R_2; (b) and (e) Ch.1:-V_{HB1}, Ch.2:-V_{HB2} and Ch.3:-V_{HB} and (c) and (f) Ch.1:-V_{RO}, Ch.2:-V_{BO} and Ch.3:-V_{YO} when (i) the zero crossings of voltage references are in phase with the zero crossings of carrier C_{HB1} and (ii) the zero crossings of voltage references are placed at the midpoint of the positive zero crossings of carriers C_{HB1} & C_{HB2} for $f_c=3f_s$ with a modulation index of 0.8 and f_s=50Hz.

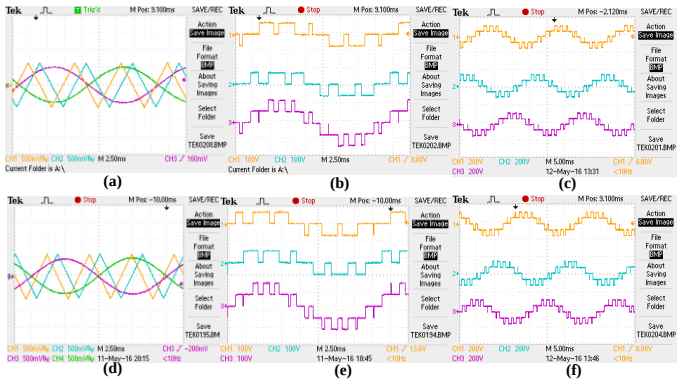

Fig. 12. (a) and (d) Ch.1:-C_{HB1}, Ch.2:-C_{HB2}, Ch.3:-R_1 and Ch.4:-R_2; (b) and (e) Ch.1:-V_{HB1}, Ch.2:-V_{HB2} and Ch.3:-V_{HB} and (c) and (f) Ch.1:-V_{RO}, Ch.2:-V_{BO} and Ch.3:-V_{YO} when (i) the zero crossings of voltage references are placed at $+\pi/12$rad with respect to the zero crossings of carrier C_{HB1} for $f_c=3f_s$ with a modulation index of 0.8 and f_s=50Hz and (ii) for f_c=160Hz with a modulation index of 0.8 and f_s=50Hz.

In order to compare the proposed PSPWM technique, the experiment is done with two sets of carriers C_{HB1} and C_{HB2} where the zero crossings of voltage references, R_1 and R_2 are placed at an angle of $+\pi/12$ rad with respect to the zero crossing of C_{HB1}. The ratio p is kept at 3. This condition ensures the three phase symmetry and half wave symmetry. But quarter wave symmetry is not maintained. Fig.12.(a) shows the above mentioned conditions for voltage references, R_1 and R_2 and carriers C_{HB1} and C_{HB2}. Fig.12.(b) shows that the individual bridge voltages V_{HB1} and V_{HB2} along with resultant bridge voltage V_{HB} maintain half wave symmetry without maintaining quarter wave symmetry. Fig.12.(c) shows the three phase pole voltages maintain three phase symmetry. Similarly, a pair of carriers C_{HB1} and C_{HB2} having frequency of 160Hz (asynchronous PWM) are used to generate the same waveforms. The results are shown in Fig.12.(d), (e) and (f). It can be observed that the individual bridge voltages along with the resultant bridge voltage do not maintain half wave symmetry, quarter wave symmetry or three phase symmetry. During the experiment, the modulation index of the voltage references is kept at 0.8 with a frequency of 50Hz.

The harmonic spectrums of line voltages (V_{RY}) with and without waveform symmetries and synchronization are compared in Fig.13 and Fig.14. Fig.13.(b) and (d) show the harmonic spectrum of line voltage V_{RY} which is the result of maintaining quarter wave symmetry for one of the conditions mentioned in TABLE-II. Fig.14.(b) shows the harmonic spectrum of the line voltage V_{RY}, when there is no QWS present among the pole voltage waveform. The harmonic spectrums of Fig.13.(b), Fig.13.(d) and Fig.14.(b) are free from even order voltage harmonics, as the pole voltage waveform maintains HWS. The harmonic spectrums of Fig.13.(b), Fig.13.(d) and Fig.14.(b) show that the line voltage is free from triplen order voltage harmonics. Hence, the three phase symmetry is maintained among the three phase pole voltage waveforms. The WTHD of line voltage V_{RY} for the above three cases are almost equal. The minor difference is already shown in Fig. 10. Fig.14.(d) shows that the harmonic spectrum of the line voltage V_{RY} contains a small dc offset for 160Hz phase shifted carriers. This DC offset is observed in the harmonic spectrum, as the harmonic spectrums are plotted for one fundamental cycle. For an asynchronous carrier, the pole voltage waveform along with the line voltage waveform are not periodic considering one fundamental period of the voltage reference. But, if the harmonic spectrums are plotted based on a data of a time period in which both the fundamental and the carriers complete integer number of cycles, then this DC offset will not be observed in the harmonic spectrums of pole voltage as well as line voltage. Rather, it will appear as subharmonic component. The subharmonic frequency is very bad for drive's application, because it may match with the mechanical resonance frequency of the drive shaft. Moreover, it is a common practice to use inverter output filters for drives with long distance between the converter and the motor. It can be observed that the frequency spectrum with synchronized carrier are of concentrated nature, whereas, with asynchronous carrier are of distributed nature. Hence, design of output filter is more economical for synchronized carrier based approach where the ratio between the carrier frequency and the fundamental frequency (p) is very low. Also, with asynchronous carriers even order voltage harmonics are observed in the line voltage waveform, due to the absence of HWS among pole voltage waveform.

Some experimental results are also taken for a three phase five level CHBMLI fed squirrel cage induction motor drive with p=6 and f_s=50Hz. This experiment is done in order to show that the proposed PSPWM technique is also valid for carriers having a frequency ratio p being even. Fig.15.(a) and Fig.16.(a) show the individual bridge voltages along with the resultant bridge voltage of a single phase five level CHBMLI with the conditions for maintaining QWS among pole voltage V_{HB} (as mentioned in TABLE-II). Fig.15.(a) shows that the individual bridge voltages along with the resultant bridge

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voltage maintain HWS and QWS, when the zero crossing of one carrier coincides with the zero crossing of voltage references. Fig.16.(a) shows the individual bridge voltages do not maintain QWS but the resultant bridge voltage maintains QWS when the zero crossing of the voltage references are placed at the midpoint of the zero crossings of the carriers.

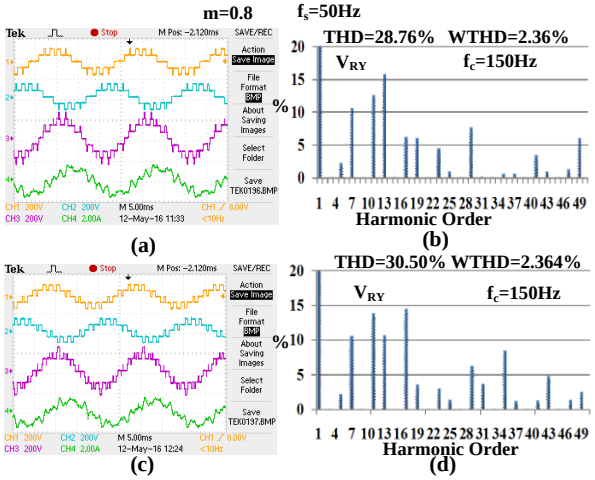

Fig. 13. (a) and (c) Ch.1:-V_{RO}, Ch.2:-V_{YO}, Ch.3:-V_{RY} and Ch.4:-i_R; (b) and (d) Harmonic spectrum of V_{RY} for (i) the zero crossings of voltage references are in phase with the zero crossings of carrier C_{HB1} and (ii) the zero crossings of voltage references are placed at the midpoint of the positive zero crossings of carriers C_{HB1} & C_{HB2} for $f_c=3f_s$ with a modulation index of 0.8 and f_s=50Hz.

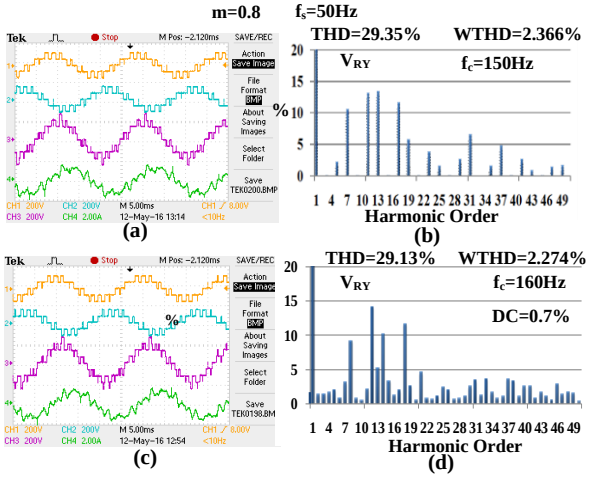

Fig. 14. (a) and (c) Ch.1:-V_{RO}, Ch.2:-V_{YO}, Ch.3:-V_{RY} and Ch.4:-i_R; (b) and (d) Harmonic spectrum of V_{RY} for (i) the zero crossings of voltage references are placed at $+\pi/12$ rad with respect to the zero crossings of carrier C_{HB1} for $f_c=3f_s$ and (ii) f_c=160Hz with a modulation index of 0.8 and f_s=50Hz.

Fig.15 and Fig.16 also show the FFT spectrums of pole voltage V_{RO} and line voltage V_{RY} for p=6 and f_s=50Hz with a modulation index of 0.8. The harmonic spectrums of pole voltage V_{RO} in Fig.15.(b) and Fig.16.(b) show that even order voltage harmonics are absent. This signifies the pole voltage waveform V_{RO} maintains HWS. The harmonic spectrums of line voltage V_{RY} in Fig.15.(d) and Fig.16.(d) show the triplen harmonics are absent from the line voltage waveform V_{RY}. This shows that the three phase pole voltage waveforms maintain three phase symmetry. The THD of all waveforms are calculated and WTHD is also shown for line voltage V_{RY}. The WTHD of the line voltage V_{RY} shows that the effect of lower order voltage harmonics is identical in both the conditions mentioned in TABLE-II. This happens as with higher p, the WTHDs of line voltages are almost identical irrespective of the different conditions for maintaining QWS.

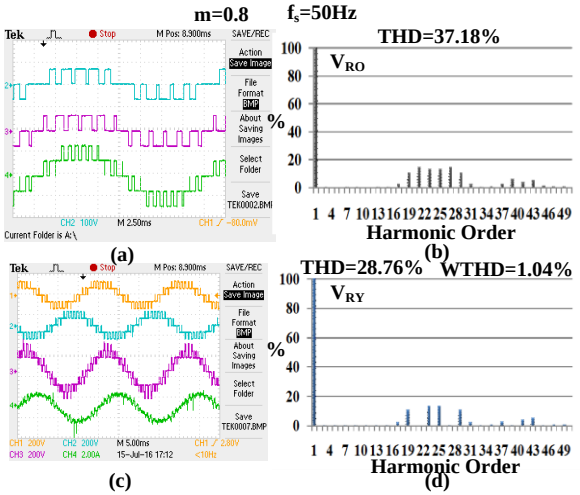

Fig. 15. (a) Ch.2:- V_{HB1}, Ch.3:- V_{HB2} and Ch.4:- V_{HB}; (b) Harmonic spectrum of V_{RO}; (c) Ch.1:-V_{RO}, Ch.2:-V_{YO}, Ch.3:-V_{RY} and Ch.4:-i_R and (d) Harmonic spectrum of V_{RY} when the zero crossings of voltage references are in phase with the zero crossings of carrier C_{HB1} for $f_c=6f_s$ with a modulation index of 0.8 and f_s=50Hz.

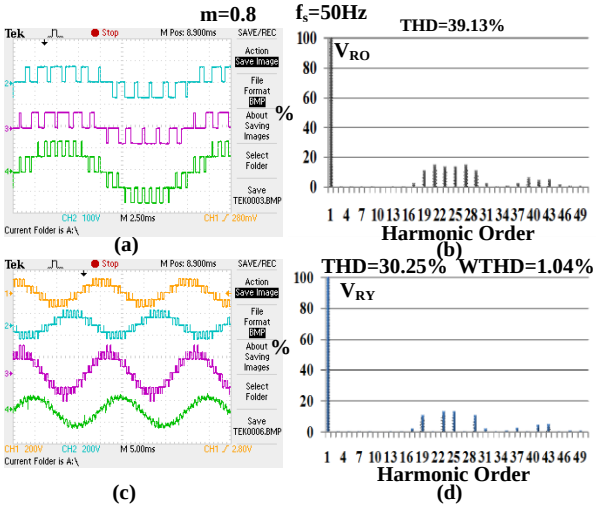

Fig. 16. (a) Ch.2:- V_{HB1}, Ch.3:- V_{HB2} and Ch.4:- V_{HB}; (b) Harmonic spectrums of V_{RO}; (c) Ch.1:-V_{RO}, Ch.2:-V_{YO}, Ch.3:-V_{RY} and Ch.4:-i_R and (d) Harmonic spectrums of V_{RY} when the zero crossings of voltage references are placed at the midpoint of the zero crossings of carriers C_{HB1} & C_{HB2} for $f_c=6f_s$ with a modulation index of 0.8 and f_s=50Hz.

Fig.17 and Fig.18 are taken with the help of a three phase five level CHBMLI fed squirrel cage induction motor drive (during the open loop V/f control). Fig.17 also shows the results for maintaining quarter wave symmetry among the resultant pole voltage waveform for double cascaded H-Bridges with p=9. Hence, the conditions tabulated in TABLE-II, are valid for any 3n (where n=1, 2, 3,..... etc.) carrier. Fig.18.(b) shows the transition of the R-Phase current i_R during the shifting between the synchronous carriers having p=9 to p=3. Fig.18.(b) shows a smooth transition between the

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carriers having p=9 to p=3, as no significant transients are observed in motor current i_R. The results of Fig.18 are taken when the zero crossings of voltage references are placed at the midpoint of the positive zero crossings of carriers C_{HB1} and C_{HB2}. This approach is selected for experimental verification as the power handled by each bridge is equal for lower p and higher values of modulation indexes as discussed in section II.

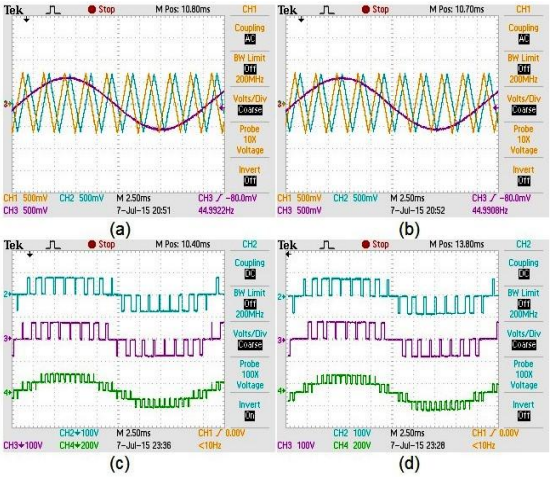

Fig. 17. (a) and (b) Ch.1:-C_{HB1}, Ch.2:-C_{HB2}, Ch.3:-R_1 and Ch.4:-R_2 and (c) and (d) Ch.1:-V_{HB1}, Ch.2:-V_{HB2} and Ch.3:-V_{HB} when (i) the zero crossings of voltage references are placed at the midpoint of the positive zero crossings of carriers C_{HB1} & C_{HB2} and (ii) the zero crossings of voltage references are in phase with the zero crossings of carrier C_{HB2} for $f_c=9f_s$ with a modulation index of 0.9 and f_s=45Hz.

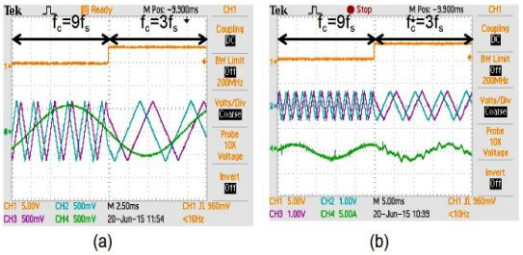

Fig. 18. (a) Ch.1:-Transition signal,Ch.2:-C_{HB1},Ch.3:-C_{HB2} and Ch.4:-R-Phase voltage reference and (b) Ch.1:-Transition signal,Ch.2:-C_{HB1},Ch.3:-C_{HB2} and Ch.4:-i_R during the transition from p=9 to p=3.

In order to compare the proposed PSPWM technique for higher number of cascaded H-Bridges, the experiment is also performed with a nine level cascaded H-Bridge multilevel inverter. Fig.19 shows the results for two possible combinations of placement of zero crossings of voltage references with respect to the positive zero crossings of the carriers. Fig.19.(a) and (b) show the waveforms of individual bridge voltages along with the resultant bridge pole voltage respectively, when the zero crossing of voltage reference co-incides with the positive zero crossing of one of the carriers. Fig.19.(d) and (e) show the waveforms of individual bridge voltages along with the resultant bridge pole voltage respectively, when the zero crossing of voltage references is placed at the midpoint of the positive zero crossings of two adjacent carriers. The harmonic spectrums of pole voltage waveform V_{RO} are shown in Fig.19.(c) and (f) respectively. The even order harmonics are eliminated from the harmonic spectrum of the pole voltage waveform, as all the waveforms maintain HWS. It can be stated that, with the increase in the number of voltage levels, the harmonic spectrum is shifted to higher orders and their magnitude also comes down. All the plots are done for a modulation index (m) of 0.8 at a pole voltage reference frequency (f_s) of 50Hz and p=3.

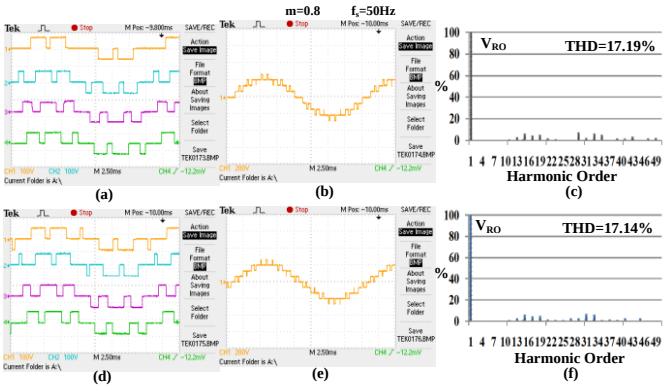

Fig. 19. (a) and (d) Ch.1:-V_{HB1}, Ch.2:-V_{HB2}, Ch.3:-V_{HB3} and Ch.4:-V_{HB4}; (b) and (e) Ch.1:-V_{HB} and (c) and (f) Harmonic spectrum of V_{HB} when (i) the positive zero crossing of one carrier co-incides with the zero crossing of fundamental voltage reference and (ii) the zero crossing of fundamental voltage reference is placed at the midpoint of two adjacent carriers with a modulation index of 0.8, f_s=50Hz and p=3 for a single phase nine level CHBMLI.

IV. Conclusion

This paper shows analytically the possible positions of zero crossings of the carriers with respect to the zero crossings of voltage references for the CHBMLIs using the PSPWM technique for maintaining three phase symmetry, half wave symmetry and quarter wave symmetry. Three phase and half wave symmetries are maintained among the H-Bridge pole voltage waveforms for any position of zero crossing of carrier with respect to the zero crossing of the voltage references, as long as carrier frequency is 3n time the fundamental frequency with n being any integer (even/odd). But the positions of zero crossings of the carriers with respect to the zero crossings of voltage references are important for maintaining quarter wave symmetry among the pole voltage waveforms. This is analytically studied in this paper for single and two cascaded H-Bridges and generalized for x number of cascaded H-Bridges. The study is experimentally verified with the help of a three phase five level CHBMLI laboratory prototype and the results are presented.

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APPENDIX

A. Squirrel Cage Induction Motor Parameters

Stator phase voltage(V)	400
Rated supply frequency(Hz)	50
Stator phase current(Amp)	7.7
Shaft power(kW)	3.73
Pole pairs	3
Full load rated speed(rpm)	960
Magnetizing inductance(mH)	190
Stator and rotor leakage inductance (mH)	8.8
Stator resistance (Ω)	0.9
Rotor resistance (Ω)	0.78
Rotor inertia (kg-m^2)	0.1
Viscous coefficient (N-m/radpsec)	0.003

Saroj Kumar Sahoo (Student M'16) received received the B.E. degree in electrical engineering from the Biju Pattnaik University of Technology, Rourkela, India, in 2008, and the M.Tech. Degree in machine drives and power electronics from the Indian Institute of Technology (IIT), Kharagpur, in 2011. He is currently working towards his Ph.D. degree in the Electrical Engineering Department, Indian Institute of Technology (IIT), Kharagpur.

His research interests include control of traction drives, low switching frequency PWM techniques , multilevel converters, etc.

Tanmoy Bhattacharya (M'11) received the B.E. degree in electrical and electronics engineering from the National Institute of Technology, Tiruchirapalli, India, in 2002, and the M.Sc. (Eng.) and Ph.D. degrees in power electronics from the Indian Institute of Science (IISc), Bangalore, in 2005 and 2009, respectively.

He also worked as a Research Fellow at National University of Singapore, Singapore. He is currently working as an Assistant Professor in the Electrical Engineering Department, Indian Institute of Technology (IIT), Kharagpur. His research interests include hybrid electric vehicles, traction drives, wind, solar hybrid systems, renewable powered micro-grids, etc.