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Photovoltaic Module Integrated Standalone Single Stage Switched Capacitor Inverter with Maximum Power Point Tracking

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***Abstract*— A Switched Capacitor (SC) based inverter that tracks the maximum power point (MPP) of a photovoltaic (PV) source and generates a pure sine output is presented. To enable integration with the PV module, efficiency and compactness are maximized with a single stage topology that tracks the MPP of the PV source, boosts the input dc voltage and generates a regulated ac output in a standalone configuration with scope for grid connected applications. The SC inverter is realized with multiple identical SC blocks controlled by sinusoidal pulse width modulation and load dependent output capacitor adjustment. A detailed steady state analysis is done and a mathematical model is derived to understand the interdependence of various inverter parameters on each other and to optimally choose the inverter components. A hardware prototype of the standalone single stage SC inverter that operates from a 60V / 70W PV module and delivers a 110V rms, 50Hz output is wired to demonstrate the functioning of the proposed MPP tracking inverter under different operating conditions. An inversion efficiency > 95%, tracking efficiency > 97% and THD < 4% have been practically achieved. All the details of this work are presented.**

***Index Terms*— Inverter, Maximum power point tracking, Module integrated, Photovoltaic source, Switched Capacitor**

I. INTRODUCTION

Switched capacitor (SC) power conditioners achieve power conversion by electronically switching capacitors between the input power source and the load. SC power conditioners are extensively used for dc-dc conversions. A lot of literature dealing with analysis [1], control methods [2], topologies [3] efficiency issues [4] and applications of SC dc-dc converters are available. The most distinguishing feature of SC dc-dc converters is the absence of inductors and transformers for handling power, leading to higher power densities compared to conventional dc-dc converters [5-6]. The other relative advantages of SC dc-dc converters are efficiency over 95% under certain operating conditions [7] for a wide range of load variation, amenability for mass production and cost effectiveness, ruggedness and compactness due to the absence of magnetic components, easy thermal management by heat steering techniques [4] and a wide spectrum of output power ranging from a few milli-watts for single chip power solutions [8] to over a kilowatt of output power [6].

SC power conditioners are not restricted only to dc-dc applications. SC power conditioners have been used for dc-ac, ac-ac [9] and ac-dc [10] conversions also. However, compared to SC dc-dc converters, the use of SC power conditioners for these applications has been relatively less explored.

Since this paper deals with SC dc-ac inverters, we now survey the literature available in this field. Reference [11] discusses a 24W output SC based dc-ac inverter. The input is 12Vdc and the output is 110V rms, 50Hz sinusoidal output with 64 steps. The topology has two SC sub circuits each containing 15 basic SC cells where each cell is composed of a capacitor, two MOSFETs and two diodes. Y. H. Chang has introduced two types of SC boost inverters in [12] and [13]. The one in [13] has n stages of SC voltage doublers for boosting the voltage to 2^n times the dc source voltage. It is followed by an H-Bridge for generating ac output. The topology in [12] requires two equal dc voltage sources of opposite polarities to generate each half of the output sine wave. A total of $2(n - 1)$ SC cells are required for realizing an n level sinusoidal output. Ke Zou *et al.* have analyzed a modular SC cell based inverter topology powered from a dc source in [14]. Two types of SC cells are discussed. One is the full cell that can be used for dc-ac inversion and the other is the half cell that can perform both dc-dc and dc-ac operations. To realize a $2n + 1$ level inverter, n full cells are required. An SC transformer is used in [15, 16] to invert a dc input V_S to a sine output. The scheme in [15] gives a bucked sine output whereas the one in [16] gives a boosted output. A 5 level high voltage SC inverter powered from a battery for driving the capacitive loads of electroluminescent displays is described in [17]. Ye *et al* describe an SC step up multilevel inverter in [18]. It is a combination of a multilevel dc-dc converter and an H-bridge for unfolding. The inverter provides $2n + 3$ levels on the output voltage using n capacitors and $n + 5$ switches. An SC multilevel inverter consisting of an SC front end stage powered from a 12V dc source followed by an H-Bridge is used in [19] for high frequency ac power distribution. A multilevel boost type SC inverter powered from an 8V dc source for an inductive load is explained in [20]. All the above SC inverters are powered from constant dc voltage sources like batteries.

Global efforts are on to reduce the cost of photovoltaic (PV) power production to \$1/W. Lowering the cost of the associated power electronics from \$0.22/W to about \$0.1/W is also part of this effort [21-22]. Integrating the power electronics with the PV module is a step towards economization. SC power conditioners are excellent candidates for integration with PV sources compared to conventional power conditioners due their relative advantages like compactness, ruggedness, ease of mass production, cost effectiveness, efficiency etc. Hence in this paper we propose MPP tracking SC inverters for PV module integration.

Existing literature related to the use of SC power conditioners in conjunction with PV sources are surveyed. References [23] and [24] are some of the early attempts that have studied the feasibility to use SC dc-dc converters for

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tracking the maximum power point (MPP) of PV sources. SC converter based voltage equalization and current equalization methods are explored in [25] and [26] respectively for mitigating the problems of module mismatch in series connected PV modules. An SC power converter capable of performing MPP tracking of individual PV modules such that only the mismatch power between PV modules is processed while converging each of the modules to their MPP is proposed in [27]. Scott *et al.* [28] have presented an SC based two stage PV module integrated inverter. The first stage is an SC based dc-dc converter that quadruples the input voltage while the cascaded second stage is a five level inverter that also does the MPP tracking. The transformer less SC based topology investigated in [29] is a PV source fed grid connected solution without voltage boosting capability while that of [30] is a two stage boost topology with grid interface.

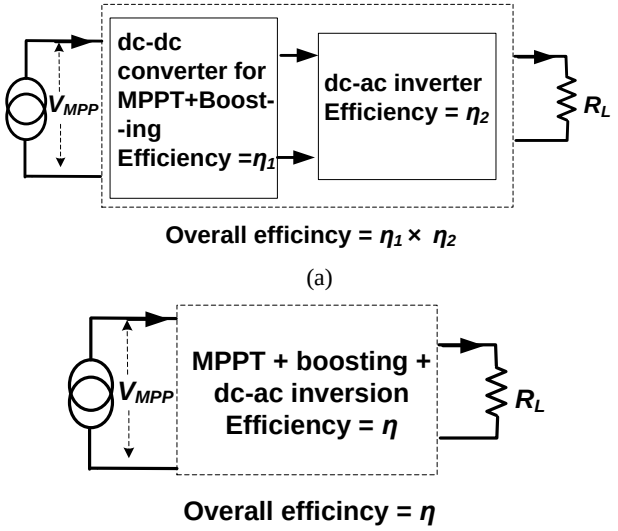
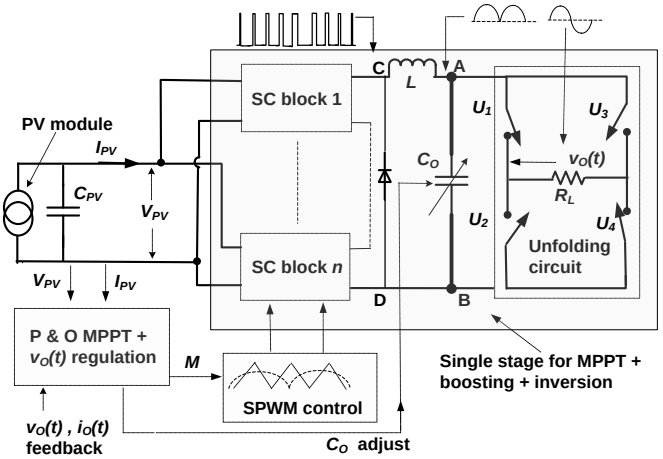


Fig. 1. Comparison of (a) two stage and (b) single stage solutions for MPP tracking, boosting and inversion.

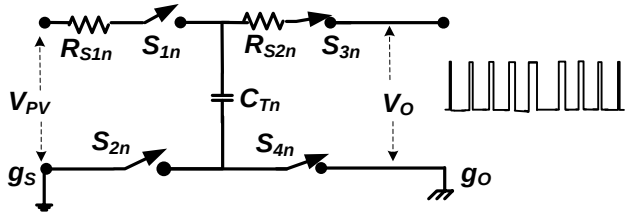
Processing power from a PV source to get an ac voltage involves (1) MPP tracking (2) voltage boosting since the PV module voltage is usually lower than the required ac voltage (3) dc to ac inversion. This is usually achieved with two stages as shown in Fig. 1(a) with an overall efficiency of $\eta_1 \times \eta_2$. Accomplishing this with a single stage is not only more efficient but is also cost effective due to lower component count as shown in Fig. 1(b). The SC converter based schemes available till date for this [28, 30] and many of the proposals with conventional converters are two staged solutions. Jain and Agarwal [31] have surveyed the single stage solutions with conventional converters. Due to the obvious advantages of single stage topologies, we propose a PV module integrated single stage SC based topology that tracks the MPP as well as boosts and inverts the PV source voltage (≈ 60V) to 110V rms, 50Hz ac voltage. Most of the schemes available in literature are grid connected systems. Unlike these, the scheme introduced in this paper is a standalone system which can support loads directly connected to its output. However it may be modified for grid connected applications also. To the best of authors' knowledge a single stage, boost type, standalone solar PV inverter based on SC converters has not been reported so far in the literature.

II. Proposed Topology

This section presents the block diagram of the proposed SC based inverter, the process of dc to ac inversion and MPP tracking and the algorithm for standalone operation.



(a)



(b)

Fig. 2. PV module integrated single stage SC inverter (a) overall configuration (b) n^{th} basic SC building block of the inverter.

A. DC-AC conversion, SPWM and MPP tracking

The overall schematic of the SC based PV module integrated single stage boost MPP tracker and inverter is given in Fig. 2(a). The SC block that forms the basic building block of the inverter is shown in Fig. 2(b). This is a buck topology since a steady dc voltage $V_O < V_{PV}$ can be obtained by connecting an output filter capacitor [4]. In the absence of the output filter capacitor, voltage pulses as shown in Fig. 2(b) are obtained at the output. When S_{1n} and S_{2n} close, C_{Tn} charges. Then there is a dead time when all switches are open. Next S_{3n} and S_{4n} close. Now C_{Tn} discharges into the load. Thus, this topology generates a floating output voltage with respect to the source V_{PV}. By connecting the inputs of multiple basic SC blocks in parallel across the input source V_{PV} and their floating outputs in series, the topology can be used as a buck or boost depending on the duty ratio (D_1 and D_2) of the switches. When the duty ratio is low, such a topology acts like a buck topology and as the duty ratio increases, the topology acts like a boost topology.

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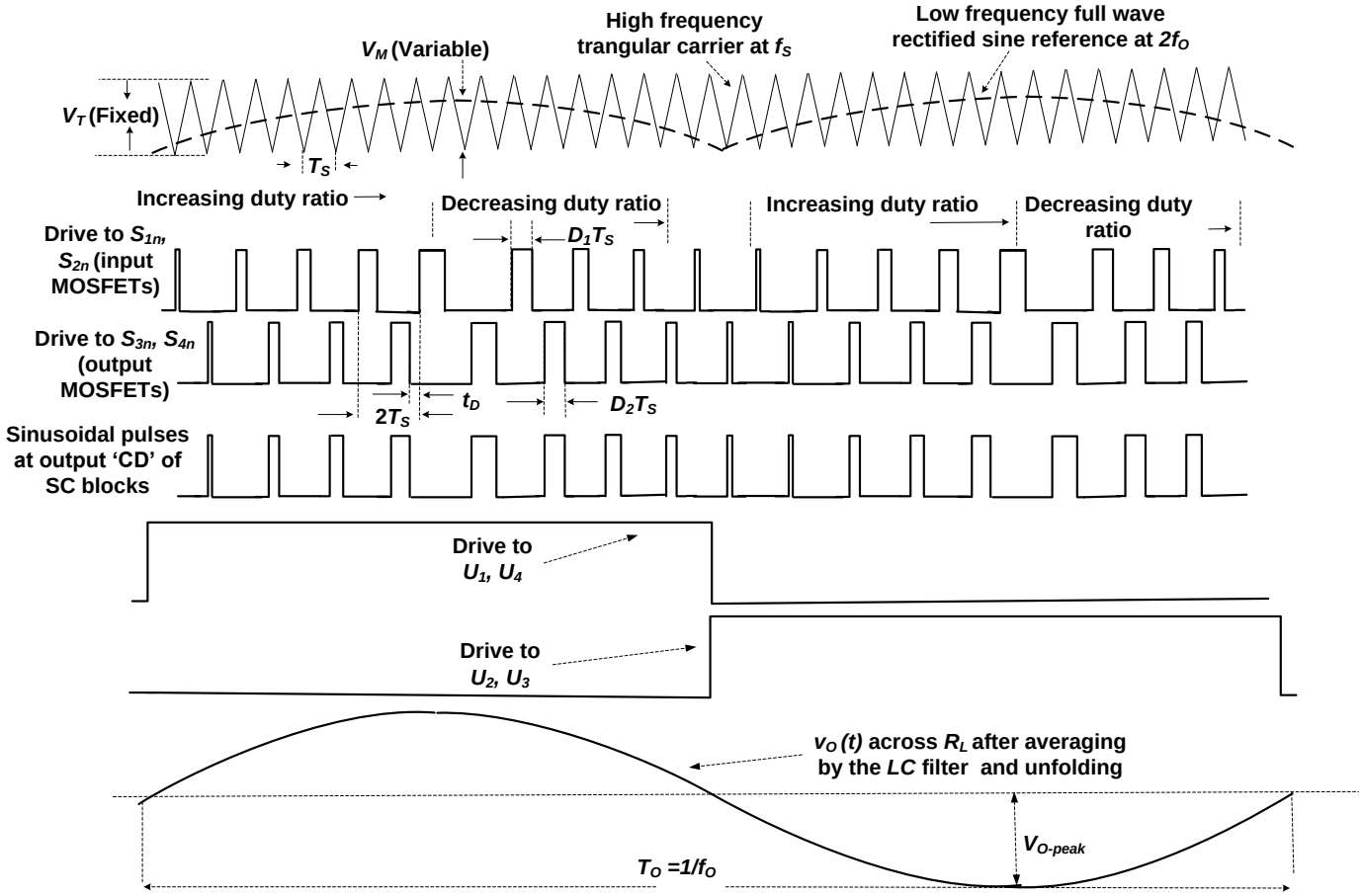

Fig. 3. SPWM for generating a sine output by comparing a high frequency triangular carrier with a low frequency full wave rectified sine reference

Sinusoidal Pulse Width Modulation (SPWM) is used due to its simplicity and ease of implementation. To minimize the distortion during zero crossing of $v_O(t)$ (cross over distortion) the output capacitor C_O is altered for different ranges of output load. This is explained in sections V and VI.

Fig. 3 shows the generation of SPWM drive signals for the SC inverter by a single SPWM generator. It involves the comparison of a low frequency full wave rectified sine reference of peak amplitude V_M at frequency $2f_O$ (where f_O is the frequency of $v_O(t)$) with a high frequency triangular carrier of fixed peak amplitude V_T at frequency f_S. Let $1 \le N \le f_S / f_O$. Since $f_S >> f_O$ (Fig. 3), the ON duration D_1T_S of the input switches (S_{1n} and S_{2n}) of all the n SC blocks and the ON duration D_2T_S of the output switches (S_{3n} and S_{4n}) of all the n blocks are almost equal i.e. $D_1T_S \approx D_2T_S$ where D_1 and D_2 generated by SPWM are given by:

$$D_1 \approx D_2 = M\left|\sin(2\pi f_O N T_S)\right| \; ; M = \frac{V_M}{V_T} \qquad (1)$$

S_{1n} and S_{2n} of all the SC blocks are turned ON simultaneously for a duration D_1T_S for charging the C_T of all the SC blocks parallelly from V_{PV}. Then the input switches are turned OFF. There is a dead-time t_D when all the switches S_{1n} to S_{4n} are turned OFF. After t_D, all the output switches S_{3n} and S_{4n} are turned ON together for the interval D_2T_S to discharge C_T serially. Thus, the charge transfer capacitors C_T are switched between the input source V_{PV} and output V_O with the pulse width increasing and decreasing in a sinusoidal manner as per (1). The output ground g_O is floating with respect to the input ground g_S (Fig. 2b). This causes the series connection of all the C_T s to boost V_{PV} when the output switches are turned ON and input switches are turned OFF. The output LC filter averages the boosted SPWM pulses to yield a full wave rectified sine output across AB in Fig. 2(a). The unfolding circuit comprising switches U_1 to U_4 , driven as shown in Fig. 3, at a low frequency f_O unfolds alternate full wave sine waveforms to yield a bidirectional sine output $v_O(t)$ across R_L.

As per [32], a stage of an inverter is defined as the section where high frequency switching and power conversion is done. In the topology of Fig. 2, only the SC blocks operate at a high frequency f_S, whereas the unfolding circuit switches at a low frequency f_O. Also, the conduction losses in the unfolding stage can be minimized by choosing low $R_{DS\text{-}ON}$ MOSFETs. Thus the losses here are small compared to the losses in the high frequency SC stage. Hence it is a single stage topology. Furthermore, since only capacitors are used in the high frequency power conversion stage the topology may be classified as an SC topology. An inductor is used only in the output filter to achieve a THD < 5%.

There is a unique operating point on the array's Power-Voltage (P-V) curve called the Maximum Power Point (MPP), where the power generation is maximum. The P-V curve and the MPP shift depending on the solar illumination intensity and angle, module temperature etc. To extract maximum power from the PV array it is necessary to operate the array at the MPP. The 'perturb and observe' (P & O) method elaborated in [33] is employed here to track the MPP due to its

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simplicity. The operating point on the module's *P-V* curve is altered by incrementing or decrementing the modulation index $M = V_M / V_T$. When M is increased, the SPWM control pulse width increases and more power is extracted from the PV module and vice versa.

B. Output voltage regulation for stand-alone application

As per the literature survey presented in the previous section, it is seen that most of the PV source fed inverters are grid connected. The advantage of grid connected systems is that since the inverter outputs are tied to the grid, the output voltage $v_O(t)$ is automatically regulated. Also, since the grid is

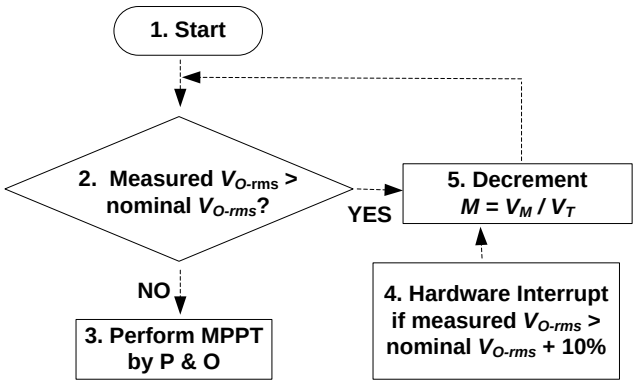

Fig. 4. Flowchart for regulating $v_O(t)$ for standalone operation and performing MPP tracking.

an infinite sink, it can always absorb all the ac output power of the inverter. In a PV source fed standalone inverter, we have the following observations *(a)* For a fixed load, $v_O(t)$ increases when the power generation from the PV source increases and vice versa; *(b)* For a fixed power generation, $v_O(t)$ increases when the load decreases and vice versa. Since loads cannot tolerate a widely varying supply voltage, especially high voltages, it is mandatory to regulate the upper limit of $v_O(t)$ in standalone systems.

By controlling M, the MPP of the PV module is tracked and regulation of $v_O(t)$ is achieved. The rms value of the sinusoidal output ($V_{O\text{-rms}}$) is restricted to within +10% of the desired nominal value. In the flowchart of Fig. 4, initializations are carried out in block 1. $V_{O\text{-rms}}$ is measured in block 2. If the measured value of $V_{O\text{-rms}}$ < the nominal rms, the standard P & O MPP tracking algorithm of block 3 tracks the MPP of the PV source. At any point of time if the measured $V_{O\text{-rms}}$ exceeds the nominal $V_{O\text{-rms}}$ by 10%, a hardware interrupt (block 4) causes M to be decremented in steps (block 5). This causes the decrease of $V_{O\text{-rms}}$ up to just below the nominal $V_{O\text{-rms}}$ after which the P & O MPP tracking algorithm of block 3 takes over.

Two different operating modes will result due to the above algorithm. In mode 1, R_L is such that it is able to absorb all the power generated by the PV source such that $V_{O\text{-rms}}$ will not exceed 10% of the nominal $V_{O\text{-rms}}$. Now it is mandatory to track the MPP and the P & O MPP tracking algorithm of block 3 will be continuously executed. The actual value of $V_{O\text{-rms}}$ will depend on the prevailing load on the inverter and generation from the PV module. A limit on the minimum value of $V_{O\text{-rms}}$ has not been set. If the PV source's MPP is not tracked in this scenario, we will be operating at a sub-optimal point on the panel's *P-V* curve. In mode 2, the inverter may be on light load and the PV panel may be well illuminated. Now if the MPP is tracked, the power generation will be a surplus causing a rise in $V_{O\text{-rms}}$. If it rises beyond $V_{O\text{-rms}}$ + 10%, the MPP is no longer tracked since the hardware interrupt causes a step by step decrementing of M which in-turn leads step by step reduction of $V_{O\text{-rms}}$. The moment the measured $V_{O\text{-rms}}$ < nominal $V_{O\text{-rms}}$, the P & O algorithm is executed to track the MPP. If the load continues to be light, $V_{O\text{-rms}}$ again increases beyond $V_{O\text{-rms}}$ + 10% and the above procedure is repeated. $V_{O\text{-rms}}$ will continuously oscillate between the nominal value and nominal value + 10%. Now the module is not continuously operated at the MPP. These are shown in the experimental results in section VI. Using instantaneous $v_O(t)$ may make the algorithm prone to spurious spikes in $v_O(t)$ whereas using $V_{O\text{-rms}}$ will avoid this situation.

III. Detailed Operation Of The Single Stage SC Inverter Topology

The block diagram of the SC inverter is discussed in the previous section. Here the detailed circuit operation is examined by sub dividing a complete charge-discharge cycle of time period $2T_S$ into four sub intervals. The expected waveforms are given in Fig. 5. The capacitor C_{PV} [Fig. 2(a)] connected across the PV source ensures that a steady dc voltage V_{PV} with a negligible ripple is presented to the SC inverter.

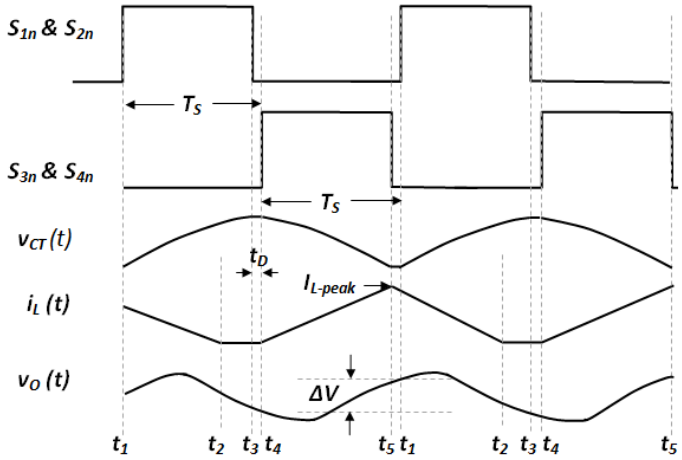

Fig. 5. Drive signals to the input switches (S_{1n} and S_{2n}) and output switches (S_{3n} *and* S_{4n}), charge transfer capacitor voltage $v_{CT}(t)$ across one C_T, inductor current $i_L(t)$ and output capacitor voltage $v_O(t)$

<u>t_1 *to* t_2 *(Fig. 6a):*</u> This is part of the interval during which the input switches S_{1n} and S_{2n} of all the SC blocks are ON and output switches S_{3n} and S_{4n} are OFF. The charge transfer capacitors C_T of all blocks are connected in parallel across the PV source and they are charged in parallel. Inductor L freewheels through diode D and supports the load R_L and charges C_O as long as $i_L(t)$ > the output current. When $i_L(t)$ < the output current, R_L is supported by both C_O and L. Finally at $t = t_2$, $i_L(t) = 0$.

<u>t_2 *to* t_3 *(Fig. 6b):*</u> The input switches S_{1n} and S_{2n} continue to be ON, charging C_T. The output switches S_{3n} and S_{4n} continue to be OFF. Now R_L is supported only by C_O since $i_L(t) = 0$.

<u>t_3 *to* t_4 *(Fig. 6c):*</u> This is the dead time when all switches S_{1n} to S_{4n} of all the SC blocks are OFF. R_L continues to be supported only by C_O.

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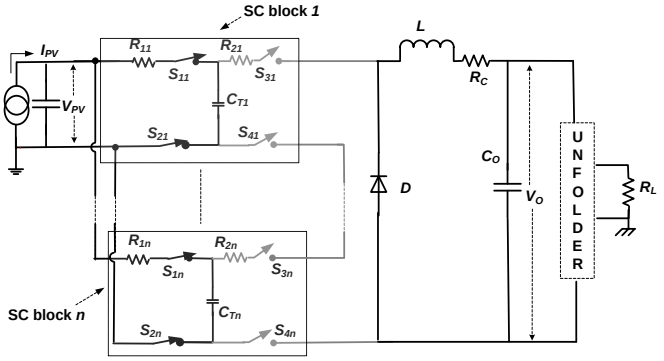
t_4 to t_5 (Fig. 6d): The input switches S_{1n} and S_{2n} of all the SC blocks are OFF and output switches S_{3n} and S_{4n} are ON. All C_Ts are connected in series and they discharge serially into the circuit comprising L and R_C in series and C_O and R_L in shunt. $i_L(t)$ ramps up. C_O starts charging when $i_L(t)$ > the output current.

t_5 to t_1 (Fig. 6e): This is the dead time. All switches S_{1n} to S_{4n} of all the SC blocks are OFF. L begins to freewheel through D.



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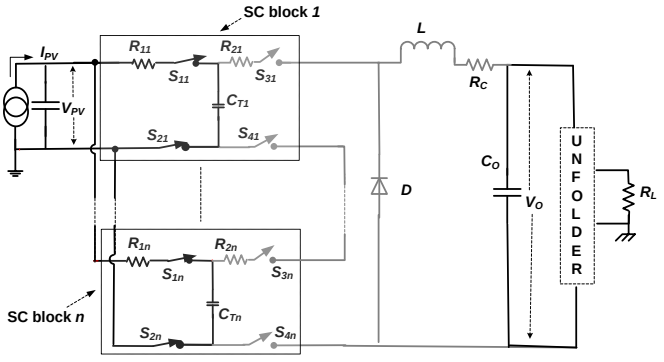

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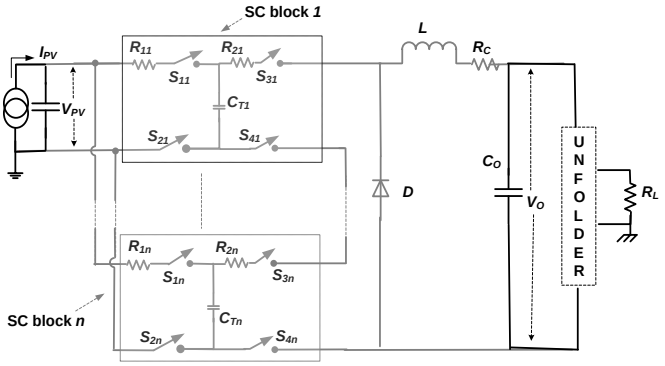

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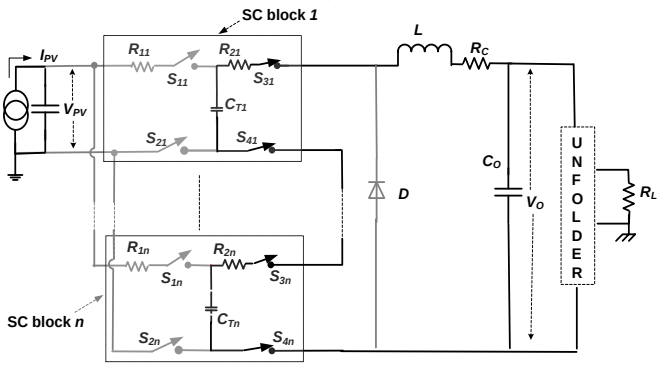
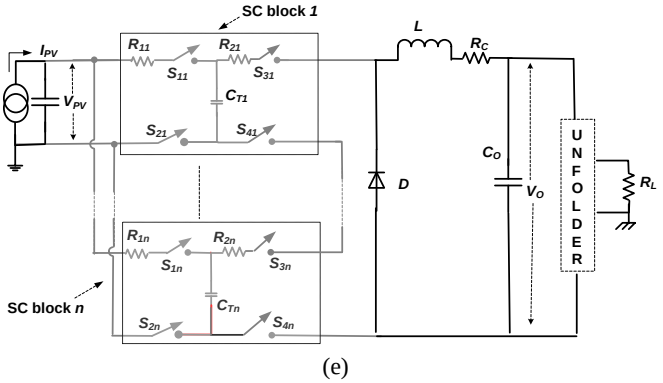


(d)



(e)

Fig. 6. Circuit configurations of the SC based inverter during different sub intervals: (a) t_1 to t_2; (b) t_2 to t_3; (c) t_3 to t_4;(d) t_4 to t_5. (e) t_5 to t_1: The part of the circuit shown in BLACK colour is active and the part in GREY is inactive.

IV. Steady State Analysis And Mathematical Model Of The Single Stage SC Inverter Topology

In this section the steady state analysis of the inverter is carried out and a mathematical model is developed. The analysis enables to understand the interdependence of various parameters and component values on the overall performance of the inverter. This is used as a quantitative tool to optimize the inverter design. The mathematical model is developed by formulating equations and solving them to determine the state variables for the four distinct sequential phases in the operation of the SC inverter. The state variables involved are charge transfer capacitor voltage $v_{CT}(t)$ during charge up phase and $v_{CT/n}(t)$ during discharge phase (due to serial discharge), inductor current $i_L(t)$ and output capacitor voltage $v_O(t)$. Each phase and the relevant equations are given below.

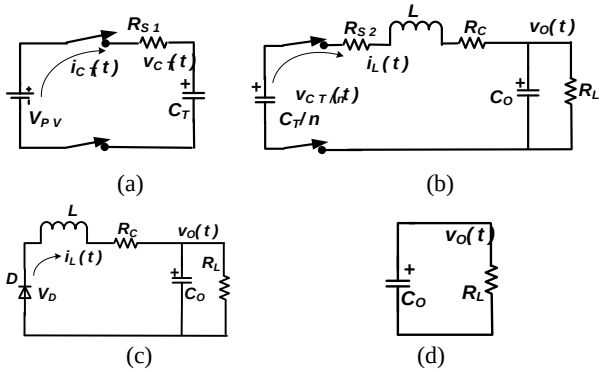


Fig. 7. Four sequential phases of the SC inverter: (a) C_T charging; (b) C_T serially discharging; (c) L freewheeling and C_O discharging; (d) C_O discharging.

Phase 1- C_T charge up (Fig. 7a): This corresponds to the time period from t_1 to t_3 in Fig. 5 during which all input switches S_{1n} and S_{2n} of all the SC blocks are ON and all the C_T s charge up in parallel from V_{PV} [Figs 6(a) and (b)]. Let $\tau_1 = R_{S1}C_T$, where R_{S1} is the sum of all the parasitic resistances (like the MOSFET $R_{DS\text{-}ON}$, capacitor ESR etc.) in the charging path. Let $v_{CT}(t_1)$ be the value of the voltage across each C_T at the start of the charge cycle. It is the initial value for phase 1. The state variable involved is $v_{CT}(t)$ and is given by:

$$v_{CT}(t) = V_{PV} + [v_{CT}(t_1) - V_{PV}]e^{-t/\tau_1} \qquad (2)$$

At the end of the charge up phase, $t = t_3$ and $v_{CT}(t) = v_{CT}(t_3)$.

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Phase 2- C_T serial discharge (Fig. 7b): This phase corresponds to the time period from t_4 to t_5 in Fig. 5 during which output switches S_{3n} and S_{4n} of all the SC blocks are ON and all the C_Ts discharge in series [Fig. 6(d)] into the load R_L. The effective charge transfer capacitance due to the serial discharge is C_T/n. R_{S2} is the sum of the parasitic resistances in the discharging path and R_C is the series resistance of L. The state variables involved are $v_{CT/n}(t)$, $i_L(t)$ and $v_O(t)$. They are given by:

$$\frac{di_L}{dt} = \frac{v_{CT/n}}{L} - \frac{i_L R_{S2}}{L} - \frac{i_L R_C}{L} - \frac{v_O}{L} \tag{3}$$

$$\frac{dv_O}{dt} = \frac{i_L}{C_O} - \frac{v_O}{R_L C_O} \tag{4}$$

$$\frac{dv_{CT/n}}{dt} = -\frac{i_L}{C_T} \tag{5}$$

Solving the above differential equations yields the expressions for the three state variables for phase 2. $i_L(t)$ is given by:

$$i_L(t) = \mathrm{Z}_1 e^{r_1 t} + e^{p_1 t}(\mathrm{Z}_2 \cos q_1 t + \mathrm{Z}_3 \sin q_1 t) \tag{6}$$

where the constants Z_1 to Z_3 and r_1, p_1 and q_1 are given by:

$$\mathrm{Z}_1 = -\mathrm{Z}_2 = \frac{v_{CT/n}(t_4) C_{T/n}\left(p_1^2 + q_1^2\right) r_1 + \frac{\left[v_O(t_4) - v_{CT/n}(t_4)\right]}{L} r_1}{\left[-(r_1 - p_1) r_1 - \left(p_1^2 + q_1^2\right) + p_1 r_1\right]} \tag{7}$$

$$\mathrm{Z}_3 = \frac{v_{CT/n}(t_4) C_{T/n}\left(p_1^2 + q_1^2\right)}{q_1} + \frac{\mathrm{Z}_1\left(p_1^2 + q_1^2\right)}{r_1 q_1} - \frac{\mathrm{Z}_1 p_1}{q_1} \tag{8}$$

r_1 is the real root and p_1 and q_1 are the imaginary roots of the cubic equation $x^3 + K_2 x^2 + K_1 x + K_0 = 0$ where:

$$K_2 = \left(\frac{1}{C_O R_L} + \frac{R_{S2}}{L} + \frac{R_C}{L}\right) \tag{9}$$

$$K_1 = \left(\frac{R_{S2}}{C_O R_L L} + \frac{R_C}{C_O R_L L} + \frac{1}{L(C_T/n)} + \frac{1}{LC_O}\right) \tag{10}$$

$$K_0 = \frac{1}{C_O R_L L (C_T/n)} \tag{11}$$

$v_O(t_4)$ is the final value of $v_O(t)$ at the end of the C_O discharge phase. Due to the discontinuous operation of L, $i_L(t_4) = 0$. $v_{CT/n}(t_4)$ is the voltage across the series connected charge transfer capacitors at $t = t_4$ which is derived from the final value of $v_{CT}(t)$ at the end of phase 1. These are the initial values for phase 2.

Equations (12) and (13) given in the Appendix are the expressions for the other state variables $v_{CT/n}(t)$ and $v_O(t)$.

Phase 3- L freewheeling and C_O discharge (Fig. 7c): This phase corresponds to the time period from t_5 to t_2 in Fig. 5. It overlaps with part of phase 1 [Fig. 6(a)]. V_D denotes the drop across the diode D. The state variables involved are $i_L(t)$ and $v_O(t)$. They are given by:

$$\frac{di_L}{dt} = -\frac{i_L R_C}{L} - \frac{v_O}{L} - \frac{V_D}{L} \tag{14}$$

$$\frac{dv_O}{dt} = \frac{i_L}{C_O} - \frac{v_O}{R_L C_O} \tag{15}$$

Solving (14) and (15) yields the expressions for $i_L(t)$ and $v_O(t)$.

$$i_L(t) = e^{p_2 t}\left(\mathrm{Z}_4 \cos q_2 t + \mathrm{Z}_5 \sin q_2 t\right) - \frac{V_D}{LC_O R_L}\frac{1}{m_1 m_2} \tag{16}$$

where the constants Z_4 and Z_5 and m_1 and m_2 are given by:

$$\mathrm{Z}_4 = i_L(t_5) + \frac{V_D}{LC_O R_L}\frac{1}{m_1 m_2} \tag{17}$$

$$\mathrm{Z}_5 = -\frac{v_O(t_5) + L\mathrm{Z}_4 p_2 + R_C \mathrm{Z}_4 + \frac{R_C V_D}{LC_O R_L}\frac{1}{m_1 m_2} + V_D}{Lq_2} \tag{18}$$

$m_1 = p_2 + iq_2$ and $m_2 = p_2 - iq_2$ where:

$$p_2 = \frac{-\left(\frac{R_C}{L} + \frac{1}{R_L C_O}\right)}{2} \tag{19}$$

$$q_2 = \frac{\sqrt{\left(\frac{2}{\sqrt{LC_O}}\right)^2 - \left(\frac{R_C}{L} - \frac{1}{R_L C_O}\right)^2}}{2} \tag{20}$$

The state variable $v_O(t)$ is given by (21) in the Appendix:

In (17) and (18), $i_L(t_5)$ and $v_O(t_5)$ are the final values of $i_L(t)$ and $v_O(t)$ at the end of phase 2 i.e. at $t = t_5$. These are the initial values for phase 3.

Phase 4- C_O discharging (Fig. 7d): This phase corresponds to the time period from t_2 to t_4 in Fig. 5 and Figs. 6(b) and (c) when $i_L(t) = 0$. Now R_L is supported only by C_O. Let $\tau_2 = R_L C_O$. $v_O(t_2)$ is the final value of $v_O(t)$ in phase 3. It is the initial value of $v_O(t)$ in phase 4.The state variable involved in this phase is $v_O(t)$ and is given by:

$$v_O(t) = v_O(t_2) e^{-t/\tau_2} \tag{22}$$

V. Applications Of The Mathematical Model

The applications of the steady state analysis and mathematical model based on equations (1) to (22) developed in the previous section are discussed in detail in this section. For a given operating condition, the model enables the determination of the state variables viz. $v_O(t)$, $i_L(t)$ and $v_{CT}(t)$ at any given time. This is used to analyze the inverter performance and optimize the component choice.

A. Validating the mathematical model

At the outset, the validity of the mathematical model of the SC inverter is established by examining the inverter output $v_O(t)$ which must be a sine waveform. The equations of the state variables that describe each phase of operation of the inverter are solved sequentially to determine the value of the state variables at the end of the respective phase. Initially, zero initial values are assumed for the state variables. Later, the final values of the state variables involved in each phase are used as the initial values in the following phase. This process is outlined in the flowchart of Fig. 8. When the loop is executed f_S / f_O times by incrementing N, a complete cycle of the steady state output $v_O(t)$ is generated by plotting $v_O(t)$ in every alternate iteration of the loop since its periodicity is $f_S / 2$.

$v_O(t)$ plotted in Fig. 9 (a) and (b) are the outputs of the flow chart of Fig. 8 for different PV module illumination conditions. M and C_O are adjusted to get the desired $v_O(t)$. All other parameters and component values are the same.

The Total Harmonic Distortion (THD) of $v_O(t)$ gives the measure of its quality. The flowchart of Fig. 8 generates a vector of $f_S / 2f_O$ points that represents one cycle of $v_O(t)$. The theoretical THD of $v_O(t)$ is determined with MATLAB. An *m-file* is used to determine the Discrete Fourier Transform of the

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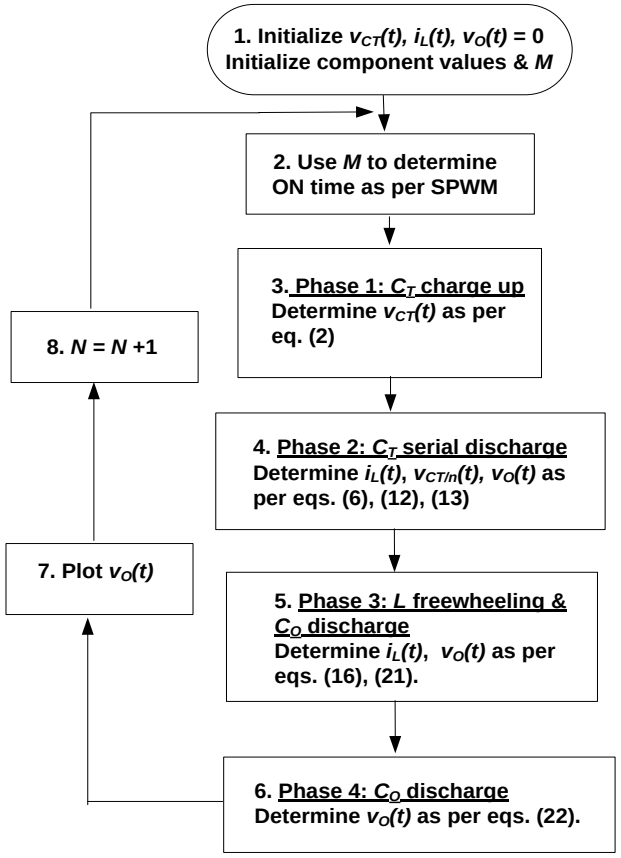
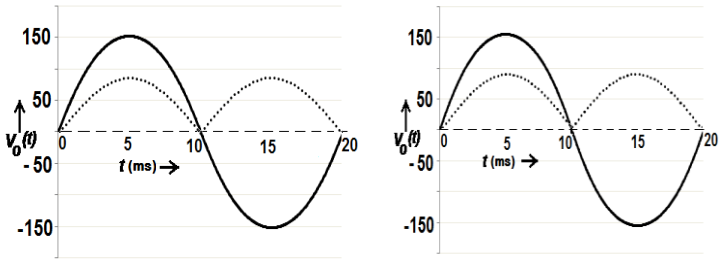


Fig. 8. Flow chart for plotting $v_O(t)$ using the mathematical analysis.



(a) (b)

Fig. 9. (a) and (b) show the output $v_O(t)$ of the flowchart of Fig. 8. The fullwave rectified sine reference is shown in dotted trace. In (a) P_O = 66W, V_{PV} = 60V. Theoretical THD = 4.03%. In (b) P_O = 33W, V_{PV} = 55V, Theoretical THD = 5.01%. In both cases $v_O(t) \approx$ 110V rms at 50Hz.

vector representing $v_O(t)$. The location of the fundamental is ascertained as it has the maximum amplitude. Then the location of the harmonics is determined. Finally the THD is computed from the square of the amplitude of the fundamental and its harmonics. The THD of $v_O(t)$ of Fig. 9(a) is 4.03% while that of Fig. 9(b) is 5.01%.

The following conclusions may be derived from these observations: *a)* SPWM generates a boosted sinusoidal output $v_O(t)$ when applied to the SC topology of Fig. 2. *b) M* and C_O may be adjusted to generate a pure sine output for different input and load conditions.

Hence the mathematical model and analysis is validated and may be used for further studies.

B. Analysis and optimization of the SC inverter

The possibility to determine any of the state variables at any desired time under a given operating condition with the flow chart of Fig. 8 forms the basis of the methods presented in this section for analysis and optimization. Due to SPWM, the state variables do not attain a fixed steady state value as in dc-dc converters. Hence a graphical method is presented to optimize the component values.

The average output power P_O is given by:

$$P_O = \frac{V_{O-rms}^{\ 2}}{R_L} = \frac{V_{O-peak}^{\ 2}}{2R_L} = \frac{\left(v_O(t)\Big|_{N=\frac{f_S}{4f_O}} \right)^2}{2R_L} \qquad (23)$$

where the value of $v_O(t)$ evaluated at $N = f_S / 4f_O$ corresponds to the peak output value $V_{O\text{-}peak}$.

Optimizing C_T: C_T used in each SC block (Fig. 6) is responsible for transferring power from the PV source to the load. It has to handle a large current ripple. Hence a low ESR ceramic or metalized polyester capacitor is used. For a cost effective design, the capacitors have to be optimized. To optimize C_T for a given operating condition, P_O is determined for different values of C_T under the given operating condition. The variation of P_O with C_T is studied as shown in Fig. 10. Initially P_O increases steadily when C_T is increased. Beyond a certain value, P_O almost stabilizes even if C_T continues to increase due to the fact that the increase in C_T is now offset by the decrease in ΔV_{CT} limiting the charge transfer $Q_{CT} = C_T.\Delta V_{CT}$ in each cycle. This shows that it is possible to choose an optimum value of C_T for a desired P_O.

Optimizing MOSFETs : MOSFET switches are usually used in SC power conditioners. MOSFET optimization implies choosing MOSFETs with lowest V_{DS} and I_{DS} ratings and highest $R_{DS\text{-}ON}$ rating to meet the required design since MOSFETs with higher V_{DS} and I_{DS} and lower $R_{DS\text{-}ON}$ are more expensive due to larger die size. MOSFET $R_{DS\text{-}ON}$ optimization in this context refers to choosing the MOSFETs with the highest $R_{DS\text{-}ON}$ that meet the initial design assumptions. If MOSFETs with lower $R_{DS\text{-}ON}$ are used in the charging circuit [Fig. 7(a)], the efficiency does not improve since charging circuit resistances do not play a part in the capacitor charging efficiency [4]. The optimum $R_{DS\text{-}ON}$ MOSFET in charging circuit will enable to extract the MPP power at maximum *M*. Using MOSFETs with lower than optimum $R_{DS\text{-}ON}$ will result in operating at the MPP even at lower than maximum *M*. However using lower $R_{DS\text{-}ON}$ MOSFETs in the discharging circuit will marginally increase the efficiency and the inverter will be able to deliver more output power than the initial design assumptions when operating at maximum value of *M*. The input MOSFETs (S_{1n} and S_{2n} of Fig. 6) are chosen so that $I_{DS} > i_{CT\ max}(t)$ where [referring to Fig. 5 and Fig. 7(a) and equation (2)]:

$$I_{DS} > i_{CT\ \max}(t) = \frac{V_{PV} - v_{CT}(t_1)\Big|_{N=\frac{f_S}{4f_O}}}{R_{S1}} \qquad (24)$$

The second term in the numerator corresponds to the value of $v_{CT}(t)$ at $t = t_1$ evaluated at $N = f_S / 4f_O$. This is the lowest value of $v_{CT}(t)$ causing the highest value of $i_{CT}(t)$. Since MPP is tracked, the operating point on the array is at V_{MPP}. The maximum voltage that the input MOSFETs (S_1 and S_2 of Fig. 6 and Fig. 13), must block depends on V_{MPP} and the number of SC blocks *n*. During the discharge phase *n* C_Ts that are

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charged to V_{MPP} are connected in series. Now, the maximum voltage that each of the output MOSFETs (S_3 and S_4 of Fig. 6 and Fig. 13), have to block is nV_{MPP}. For output MOSFETs, $I_{DS} > 4I_{O\ peak}$ since L operates in discontinuous mode. R_{S1} represents the parasitic resistances in the charging path including the sum of MOSFET ON resistances in the charging circuit and R_{S2} represents the parasitic resistances in the discharging path including the sum of MOSFET ON resistances in the discharging circuit. For a given operating condition, P_O is plotted for different values of R_{S1} and R_{S2} in Fig. 11. P_O decreases with increase in R_{S1} and R_{S2} since Q_{CT} decreases with increase of resistance in the charge path. From this figure it is possible to determine optimum values of R_{S1} and R_{S2} that meet the required operating specifications.

Optimizing C_O: C_O affects the average output ripple ΔV. Referring to Fig. 5, R_L is supported by L and C_O during the time period t_5 to t_4. When $v_O(t) = V_{O\text{-}peak}$, the duty ratio is maximum and if we neglect the dead time t_D, the time duration between t_5 and t_4 is T_S. In step 2 (Design of L) of the design procedure given below, it is given that L operates in discontinuous mode such that $i_L(t) = 0$ in $\frac{2}{3}T_S$. Now R_L is supported fully by C_O for about $0.5T_S$. Thus C_O is given by:

$$C_O = \frac{-0.5T_S}{R_L \times \ln\left(\frac{V_{O-peak} - \Delta V}{V_{O-peak}}\right)} \quad (25)$$

Cross over distortion $V_{cross\text{-}over}$ refers to $v_O(t)$ evaluated at $N = 1$. It is given by:

$$V_{cross-over} = v_O(t)\big|_{N=1} \quad (26)$$

Ideally $V_{cross\text{-}over} = 0$. Non zero $V_{cross\text{-}over}$ deteriorates the THD. A higher C_O results in a lower ΔV but larger $V_{cross\text{-}over}$ and vice versa. From (22) it is seen that R_L has a strong influence on $v_O(t)$. Hence it is essential to change C_O dynamically depending on R_L to keep $V_{cross\text{-}over}$ to a minimum and hence the THD within desired limits.

VI. Experimental Results

This section presents: *(a)* A stepwise design procedure for the choice of optimum components for the SC inverter based on the graphical analysis and optimization methods discussed in the previous section; *(b)* Experimental waveforms of the hardware prototype and correlation with the theoretical aspects.

A. Stepwise design procedure for the SC inverter

Input and output specifications: The aim is to design a single stage SC inverter of Fig. 6 that operates on a PV module with $35W \le P_{MPP} \le 70W$ and $55V \le V_{MPP} \le 60V$ with variation of the intensity of solar illumination. The desired ac output under nominal operating conditions is 50Hz sine with $V_{0\text{-}rms}$ = 110V±10% and THD ≤ 5%.

Step 1 - Selecting C_{PV}: A constant voltage must be presented to the input of the SC inverter. A capacitor C_{PV} (Fig. 2) is connected across the PV module's output for this purpose where [31]:

$$C_{PV} = \frac{P_{PV}}{4\pi f_O V_{PV} \Delta V_{PV}} \quad (27)$$

Here P_{PV} is the maximum power that the PV array can deliver and ΔV_{PV} is the maximum allowed ripple on the PV voltage V_{PV}. Allowing $\Delta V_{PV} \approx 2\%$ of V_{PV}, $C_{PV} \approx 1800\mu F$ is chosen.

Step 2 - Design of L: Let f_S = 35kHz. L is designed to always operate in discontinuous conduction mode to minimize its size. Let $I_{L\text{-}peak}$ be the peak value of $i_L(t)$. It is assumed that $I_{L\text{-}peak} = 4I_{O\text{-}peak}$. Take efficiency $\eta \approx 95\%$. When P_{MPP} = 70W, $I_{O\text{-}peak}$ = 0.87A. Referring to Fig. 5, $i_L(t)$ begins to ramp down from $I_{L\text{-}peak}$ to zero after the output MOSFETs turn OFF at t_5. Assume that this ramp down of $i_L(t)$ is accomplished in $0.65T_S$ (i.e. $\frac{2}{3}T_S$). Now $L = (V_{O\text{-}peak} \cdot dt / di) \approx 850\mu H$ where $dt = 0.65T_S$ and $di = 4I_{O\text{-}peak}$. A toroidal core is used to realize the inductor. Coil resistance $R_C \approx 0.2\Omega$.

Step 3 - Determine n (the number of SC blocks): n SC blocks (Fig. 2b) are connected as in Fig. 6 to boost the input voltage. Minimum value of n has to be determined so that the desired $V_{O\text{-}rms}$ = 110V may be achieved for the peak output load of 66W corresponding to $R_L = 180\Omega$. If $\Delta V \approx 7\%$ of $V_{O\text{-}peak}$ is allowed, then using (25), C_O is approximately 0.75µF. Make an initial assumption of $C_T = 100\mu F$ and $R_{S1} = R_{S2} = 0.1\Omega$. From step 2, $L = 850\mu H$ and $R_C = 0.2\Omega$. The algorithm of Fig. 8 is executed to determine $V_{O\text{-}rms}$ for different values of n with the maximum value of M i.e. $M = 0.95$ and V_{PV} = 60V. For n = 1, $V_{O\text{-}rms}$ = 27.58V. For n = 2, $V_{O\text{-}rms}$ = 56V and for n = 3, $V_{O\text{-}rms}$ = 84V. When n = 4, $V_{O\text{-}rms}$ = 111.7V. This is above our requirement of $V_{O\text{-}rms}$ = 110V. Thus we choose n = 4 to meet the required specifications.

Step 4 – Selecting optimum C_T : In Fig. 10, P_O is plotted for different values of C_T. The operating conditions assumed are V_{PV} = 60V, $R_{S1} = R_{S2} = 0.1\Omega$, C_O = 0.75µF and M = 0.95. From step 2, L = 850µH and R_C = 0.2 Ω. From step 3, n = 4. Required $V_{0\text{-}rms} \approx 110V$ and $P_O \approx 66W$. C_T is varied from 1µF to 100µF. From Fig. 10, C_T = 33 µF is the optimum choice. With this value we can meet the requirement of $P_O \approx 66W$ at $V_{0\text{-}rms}$ = 110V. A metallized polyester capacitor (Euro Farad PM90R1S) is used due to its very low ESR (≈ 4mΩ) and high ripple current rating.

Step 5 – Selecting optimum MOSFETs: R_{S2} = (Σ $R_{DS\text{-}ON}$ of output side MOSFETs + parasitic resistances in discharge path). R_{S1} = (Σ $R_{DS\text{-}ON}$ of input side MOSFETs + parasitic resistances in the charging path). The MOSFET $R_{DS\text{-}ON}$ is the major factor influencing R_{S1} and R_{S2}. As in step 4, a graphical method is adopted to select optimum MOSFET $R_{DS\text{-}ON}$.

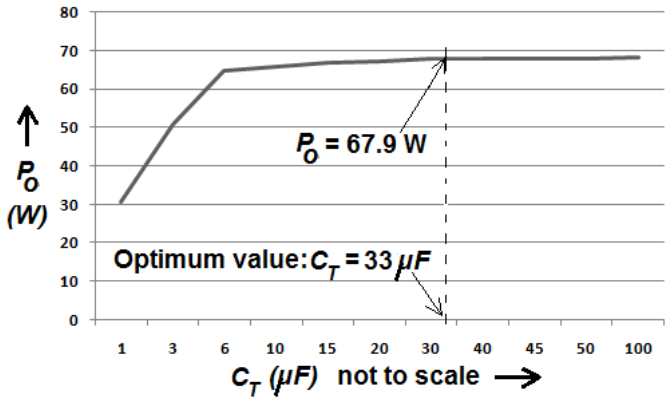

Fig. 10. Optimization of C_T for a desired input and output specification.

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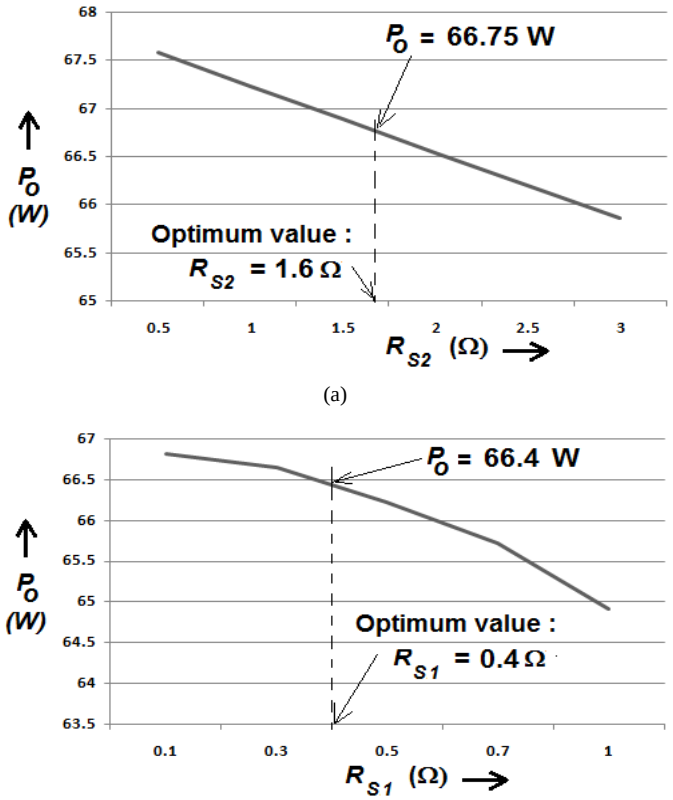

Fig. 11. Optimization of (a) R_{S2} and (b) R_{S1} for a desired input and output specification.

Firstly it is assumed that $R_{S1} = 0.1\Omega$. P_O is plotted in Fig. 11(a) for the same operating conditions and output specifications as in step 4 except that now $C_T = 33\mu F$. R_{S2} is varied such that $0.5\ \Omega \le R_{S2} \le 3\ \Omega$. Fig. 11(a) shows that even when R_{S2} varies from 0.2Ω to 3Ω, P_O changes by only about 2W. For $P_O \approx$ 66W, R_{S2} may be fixed at 1.6Ω. IRFM360 is chosen as the output MOSFET. It has an $R_{DS\text{-}ON} = 0.2\Omega$.

During the discharge phase, the eight output MOSFETs S_{31}, S_{41} etc. (Fig. 6) are in series. Hence total $R_{DS\text{-}ON} = 1.6\Omega$. Required $V_{DS} = nV_{MPP} = 4\times60V = 240V$ where n is the number of SC blocks. V_{DS} of IRFM360 that is selected is 400V. Also $I_{DS} = 23A$ which is well above the required value of $4I_{O\text{-}peak} =$ 3.5A. Capacitor ESR is negligible.

Next, R_{S2} is fixed at 1.6Ω and R_{S1} is varied such that $0.1\ \Omega \le R_{S1} \le 1\Omega$. P_O is plotted against R_{S1} in Fig. 11(b). For $P_O \approx$ 66W, R_{S1} may be fixed at 0.4Ω. IRF6215 ($R_{DS\text{-}ON} = 0.3\Omega$) is chosen as the high side input MOSFET (S_{1n}). The simple drive circuit for a p-channel device in this location is the reason for choosing it. IRFB52N15D ($R_{DS\text{-}ON} = 0.03\Omega$) is chosen as the low side input MOSFET (S_{2n}). In this implementation, $n = 4$. An analysis of Fig. 13 shows that a maximum reverse voltage of $2V_{MPP} = 2\times60V$ develops across some of the input MOSFETs when the C_Ts are connected in series during the discharge. Hence MOSFETs with $V_{DS} > 2V_{MPP}$ are chosen as the input MOSFETs (S_1, S_2 etc). The input MOSFETs that are selected have a $V_{DS} = 150V$. Using (24), $i_{CT\ max}(t) = 3.12A$ which is well below the I_{DS} of the MOSFETs considered.

Step 6 – Choosing C_O : Let $\Delta V = 10V$ (≈ 7% of $V_{O\text{-}peak}$). Similar ripple is observed in [12, 31]. At maximum load $R_L = 180\Omega$ ($P_0 = 67W$). Using (25), $C_O = 0.75\mu F$. Since C_O affects $V_{cross\text{-}over}$ and hence THD also, it is mandatory that C_O be changed dynamically depending on R_L. The PV module's P_{MPP} varies such that $35W \le P_{MPP} \le 70W$. Assuming $\eta \approx 95\%$, $360\ \Omega \le R_L \le 180\Omega$. This range is sub divided into four smaller ranges. Table I gives the values of C_O for these ranges of R_L that are chosen to keep the THD ≈ 5%.

The output capacitor C_O is determined by a network similar to that in [34] such that $C_O = C_{O1} + C_{O2} + C_{O3} + C_{O4}$ where $C_{O1} = 0.37\mu F$ and $C_{O2} = C_{O3} = C_{O4} = 0.13\ \mu F$. As shown in Fig. 12, C_{O1} is permanently hardwired to the circuit whereas the other three capacitors are included or excluded with low $R_{DS\ ON}$ MOSFETs to adjust the overall value of C_O. Ceramic capacitors are used due to their low ESR (typically a few milliohms). An analog divider (AD 535) determines R_L by dividing V_{Orms} by I_{Orms}. R_L, which is represented by a voltage, is compared by three different comparators to the different reference levels set for each of them. Reference V_{R1} is a voltage that corresponds to 315Ω, V_{R2} corresponds to 270Ω and V_{R3} corresponds to 225Ω. When $180\Omega \le R_L < 225\Omega$, S_{C2} to S_{C4} are ON and $C_O = 0.75\mu F$. When $225\Omega \le R_L < 270\Omega$, S_{C4} is OFF and S_{C2} and S_{C3} are ON. Now $C_O = 0.62\ \mu F$. When $270\Omega \le R_L < 315\Omega$, S_{C4} and S_{C3} are OFF and $C_O = 0.5\ \mu F$. When $315\Omega \le R_L < 360\Omega$, S_{C4} , S_{C3} and S_{C2} are OFF and $C_O = 0.37\mu F$.

Table I summarizes the specifications and components finalized as per the steps formulated above. Fig. 13 shows the actual implementation of the SC blocks and the unfolding circuit with MOSFETs. In block 1, S_{11} and S_{21} are reversed when compared to the other blocks.

B. Experimental waveforms of the hardware model

The experimental setup consists of a tunable solar array simulator to simulate the PV module operating under different conditions of solar illumination. The number of SC blocks n will have to be increased if the voltage from an actual PV

TABLE I. Summary of operating specifications and components selection

Input specifications: $35W \le P_{MPP} \le 70W$, $55V \le V_{MPP} \le 60V$ Output specifications: 50Hz sine, $V_{0\text{-}rms} = 110V\pm10\%$, THD ≤ 5%.								
C_{PV}	n	Input MOSFETs	Output MOSFETs	C_T	L	R_C	C_O	Worst case theoretical THD
1800μF	4	$R_{S1} = 0.4\ \Omega$ IRF6215 IRFB52N15D	$R_{S2} = 1.6\ \Omega$ IRFM360	33μF	850 μH	0.2Ω	0.75μF for Range 1* 0.62 μF for Range 2* 0.5μF for Range 3* 0.37μF for Range 4*	4.7% 5.01% 5.07% 5.15%

* *Range1:* $180\Omega \le R_L < 225\Omega$, *Range2*: $225\Omega \le R_L < 270\Omega$, *Range3*: $270\Omega \le R_L < 315\Omega$, *Range4*: $315\Omega \le R_L < 360\Omega$

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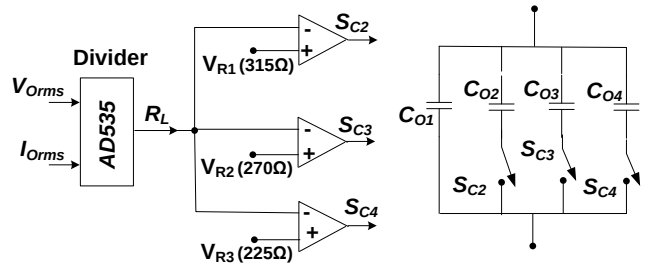


Fig. 12. Determination of C_O depending on R_L

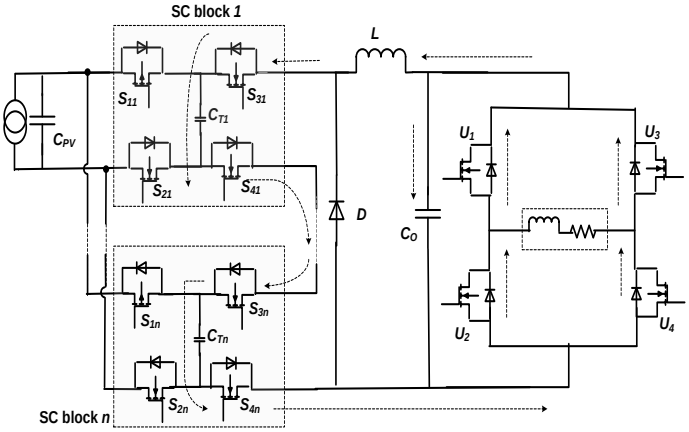


Fig. 13. Actual implantation of the SC blocks and unfolding circuit with MOSFETs. The dotted arrows show the flow of reactive current.

module is lower than that of the simulator used here. A supervisory PC executes the algorithm of Fig. 4 implemented in C language. I_{PV} and V_{PV} are monitored and used by the P & O algorithm. $v_O(t)$ and $i_O(t)$ are also monitored to compute the value of the existing load for dynamically selecting C_O as per Table I and for limiting the upper value of $v_O(t)$ to within 10% of $V_{O\text{-}rms}$. Hall effect sensors are used to sense I_{PV} and $i_O(t)$. The hardware interrupt of the PC is used to execute block 4 of the algorithm to regulate $v_O(t)$. The PC generates a signal directly proportional to V_M [equation (1)] that controls the amplitude of the full wave rectified sine reference generated by a signal generator with an IEEE interface. This reference is compared with a triangular carrier at 35kHz to generate the drive pulses. A gating circuit channelizes alternate drive signals to the input side MOSFETs and the output side MOSFETs. By detecting the zero crossings of the sine reference, the switches of the unfolding circuit are operated to unfold the alternate halves of the sine output.

Fig. 14 shows waveforms of the drive to the input and output MOSFETs and the state variables $v_{CT}(t)$, $i_L(t)$ and $v_O(t)$ acquired from the hardware model at peak duty ratio. As desired, L operates in discontinuous current mode. $i_L(t) \rightarrow 0$ in about 20μs, which is approximately $0.65T_S$ as per step 2 of the design procedure. For C_O = 0.75μF, ΔV given by (25) evaluates to 10V. From Fig. 14, the measured $\Delta V \approx$ 10V.

In Fig. 15, the 100Hz full wave rectified sine reference is superimposed on the 35kHz triangular carrier and plotted along with $v_O(t)$. A distortion analyzer (TEK AA501) is used to measure the THD of $v_O(t)$. The solar array simulator is operated to simulate different illumination conditions. R_L is manually adjusted to represent loads corresponding to range 1, 3 and 4 of Table I. The control circuit chooses the appropriate M and C_O in each case.

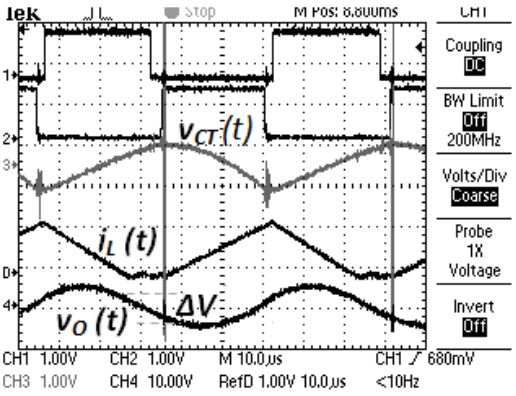
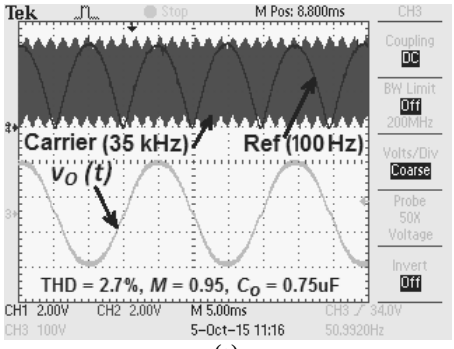
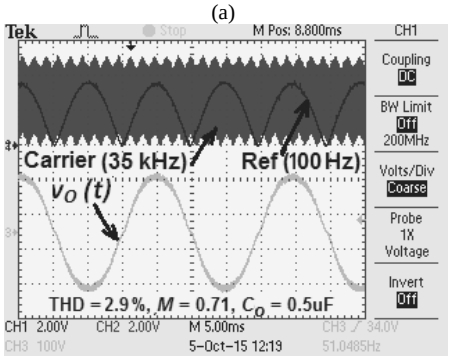


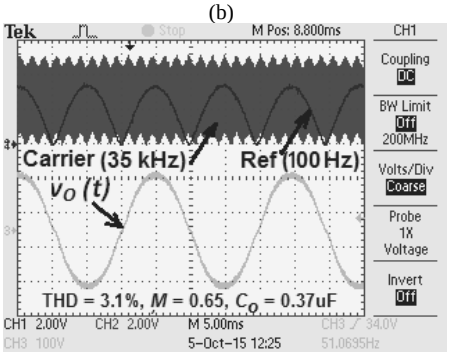
Fig. 14. Experimental waveforms: Gate drive to the input and output MOSFETs (channel 1 and 2), charge transfer capacitor voltage across one C_T $v_{CT}(t)$, inductor current $i_L(t)$ (3A / div) and output capacitor voltage $v_O(t)$ observed in 10μs / div time scale. Only the ac components of $v_{CT}(t)$ and $v_O(t)$ are shown.



(a)



(b)



(c)

Fig. 15. Experimental waveforms: 100Hz full wave rectified sine reference superimposed on 35 kHz triangular carrier and inverter output $v_O(t)$ observed in 5ms / div time scale for different solar illumination conditions (a) V_{PV} = 60V, I_{PV} = 1.14A, P_O = 65.4W (b) V_{PV} = 58V, I_{PV} = 0.82A, P_O = 44.8W (c) V_{PV} = 55V, I_{PV} = 0.66A, P_O = 33.6W. In all three cases $V_{O\text{-}rms}$ = 110V±10%.

The voltage and current ripple (ΔV_{PV} and ΔI_{PV}) on the PV source at full illumination due to the switching in the SC inverter are shown in Fig. 16. As per (27) ΔV_{PV} is limited to <

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2% of V_{PV} due to C_{PV} = 1800µF. The deviation from P_{MPP} due to ΔV_{PV} and ΔI_{PV} is < 1%. The peak MOSFET current is about 3A as predicted by (24).

$v_O(t)$ with inductive load is shown in Fig. 17. The path of the reactive current is shown in Fig. 13. The body diodes of the MOSFETs allow the reactive current to find a path through the series connected C_Ts and C_O. As the power factor decreases, the distortion in $v_O(t)$ increases as shown in Fig. 17(a) and Fig. 17(b).

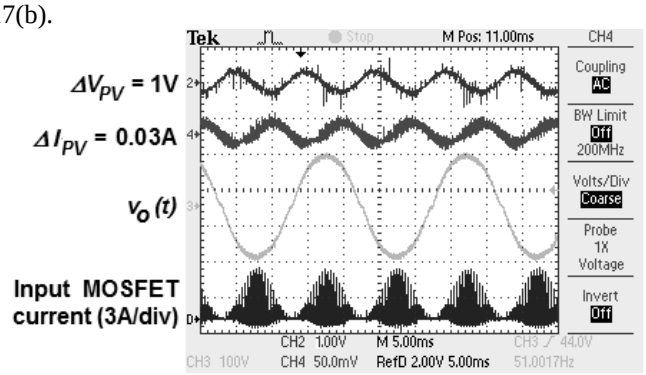

Fig. 16. Experimental waveforms: Voltage ripple (ΔV_{PV}) and current ripple on PV module (ΔI_{PV}) for full illumination. $v_O(t)$ and current through input MOSFET of one block of the SC inverter are also shown.

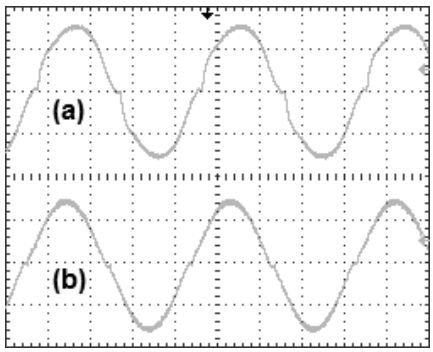

Fig. 17. Experimental waveforms: $v_O(t)$ with an inductive load. (a) R = 146Ω, L = 434mH, cos ϕ = 0.73 (b) R = 192Ω, L = 177mH, cos ϕ = 0.96

The transient and steady state performance of the MPP tracking inverter under different conditions is shown in Fig. 18. In Fig. 18(a), turn ON behavior of the inverter at full load with the PV module illuminated at full intensity is examined. Now the P & O algorithm (block 3 of Fig. 4) is executed. V_M is incremented / decremented by 0.5% once in 60ms to track the MPP. Hence it takes about 12s to increment V_M from minimum to maximum value and consequently $M = V_M / V_T$ from 0 to 0.95. At full intensity of illumination and inverter at full load, V_M has to be set very close to the maximum value to track the MPP.

In Fig. 18(b), the inverter is initially operating at full load with a fully illuminated PV module. Now $V_{O\text{-}rms} \approx$ 110V and $P_{MPP} \approx$ 69W. The illumination intensity is suddenly reduced at point A such that the *I-V* curve is altered and the new $P_{MPP} \approx$ 37W. Initially $V_{O\text{-}rms}$ falls since the value of V_M at point A causes off optimal operation on the new *I-V* curve. When the P & O algorithm readjusts V_M for operation at the new P_{MPP}, more power is delivered to the load and $V_{O\text{-}rms}$ increases. However the new value of $V_{O\text{-}rms} \approx$ 75V as compared to the nominal value of 110V. The measured MPP tracking efficiency (ratio of input power of the SC inverter to the actual MPP power of the PV module) in the above cases is > 97%.

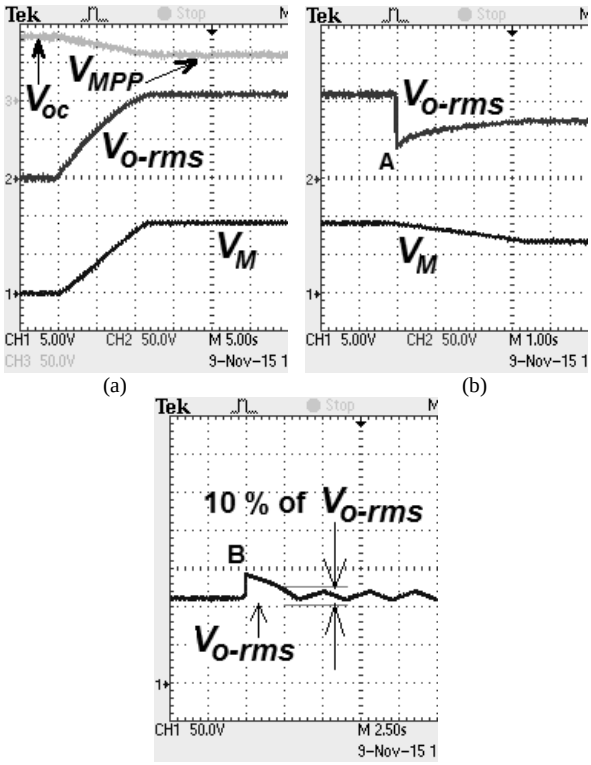

Fig. 18. Experimental waveforms: Transient and steady state behavior of the MPP tracking SC inverter. (a) Turn ON behavior: PV source illuminated with full intensity with inverter on full load. (b) Transient behavior: Full intensity illumination and full load to low intensity illumination and full load. (c) Standalone operating capability: Full intensity illumination and low load - $V_{O\text{-}rms}$ maintained within +10% of nominal value.

The test condition of Fig. 18(c) shows the standalone operating capability of the proposed SC inverter when illumination intensity is high but load is low. At point B, R_L is suddenly reduced from about 180Ω (full load) to about 360Ω (minimum load). This causes $V_{O\text{-}rms}$ to initially shoot up to 135V due to surplus power from the PV module. Now the hardware interrupt causes block 5 of the algorithm of Fig. 4 to be executed. Consequently V_T is decremented by 0.5% once every 60ms by block 5 of the algorithm and $V_{O\text{-}rms}$ gradually decreases to the nominal value of 110V.

Once $V_{O\text{-}rms}$ = 110V, the P & O algorithm (block 3 of Fig. 4)) is executed resulting in gradual increase of $V_{O\text{-}rms}$ as the MPP is approached. When $V_{O\text{-}rms}$ > nominal $V_{O\text{-}rms}$ + 10%, the hardware interrupt leads to execution of block 5. Thus $V_{O\text{-}rms}$ oscillates in a band between $V_{O\text{-}rms}$ and $V_{O\text{-}rms}$ + 10% as shown in Fig. 18(c). But for this scheme, $V_{O\text{-}rms}$ will remain well above the nominal value for low loads preventing standalone operation. Figs. 18(a) and (b) pertain to operation in mode 1 of section II B while Fig. 18(c) is an example of operation in mode 2.

The inversion efficiency of the proposed single stage SC based scheme is plotted for different output powers in Fig. 19(a). Peak inversion efficiency > 95% is achieved. An efficiency comparison with standalone ($35W \le P_O \le 70W$) and grid connected ($50W \le P_O \le 200W$) conventional inverters is shown. There is a 7% average improvement in inversion

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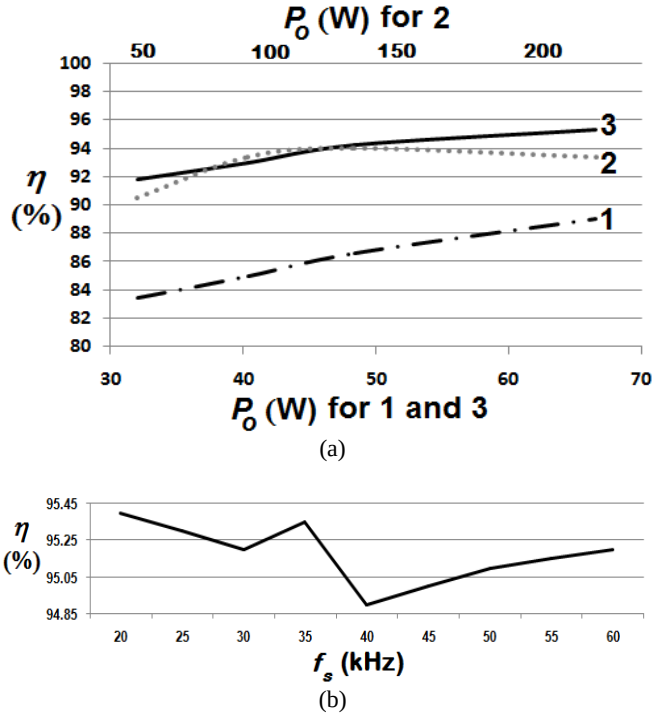

Fig. 19. Inverter Efficiency: (a) Comparison of inversion efficiency with variation in P_O of the proposed SC inverter and conventional inverters. (1) is a conventional standalone inverter with $35W \leq P_O \leq 70W$ (2) is a conventional grid connected inverter [35] with $50W \leq P_O \leq 200W$ (3) is the proposed standalone SC inverter (b) Variation of efficiency of the proposed SC inverter with f_S at $P_O \approx 66W$.

efficiency and about 150g weight advantage with the SC inverter compared to the standalone conventional inverter with similar P_O. The efficiency of a recent PV source fed grid tied conventional flyback inverter [35] that operates in the power range of 50W to 200W is also given in Fig. 19(a). This inverter has two power transformers and an output inductor. Fig. 19(b) shows efficiency variation of the proposed inverter with f_S. P_O decreases as f_S is increased due to decrease in $Q_{CT} = C_T.\Delta V_{CT}$ in each cycle. Hence when f_S is increased, additional SC blocks are needed to deliver the desired P_O. However the size of C_T and L decreases with increase in f_S. The increase in switching losses and the need for more SC blocks causes a gradual decrease in efficiency with increase in f_S.

VII. Conclusion And Future Scope

This paper has discussed a Switched Capacitor (SC) based dc-ac inverter with the following features: *(a)* The inverter is fed from a PV module; *(b)* It is a single stage topology for PV module's MPP tracking, output voltage boosting and inversion resulting in high efficiency; *(c)* It has the capability for standalone operation since upper limit of output voltage is regulated irrespective of load and intensity of illumination of the PV module and *(d)* It has scope for integration with the PV module due to the inherent features of the SC inverter like compactness, ruggedness and light weight.

A control scheme that utilizes SPWM control and load dependent output capacitor selection is used to generate a 50Hz, 110V pure sine output with a THD < 4% from a 60V / 70W PV source. Inversion efficiency > 95% and tracking efficiency > 97% is achieved with the hardware model. A mathematical model of the inverter is derived. This is used to formulate a step by step method to optimally choose the inverter components. Table II that gives a comparative study of existing SC inverters and converters highlights the uniqueness of the present proposal.

One of the drawbacks of all SC power conditioners is the large number of MOSFET switches needed compared to conventional power conditioners. This drawback may be circumvented if the switches and associated drive circuits are integrated into a single integrated circuit. This will bring out

TABLE II. SC based dc-ac inverters and PV source fed implementations

Reference no.	Powered from	Function	Remarks
11 to 14 and 16 to 20	Voltage source	dc to ac	Boost type
15	Voltage source	dc to ac	Buck type
23, 24	PV source	MPPT + dc to dc	Unregulated output
25	PV source	distributed MPPT by dc-dc conversion	voltage equalization method (buck type dc-dc)
26	Voltage source	distributed MPPT by dc-dc conversion	current equalization method (buck type dc-dc)
27	PV source	distributed MPPT by dc-dc conversion	buck type dc-dc
28	PV source	MPPT + dc to ac	Double stage, boost type, grid connected implementation
29	PV source	MPPT + dc to ac	Single stage, buck type, grid connected implementation
30	PV source	MPPT + dc to ac	Double stage, boost type, grid connected implementation
Proposed configuration	**PV source**	**MPPT + dc to ac**	**Single stage, boost type, standalone implementation**

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the other relative advantages of SC power conditioners like compactness, ease of manufacturing and ruggedness. Simple heat steering methods described in [4] may be used to minimize the thermal dissipation in this integrated circuit.

The light weight, low height profile and almost constant efficiency over the entire operating range will make this inverter suitable for easy integration with portable un-furlable solar arrays and solar panels mounted on automobiles to enable use of standard 110V ac appliances while in transit or in remote locations. The proposed SC inverter based MPP tracker may be modified for PV module integrated grid connected and per panel MPP tracking applications [23].

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APPENDIX : MATHEMATICAL MODEL OF THE SINGLE STAGE SC INVERTER TOPOLOGY

Phase 2 (section - IV):

$$v_{CT/n}(t) = -\frac{1}{C_T/n}\left[\left(\frac{Z_1 e^{r_1 t}}{r_1}\right)+\left(\frac{Z_2 p_1}{p_1^2+q_1^2}e^{p_1 t}\cos q_1 t+\frac{Z_2 q_1}{p_1^2+q_1^2}e^{p_1 t}\sin q_1 t\right)+\left(\frac{Z_3 p_1}{p_1^2+q_1^2}e^{p_1 t}\sin q_1 t-\frac{Z_3 q_1}{p_1^2+q_1^2}e^{p_1 t}\cos q_1 t\right)\right] \quad (12)$$

$$v_O(t) = -\frac{1}{C_T/n}\left\{\left(\frac{Z_1 e^{r_1 t}}{r_1}\right)+\left(\frac{Z_2 p_1}{p_1^2+q_1^2}e^{p_1 t}\cos q_1 t+\frac{Z_2 q_1}{p_1^2+q_1^2}e^{p_1 t}\sin q_1 t\right)+\left(\frac{Z_3 p_1}{p_1^2+q_1^2}e^{p_1 t}\sin q_1 t-\frac{Z_3 q_1}{p_1^2+q_1^2}e^{p_1 t}\cos q_1 t\right)\right\}$$

$$-(R_{S2}+R_C)Z_1 e^{r_1 t}-Z_2(R_{S2}+R_C)e^{p_1 t}\cos q_1 t-Z_3(R_{S2}+R_C)e^{p_1 t}\sin q_1 t-L\begin{bmatrix} Z_1 r_1 e^{r_1 t}+Z_2(p_1 e^{p_1 t}\cos q_1 t-q_1 e^{p_1 t}\sin q_1 t)+ \\ Z_3(p_1 e^{p_1 t}\sin q_1 t+q_1 e^{p_1 t}\cos q_1 t)\end{bmatrix} \quad (13)$$

Phase 3(Section - IV):

$$v_O(t) = -LZ_4 p_2 e^{p_2 t}\cos q_2 t+LZ_5 q_2 e^{p_2 t}\sin q_2 t-LZ_5 p_2 e^{p_2 t}\sin q_2 t-LZ_5 q_2 e^{p_2 t}\cos q_2 t-R_C Z_4 e^{p_2 t}\cos q_2 t-R_C Z_5 e^{p_2 t}\sin q_2 t-\frac{R_C V_D}{LC_O R_L}\frac{1}{m_1 m_2}-V_D \quad (21)$$

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