

Counter Based Low Power, Low Latency Wallace Tree Multiplier Using GDI Technique for On-chip Digital Filter Applications

Biswarup Mukherjee

*Dept. of Electronics and Communication Engineering
Neotia Institute of Technology, Management And Science
Diamond Harbour Road, India
biswarup80@gmail.com*

Aniruddha Ghosal

*Institute of Radio Physics and Electronics
University of Calcutta
Kolkata, India
aghosal2008@gmail.com*

Abstract— This paper represents a new design of a low power, low latency Wallace tree multiplier. Wallace Tree algorithm is one of the most commonly used operations in modern days DSP applications as it can provide a fast and area efficient strategy for higher operand multiplication. For higher bits of multiplications the addition operation of partial products includes greater delay and complexity. In this present communication a number of techniques are applied in the partial products addition circuitry to optimize the area delay and speed of the Wallace multiplier. Proposed Design is synthesized for 4x4 bit multiplication using standard CAD tool design compiler in 250nm process technology. Simulation results show that the proposed multiplier design has the best power and delay results as compared to other available multipliers.

Keywords—counter, full adder, GDI technique, partial products, Wallace tree multiplier

I. INTRODUCTION

In modern days with the exclusive extension in mobile computing and portable multimedia applications low power, compact and high speed digital signal processing (DSP) systems has been increasing demand for niche devices[1]. A major task for DSP system is being handled by multipliers. Not only in DSP chips but also in many public-key cryptosystems such as Elliptic Curve Cryptography (ECC) and RSA, high operand multiplications are widely used. Therefore multiplication of higher operands has been one of the topics of interest for researchers, all the time. Multiplication is just a process which deals with lot of additions. A binary multiplication of NxN bit can be represented pictorially as follows,-

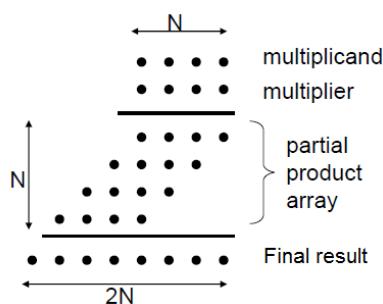


Fig. 1. Simple $N \times N$ bit multiplication

In an $N \times N$ bit binary multiplication, each bit in the multiplier is multiplied with N bit multiplicand. The results are called partial products. If the multiplier bit is a 1, then the corresponding product is simply an appropriately shifted copy of the multiplicand. If the multiplier bit is a zero, then

the product rows are also containing N nos. of zero[2]. In such way when all Partial products are generated then the corresponding columns are accumulated from top to bottom on an N -bit adder. For an N bit adder the delay of producing the output become significant as the no of transition increases [3]. Therefore in order to make a low latency multiplier circuit for higher bit of operands the accumulation of partial products must be done with modified techniques. One of such faster accumulation is performed in Booth multiplication techniques by reducing the no. of partial products with a recoding technique [4]. But such operation includes additional encoder circuitry and increases area burden. In order to make it area efficient serial multipliers or array multipliers can be used. Unfortunately, such designs suffer with poor latency. A solution to such problem can be minimized by Wallace tree algorithm. In 2010 Ron S. Waters & Earl E. Swartzlander introduced a novel architecture of modified Wallace tree architecture [5]. A high speed counter based Wallace architecture was introduced by Shahzad Asif, Yinan Kong in 2015 [6]. Many types of counters design are also communicated recently [7][8].

The main objective of the design is to achieve a novel ASIC design of Wallace tree multiplier circuit which would be efficient in power, area and delay with respect to other state of art designs. The next sections are categorized as follows. The detailed design of the proposed multiplier has been discussed in the following section. CAD tool based simulation and comparison with existing designs in terms of power, delay and area (transistor count) has been discussed later. Finally we conclude with the merits and demerits of proposed design.

II. PROPOSED WALLACE TREE MULTIPLIER DESIGN

From the above literature survey, it has been found that there are many types of multiplier architectures available for digital designs. Among all, Wallace tree can show low latency and high speed response. Such multiplication is done by the following three steps:

- For a $N \times N$ bit multiplication N^2 partial products are generated and each partial product carries a weight which depends on the bit position.
- In the next stage, the numbers of partial products are reduced by using counters/ compressors, full adders and half adders. This is done by combining the vertical partial products of same weight. The resulting sum carries the same weight but the

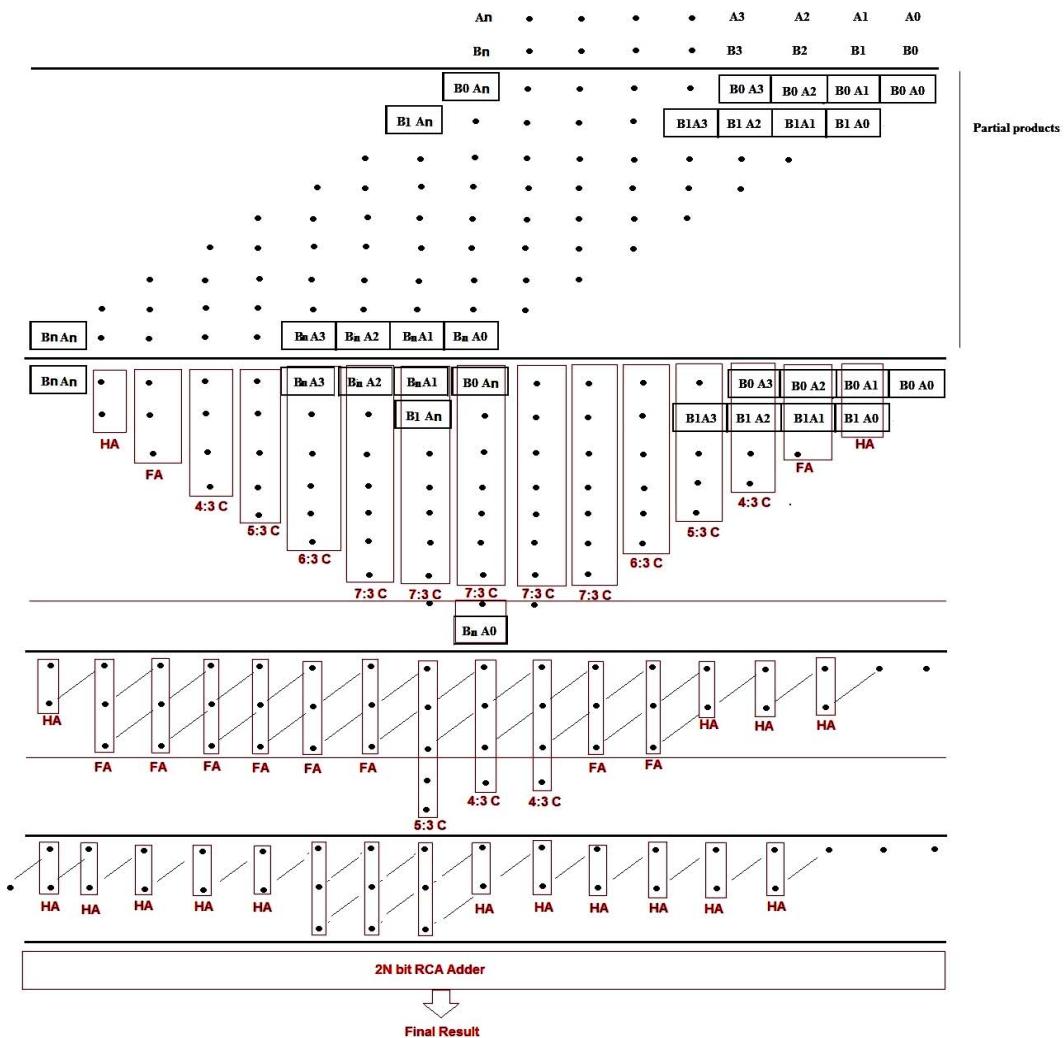


Fig. 2. Generalized architecture of modified structure of $N \times N$ Wallace tree Multiplier

generated carry out has higher weight. This process continues upto that level when there are only two layers of partial products.

- The final two layers are added using RCA adder to get the result.

The proposed multiplier uses the Wallace tree structure with modified architecture. For reducing the area, power and delay the GDI technique has been introduced in the building blocks. Fig. 2 shows general architecture for $N \times N$ bit Wallace tree architecture. The architecture consists of three major parts. Namely,- 1) Partial product generator, 2) Counter based partial product accumulation and 3) RCA adder for final result generation.

A. Partial Product Generator

First, the multiplicand each bit is multiplied with multiplier bits . The result is a partial products array. Simple AND operation can perform this job. For $N \times N$ bit multiplication operation N^2 nos. of AND gates are required. It may increase the area overhead. In order to make this stage area and power efficient a GDI based AND gates are introduced. Gate Diffusion Input (GDI) is a low power technique by which various Boolean functions can be performed by only 2 nos. of MOS transistors [9]. Figure 3

shows transistorized schematic of a partial product generator using GDI MUX based AND gate [2].

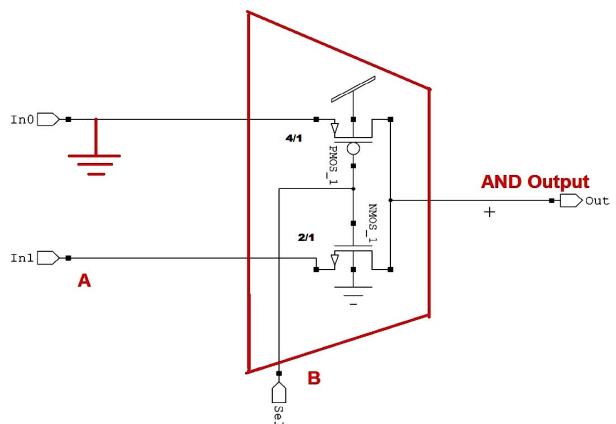


Fig. 3: GDI MUX based AND gate

B. Counter Based Partial Product Accumulation

The reduction of partial products can be done by counters or compressors and full adders, half adders. For more than three partial products having same weight counter or

compressor circuits are preferred instead of full adder series. An (m,p) counter takes an m bit input bits from a column and produces a p bits output which detects the number of input 1 bits. That means it counts the number of input bits set to 1. Where as A (m:p) compressor is any circuit that takes in m equal weight input sum and carry in bits and produces p bit count along with additional carry bit. In our proposed design counter based reduction technique has been applied as it reduces the no of reduction stages than compressor based technique. Conventional high speed counter designs can be found from [10].

In the proposed design the counters have been implemented using GDI gates. A transistorized schematic of GDI AND gate has been shown in fig. 3. To design different types of counter circuit we also require designing GDI OR gate and XOR gate. Two transistor based GDI OR gate and three transistors based XOR gate schematics have been shown in fig. 4 & 5 respectively.

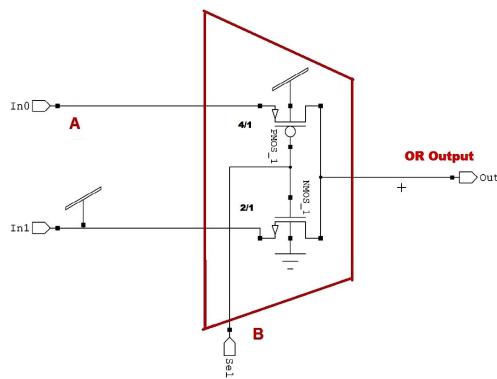


Fig. 4. GDI MUX based OR gate

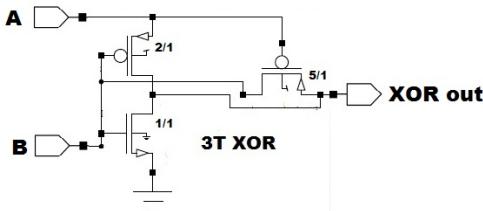


Fig. 5. Three transistors based XOR gate schematic

For accumulation of the partial products of same weights 7:3, 6:3, 5:3 and 4:3 counters are used along with full adders and half adders.

1) 7:3 Counter

A 7:3 counter can take seven input bits ($x_0, x_1, x_2, x_3, x_4, x_5, x_6$) and produces three outputs (Sum, Cout1, Cout2) as follows,-

$$\left. \begin{aligned} Sum &= [(x_0 \oplus x_1) \oplus (x_2 \oplus x_3)] \oplus [(x_4 \oplus x_5) \oplus x_6] \\ C_{out1} &= (m_1 \oplus m_2) \oplus m_3 \\ C_{out2} &= (m_1 \cdot m_2) + ((m_1 \oplus m_2) \cdot m_3) \end{aligned} \right\} \quad (1)$$

where

$$\begin{aligned} m_1 &= x_0 \cdot x_1 \cdot x_2 \cdot x_3 + ((x_0 \oplus x_1) \cdot (x_2 + x_3)) \\ m_2 &= [(x_4 + x_5) \cdot x_6 + x_4 \cdot x_5] \\ m_3 &= [x_0 \cdot x_1 \cdot x_2 \cdot x_3 + ((x_0 \oplus x_1) \oplus (x_2 \oplus x_3))] \cdot [(x_4 \oplus x_5) \oplus x_6] \end{aligned}$$

The GDI gates based schematics of 7:3 counter is shown in fig. 6. The total no. transistors required to design the counter

is (8 XOR gates x 3T)+(8 AND gates x 2T)+(8 OR gates x 2T) equal to 56.

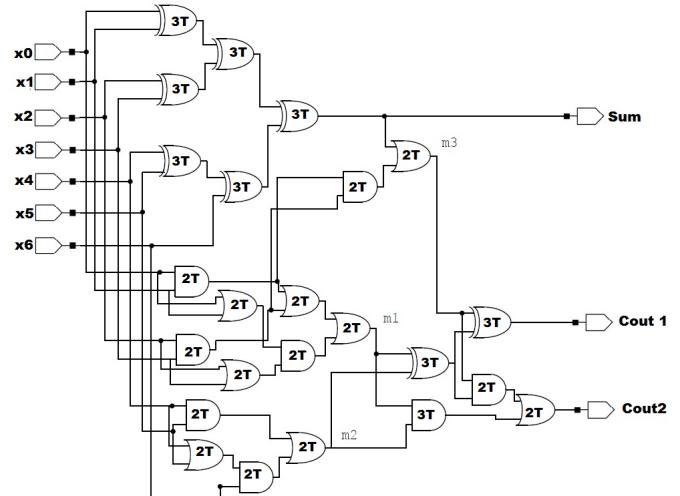


Fig. 6. GDI AND (2T), GDI OR(2T) and XOR (3T) gate based 7:3 counter schematic

2) 6:3 Counter

A 6:3 counter can take seven input bits ($x_0, x_1, x_2, x_3, x_4, x_5$) and produces three outputs (Sum, Cout1, Cout2) as follows,-

$$\left. \begin{aligned} Sum &= p_0 \oplus p_1 \oplus p_2 \\ C_{out1} &= (p_0 \cdot p_1 \oplus p_0 \cdot p_2 \oplus p_1 \cdot p_2) \oplus (g_0 \oplus g_1 \oplus g_2) \\ C_{out2} &= (p_0 \cdot g_1 + p_0 \cdot g_2 + g_1 \cdot g_2) + ((p_0 \cdot p_1) \cdot g_2) \\ &\quad + ((p_0 \cdot p_2) \cdot g_1) + ((p_1 \cdot p_2) \cdot g_0) \end{aligned} \right\} \quad (2)$$

where,

$$\left. \begin{aligned} p_0 &= x_0 \oplus x_1, \quad p_1 = x_2 \oplus x_3, \quad p_2 = x_4 \oplus x_5 \\ g_0 &= x_0 \cdot x_1, \quad g_1 = x_2 \cdot x_3, \quad g_2 = x_4 \cdot x_5 \end{aligned} \right\} \quad (3)$$

The GDI gates based schematics of 6:3 counter is shown in figure 7. The total no. transistors required to design the counter is (10 XOR gates x 3T)+(12 AND gates x 2T)+(5 OR gates x 2T) equal to 64.

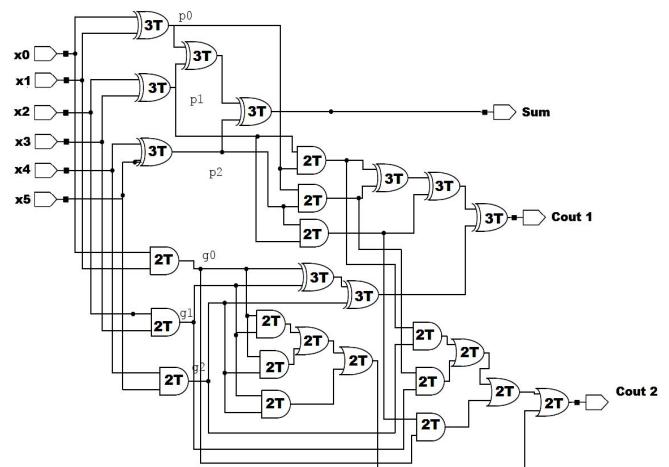


Fig. 7. GDI AND (2T), GDI OR(2T) and XOR (3T) gate based 6:3 counter schematic

3) 5:3 Counter

A 5:3 counter can take seven input bits (x_0, x_1, x_2, x_3, x_4) and produces three outputs (Sum, Cout1, Cout2) as follows,-

$$\begin{aligned} \text{Sum} &= p0 \oplus p1 \oplus x4 \\ C_{out1} &= (g0 \oplus g1 \oplus h0) \oplus (h1 \oplus h2) \oplus ((p0 \cdot p1) \oplus h3) \\ C_{out2} &= (g0 \cdot g1 + g0 \cdot h2) + (g0 \cdot h3) + (g1 \cdot h0 + g1 \cdot h1) \end{aligned} \quad \left. \right\} (4)$$

where

$$h0 = x0 \cdot x4, h1 = x1 \cdot x4, h2 = x2 \cdot x4, h3 = x3 \cdot x4$$

The GDI gates based schematics of 5:3 counter is shown in figure 8. The total no. transistors required to design the counter is (10 XOR gates x 3T)+(12 AND gates x 2T)+(4 OR gates x 2T) equal to 62.

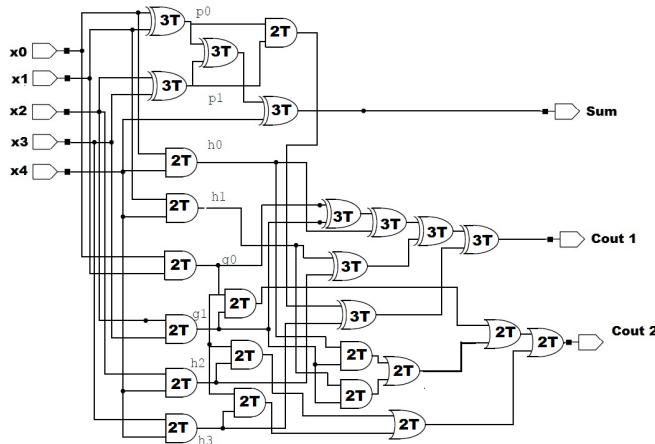


Fig. 8. GDI AND (2T), GDI OR(2T) and XOR (3T) gate based 5:3 counter schematic

4) 4:3 Counter

A 4:3 counter can take seven input bits (x_0, x_1, x_2, x_3) and produces three outputs (Sum, Cout1, Cout2) as follows,-

$$\begin{aligned} \text{Sum} &= p0 \oplus p1 \\ C_{out1} &= (p0 \cdot p1) + (g0 \oplus g1) \\ C_{out2} &= g0 \cdot g1 \end{aligned} \quad \left. \right\} (5)$$

The GDI gates based schematics of 4:3 counter is shown in figure 9. The total no. transistors required to design the counter is (4 XOR gates x 3T)+(4 AND gates x 2T)+(1 OR gates x 2T) equal to 22.

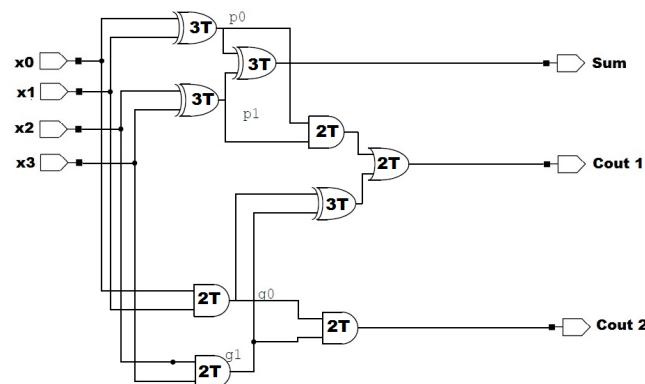


Fig. 9. GDI AND (2T), GDI OR(2T) and XOR (3T) gate based 4:3 counter schematic

5) 8T Full Adders & 5T Half Adders

In order to accumulate three partial products of same weight full adder can be used. In the proposed design full adders have been implemented using two nos. of 3T XOR gates and a GDI MUX. Similarly, half adders are used to accumulate two nos. of partial products of same weight. In

the proposed design half adders are implemented using a 3T XOR and 2T GDI MUX [2].

C. Final 2N bit RCA ADDER Stage

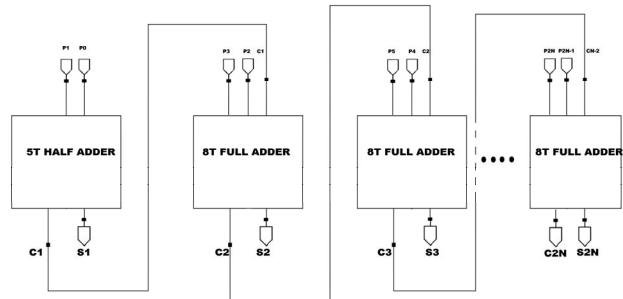


Fig. 10. Final stage 2N bit RCA adder schematic

When the partial products of same weight are reduced into two rows the final addition is done by RCA adder. The proposed RCA adder consists of $(2N-1)$ nos. of eight transistors based full adders and five transistors based half adder circuit. The outputs of the RCA adder is $(2N+1)$ bits long produces the final multiplied output.

III. SIMULATION RESULTS AND ANALYSIS

The proposed design is implemented for 4x4 bit multiplication example. A generalized schematic of 4x4 bit Wallace tree multiplier circuit is shown in fig. 11. The multiplicand is taken as $(1101)_2$ and the multiplier is $(1011)_2$. The simulation environment is set with standard EDA simulator using generic 250nm technology. Table I shows the input specifications for functional test of the design.

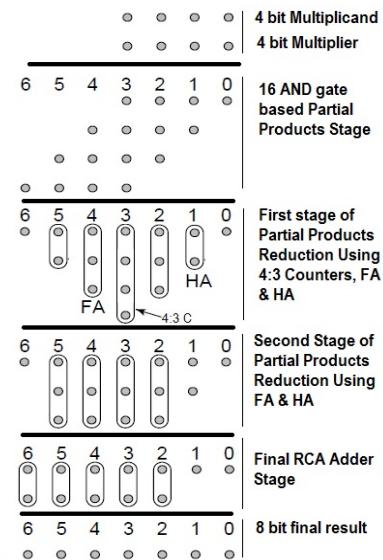


Fig. 11. 4x4 bit Wallace tree multiplier schematic

TABLE I. INPUT SPECIFICATION FOR SIMULATION

Input Type	Bit
Multiplicand	1101
Multiplier	1011
Zero value	0 v
One value	2.5 v
Bit duration	10ns
Rise and fall time	1ns

The simulation results are compared with existing designs of multipliers along with our proposed counter based GDI Wallace tree multiplier. The comparisons are made in terms of timing and power analysis and transistors counts. The proposed 4x4 counter based GDI Wallace tree multiplier consists of 16 AND gates for partial product generation. The partial product reduction is done by one 4:3 GDI counter, 6 nos. of 8 transistorized full adders and 7 nos. of 5 transistorized half adders in two stages. The circuit shows 5% improvement in latency and 43% improvement in power consumption with respect to conventional Booth multiplier. Table II shows detailed simulation results of proposed design along with other state of art designs.

TABLE II: DETAILED SIMULATION RESULT

	4x4 Array Multiplier	4x4 Vedic Multiplier	4x4 Wallace tree multiplier	4x4 Booth multiplier	Proposed Design simulated for 4x4 multiplier
<i>Power (mw)</i>	56.94	76.35	55.73	17.34	9.87
<i>Delay (ns)</i>	1.99	1.75	1.67	1.39	1.32
<i>Area (Trs. count)</i>	544	304	384	226	137

IV. CONCLUSION & FUTURE SCOPE

Analyzing the simulation results, we can conclude that the proposed counter based GDI Wallace tree multiplier shows better results in low power consumption, area concern and delay performance. The improvement will be more for higher no of bits. The Wallace tree structure can be utilized for modified Booth Wallace Tree multiplier circuit for further improvement in signed bit multiplications. Such on-chip multipliers can be implemented in different portable micro-systems and MEMS processor units.

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