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Hybrid Cascaded Multilevel Inverter (HCMLI) with Improved Symmetrical 4-Level Submodule

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Abstract: - This paper proposes an improved symmetrical 4-level submodule as a basic cell for generating multiple DC voltage levels. A hybrid cascaded multilevel inverter (HCMLI) topology is formed by the combination of n submodules and a full-bridge. A comparative analysis against the recent multilevel inverters reveals that the proposed topology requires less number of switches and DC sources. In addition, the proposed submodule reduces the number of conducting switch and gate driver requirements compared to the widely used half-bridge submodule. To validate the operation of the proposed HCMLI topology, experimental results of a 9-level single-phase inverter controlled by selective harmonic elimination pulse-width-modulation is presented.

Index Terms: Hybrid cascaded multilevel inverter, reduced switch count, symmetrical submodule

I. INTRODUCTION

Multilevel inverters (MLI) have been an emerging and enabling technology for power electronics applications. The established MLI topologies such as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) which have been extensively researched are developed predominantly for high or medium voltage (>3kV) systems [1] initially. Nonetheless, the rapidly growing trend of renewable energy integration into power grids has also precipitated the application of MLIs in low voltage (e.g. 230V) power conversion system, mainly attributed to their competency in reducing output harmonics and switching losses [2]–[4]. As the availability of commercial MOSFETs or IGBTs up to 1.2kV blocking voltage is sufficiently cater for low voltage applications, there is a surge of research activities with prominent concern on reducing the switch count in MLIs [5].

The utilization of switched DC sources is one of the well-known concept for generating multiple voltage levels in MLIs. [6]. Their voltage boosting capability renders them particularly well-suited for renewable energy systems [7]. In [8], each DC source is connected to a half-bridge submodule to control the DC-link voltage across a full-bridge inverter. MLIs with hybrid configuration is another viable alternative to generate multiple voltage levels. For instance, [9] developed a hybrid MLI topology composed of FC and CHB. However, the utilization of FC has obvious shortcomings such that it requires large electrolytic capacitors as well as complicated control strategy to get rid of the capacitor voltage balancing problem.

Concerning the attempts in reducing the switch count, [10] has recently advocate the deployment of T-type inverter in MLIs. Meantime, an asymmetrical topology based on back-to-back connection of two T-type inverters is presented in [11]. As the freewheeling current path during dead-time is not taken into account, the multistep jumps in the voltage levels might give rise to the undesirable voltage spikes. In addition, this topology is unsuitable for symmetrical configuration. A more recent study in [12] proposed a relatively different MLI which is by far the most optimized topology with the least number of switch count. As shown in Fig. 1, it made use of the T-type inverter to control the polarity and phase sequence, and two input arms which consist of half-bridge submodules to increase the number of voltage levels.

This paper proposes a hybrid cascaded multilevel inverter (HCMLI) with improved symmetrical 4-level submodule which offers further reduction of switch count than [12]. The proposed submodule also demonstrates a reduction in the number of conducting switch and gate driver requirements. This paper is organized as follows: section II presents the proposed MLI topology and the comparative analysis against [12] and CHBMLI, section III discusses the experimental results of a 9-level single-phase prototype, section IV provides some insight into the promising applications of the proposed HCMLI, and finally section V draws the conclusion.

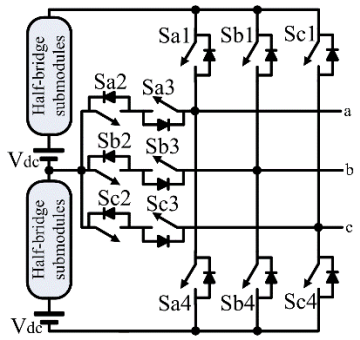

Fig. 1. Optimized MLI topology presented in [12].

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II. DESCRIPTION AND ANALYSIS OF THE PROPOSED TOPOLOGY

Fig. 2 depicts the circuit diagram of the proposed topology. Each phase is comprised of n series-connected 4-level submodule and a full-bridge, with the former is accountable for the generation of voltage levels while the latter is accountable for the control of phase voltage polarity. Each submodule is capable of generating up to four distinct voltage levels (0, V_{dc}, $2V_{dc}$, $3V_{dc}$) according to the switching states, as shown in Table I.

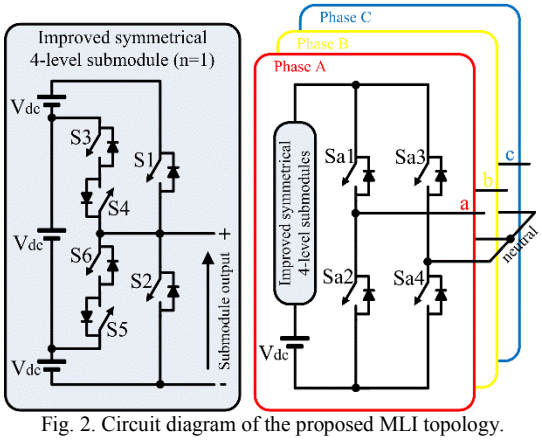

Fig. 2. Circuit diagram of the proposed MLI topology.

TABLE I
SWITCHING STATES OF THE PROPOSED SUBMODULE

	Submodule output			
Switch	**0**	**V_{dc}**	**$2V_{dc}$**	**$3V_{dc}$**
S1	0	0	0	1*
S2	1*	0	0	0
S3	0	0	1*	1
S4	1	1	1*	0
S5	0	1*	1	1
S6	1	1*	0	0

0 = OFF, 1 = ON, * = conducting switch

For the half-bridge submodule in [12] that attempts to produce 4 voltage levels, three half-bridge submodules or equivalently 6 switches are needed. The number of switches needed in the half-bridge submodule is thus the same as that needed in the proposed submodule. The proposed submodule, however, exhibits the following additional advantages:

(1) In the case of 0 and $3V_{dc}$ generation, there is only 1 conducting switch in the proposed submodule, as opposed to 3 conducting switches in the 3 half-bridge submodules.
(2) In the case of V_{dc} and $2V_{dc}$ generation, there are only 2 conducting switches in the proposed submodule, as opposed to 3 conducting switches in the 3 half-bridge submodules.
(3) The sources/emitters of switches S3,S4 and S5,S6 in the proposed submodule are interconnected and hence eliminate the need of individual isolated supply for their gate drivers. In this instance, to power up a total of 6 gate drivers, the proposed submodule requires only 4 isolated supplies, as opposed to 6 isolated supplies in the 3 half-bridge submodules.

The above advantages are more apparent if the number of levels increases (more submodules, n).

Considering the case of a three-phase inverter, Fig. 3 shows the comparison made against the conventional cascaded H-bridge multilevel inverter (CHBMLI) and the latest topology in [12]. When benchmarking with the conventional CHBMLI, the topology in [12] requires less number of switches for a given voltage level, however, at the expense of increased number of DC sources. On the other hand, the proposed HCMLI achieves significant reduction in the number of switches while retaining the number of DC sources same as the conventional CHBMLI. Note that the proposed HCMLI offers less number of switches and DC sources than the topology in [12], signifying that the proposed topology established higher degree of compactness.

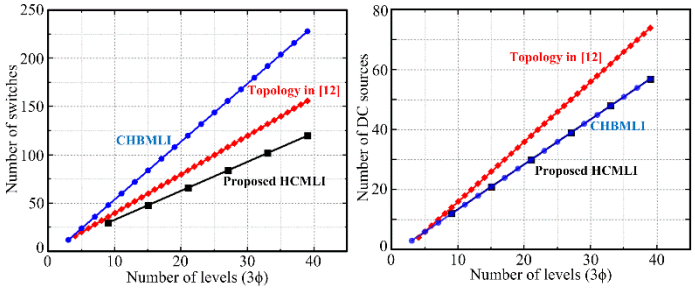

Fig. 3. The number of switches and DC sources as a function of the number of voltage levels for a three-phase inverter.

Fig. 4 illustrates the space vector diagram for the proposed topology and the topology in [12]. The generation of useless space vectors in [12] is attributed to the increased number of DC sources. These vectors, if mistakenly selected, will lead to potential damage to load since their vector magnitudes are significantly larger than the rated value. This problem is not a concern in this work as all the space vectors are useful and lie within the hexagon.

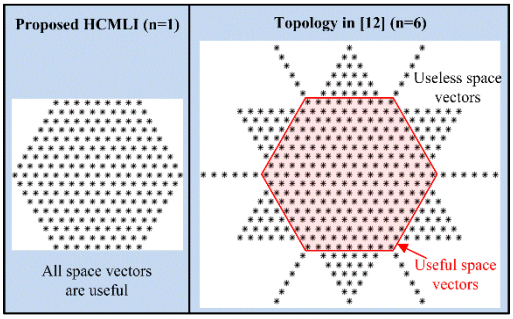

Fig. 4. Three-phase 9-level space vector diagram.

The number of switches and DC sources as a function of voltage levels for a single phase inverter are analyzed in Fig. 5. The topology in [12] is inferior to the conventional CHBMLI such that it requires equal number of switches but more number of DC sources than CHBMLI. In contrast, the proposed HCMLI needs as much DC sources as the conventional CHBMLI with significant reduction in the number of switches. Therefore, the proposed HCMLI is suitable for both three-phase and single-phase inverter. The equations for the number of levels, switches and DC sources as a function of the number of submodules are summarized in Table II.

Each switch in CHBMLI possesses the same voltage rating which is determined by the magnitude of each DC source. On the

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other hand, the maximum switch blocking voltage in the proposed HCMLI is equal to the sum of all DC sources, which is similar to the case in [12]. The switches in full-bridge are subjected to higher blocking voltage compared to the switches in submodules. Therefore, their voltage rating is equal to the maximum DC-link voltage. However, higher voltage rating is not a constraint in low voltage applications with the availability of commercial MOSFETs or IGBTs with voltage rating up to 1.2kV.

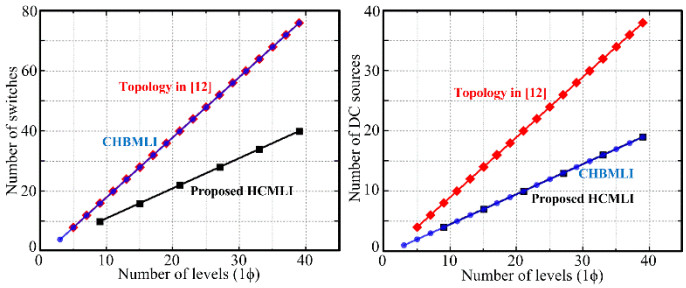


Fig. 5. The number of switches and DC sources as a function of the number of voltage levels for single-phase inverter.

TABLE II
NUMBER OF VOLTAGE LEVELS, SWITCHES, and DC SOURCES

	Proposed HCMLI	Topology in [12]	CHBMLI
3ϕ topology:			
Levels	6n+3	n+3	2n+1
Switches	3(6n+4)	4n+12	12n
DC sources	3(3n+1)	2n+2	3n
1ϕ topology:			
Levels	6n+3	2n+3	2n+1
Switches	6n+4	4n+4	4n
DC sources	3n+1	2n+2	n

n = number of submodules (or H-bridges for CHBMLI) for each phase

III. EXPERIMENTAL RESULTS

For verification, experimental prototype of a single-phase 9-level HCMLI with n=1 was tested. The prototype is depicted in Fig. 6. Selective harmonic elimination pulse width modulation (SHEPWM) [13] was implemented to compute the switching angles, α by solving the peak of fundamental component and undesirable low frequency harmonics up to $h = 6n+1$ given by (1).

$$\hat{V}_h = \frac{4V_{dc}}{h\pi}\left[\cos(h\alpha_1)+\cos(h\alpha_2)+\ldots+\cos(h\alpha_{3n+1})\right] \quad (1)$$

where $\hat{V}_h$ is the peak of h^{th} component,α is the switching angle and h is the harmonic order, $h = \{1,3,\ldots,6n+1\}$.
Genetic Algorithm was used to solve equation (1) through offline optimization of a cost function (2).

$$\text{Cost Function} = \left[100\frac{\hat{V}_1^* - \hat{V}_1}{\hat{V}_1^*}\right]^4 + \sum_{h=3,5,..}^{6n+1}\frac{1}{h}\left[50\frac{\hat{V}_h}{\hat{V}_1}\right]^2 \quad (2)$$

where $\hat{V}_1^* = \frac{(3n+1)(4V_{dc})m}{\pi}$ is the desirable/reference peak of fundamental component, and m is the modulation index. It is worth mentioning that the adoption of the aforementioned switching angle computation method is mainly for validating the operation of the proposed topology, and it can be readily replaced by more established techniques, such as that reported in [14]–[16].

The switching angles computed from (2) were stored in a look-up table while the switching signals were generated by a host-pc through Simulink Desktop Real Time software and National Instrument data acquisition device. The proposed HCMLI was implemented using Silicon Carbide power MOSFET (C2M0160120D) manufactured by CREE, with voltage rating and current rating of 1.2kV and 19A respectively. Four 30V isolated DC supplies were used as the input sources. Waveforms depicted in Fig. 7 validate the operation of the proposed topology. The efficiency recorded at 26.6W is 98.92%. The power measured using power meter are illustrated in Fig. 6. Fig. 7(b) verified that the switches S3,S4 and S5,S6 conduct only when the submodule produces $2V_{dc}$ and V_{dc} respectively. The prototype was also tested with four 12V batteries for both the purely resistive and resistive-inductive load. The waveforms depicted in Fig.8 further confirm the operation of the proposed multilevel inverter topology.

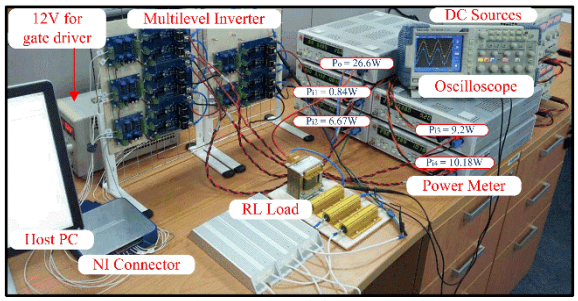
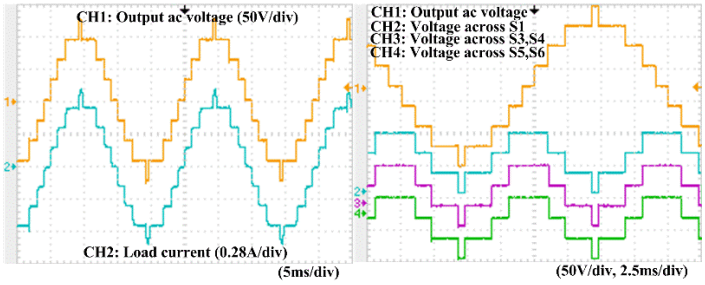
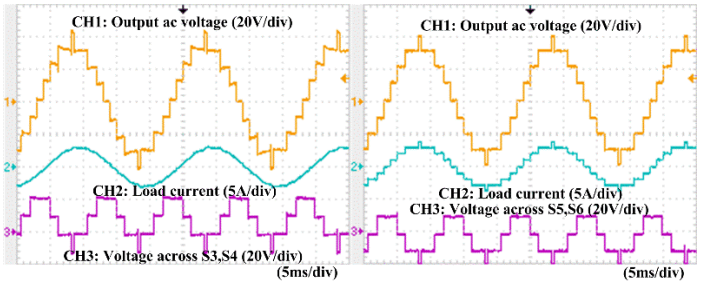


Fig. 6. Experimental prototype of the proposed MLI topology.



(a) (b)

Fig. 7. Experimental waveforms with four 30V DC supplies (R = 180Ω, L = 11mH), (a) output voltage and load current, (b) output voltage and voltages across switches in the proposed submodule.



(a) (b)

Fig. 8. Experimental waveforms with four 12V battery sources, (a) R = 10Ω, L = 11mH, and (b) R = 10Ω.

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IV. APPLICATIONS

Application of the hybrid MLI topologies in high-voltage system is less favorable than the conventional CHBMLI topology in view of their higher voltage stress across the switches in full-bridge (second stage). Nonetheless, with the availability of commercial MOSFETs or IGBTs up to 1.2kV blocking voltage, the hybrid MLI topologies have been a subject of increasing importance for low-voltage system. The proposed HCMLI, which has been validated its superiority over the most recent hybrid MLI topology in [12], is thus a promising alternative for CHBMLI in low voltage applications. This is because with the same number of DC sources, it requires substantially less number of switch count and conducting switch count.

Both the multilevel DC-link inverter [8] and the proposed HCMLI exhibit the same fundamental concept by which multiple DC voltage levels are generated across a full-bridge. Therefore, applications which are suitable for multilevel DC-link inverter are suited for the proposed HCMLI as well. For instance, the proposed HCMLI may be applied for renewable distributed generation involving fuel cells and photovoltaic cells [7] in low power range (e.g. <100kW) [8]. Besides, the successful applications of a hybrid MLI topology for battery storage system reported in [17] also implies the potentiality of the proposed HCMLI in this application. With the reduced number of conducting switches in the proposed submodule, efficiency improvement is expected in these applications.

One of the other potential applications of the proposed HCMLI is in three-phase machine drive system, in which the full-bridge is replaced by a three-phase two-level inverter. The number of switches is further reduced in this configuration, as compared to that in Fig. 2. Noting that the high torque ripple induced by direct torque control (DTC) at low speed is an issue which has been extensively studied in the literature, with emphasis mostly placed on establishing complicated controller design which involves high sampling frequency. This issue, in essence, can be easily resolved by generating multiple DC voltage levels across the DC-link of three-phase two-level inverter [18]. In other words, this implies that the proposed HCMLI is one of the promising solution in enhancing the performance of DTC.

V. CONCLUSION

In this paper, the working concept of the proposed HCMLI with improved symmetrical 4-level submodule was discussed and verified through experimental study. The topology is highly compact with reduced switch count. Modularity is achieved by cascading the proposed submodule. Moreover, the submodule is superior compared to the commonly used half-bridge submodule as it demonstrates reduction in the number of conducting switches for all voltage levels and it requires less isolated supply for gate drivers. Experimental results of a single-phase 9-level prototype with SHEPWM verified the feasibility of the proposed HCMLI.

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