# Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme

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*Abstract*—In this brief, a low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using TSMC CMOS 90-nm technology, the proposed design outperforms the conventional P-FF design data-close-to-output (ep-DCO) by 8.2% in data-to-Q delay. In the mean time, the performance edges on power and power-delay-product metrics are 22.7% and 29.7%, respectively.

*Index Terms*—Flip-flop (FF), low power, pulse-triggered.

## I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design [1], [2].

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations [3]–[8]. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In [9], a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique [10]–[13].
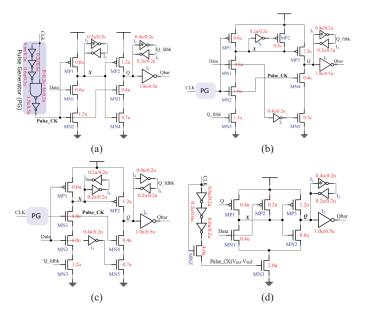
In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data "1" and "0," the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances.

Fig. 1. Conventional P-FF designs. (a) ep-DCO [7]. (b) CDFF [16]. (c) Static-CDFF [17]. (d) MHLFF [19].
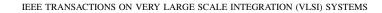
## II. PROPOSED P-FF DESIGN BASED ON A SIGNAL FEED THROUGH SCHEME

### A. Conventional Explicit Type P-FF Designs

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate [7]. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an *n*-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(a) shows a classic explicit P-FF design, named data-close-to-output (ep-DCO) [7]. It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node *X*. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed [14]–[18]. Fig. 1(b) shows a conditional discharged (CD) technique [16]. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node *X* is simplified and consists of an inverter plus a pull-up pMOS transistor only.

Fig. 1(c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique [17]. It differs from the CDFF
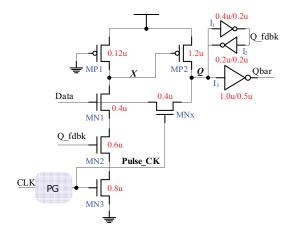
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Fig. 2.    Schematic of the proposed P-FF design.

design in using a static latch structure. Node $X$ is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flip-flop (MHLFF) [19] shown in Fig. 1(d) also uses a static latch. The keeper logic at node $X$ is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node $X$ when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node $X$ is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one $V_T$) is applied to the discharging transistor MN3. Second, node $X$ becomes floating in certain cases and its value may drift causing extra dc power [18].

*B. Proposed P-FF Design*

Recalling the four circuits reviewed in Section II-A, they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. 2(a), the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node $X$ can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node $X$ [20], [21]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two

nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feedthrough. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the proposed design shows the most balanced delay behaviors.

The principles of FF operations of the proposed design are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node $X$ is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node $X$ is discharged to turn on transistor MP2, which then pulls node Q high. Referring to Fig. 2(b), this corresponds to the worst case timing of the FF operations as the discharging path conducts only for a pulse duration. However, with the signal feed-through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. Referring to Fig. 2(c), when a "1" to "0" data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

III. SIMULATION RESULTS

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations. The compared designs include four explicit type P-FF designs shown in Fig. 1, an implicit type P-FF design named SDFF [5], a TG latch based P-FF design ep-SFF [7], plus two non-P-FF designs. One of them is a conventional TG master–slave-based FF (TGFF) and the other one is an adaptive-coupling-configured FF design (ACFF) [2]. A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain [as show in Fig. 1(a)] is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry as specified in Fig. 1(d).

The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption [10]–[13], the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input signals are generated through buffers. Since the proposed design requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with a 20-fF capacitor. An extra loading capacitance of 3 fF is also placed at the output of the clock buffer [18]. The operating condition used in simulations is 500 MHz/1.0 V. Six test patterns, each representing

TABLE I
FEATURE COMPARISON OF VARIOUS FF DESIGNS

| FF Designs | ep-DCO | CDFF | SCDFF | MHLFF | ep-SFF | TGFF | SDFF | ACFF | Proposed |
|---|---|---|---|---|---|---|---|---|---|
| Number of transistors | 28 | 30 | 31 | 19 | 24 | 22 | 25 | 22 | 24 |
| Layout area ($\mu m^2$) | 77.86 | 89.70 | 89.16 | 78.94 | 72.20 | 88.13 | 66.96 | 84.87 | 69.13 |
| Setup time (ps) | −83.8 | −88.2 | −44.8 | 1.5 | −73.2 | 67.3 | −26 | 112 | −85.7 |
| Hold time (ps) | 110 | 123.5 | 122.6 | 95.7 | 137.1 | −45.3 | 55.3 | −60.9 | 120.1 |
| Minimum D-to-Q delay (ps) | 118.9 | 129.5 | 140.0 | 173.8 | 136.8 | 271.4 | 132.5 | 284.5 | 109.1 |
| Average power (100% activity) $\mu$W | 34.41 | 34.08 | 35.16 | 31.82 | 31.14 | 34.18 | 30.69 | 33.06 | 30.09 |
| Average power (50% activity) $\mu$W | 28.72 | 25.57 | 25.13 | 24.23 | 24.57 | 25.13 | 24.73 | 20.11 | 23.43 |
| Average power (25% activity) $\mu$W | 25.26 | 20.97 | 21.25 | 20.32 | 21.28 | 20.39 | 21.22 | 13.29 | 19.52 |
| Average power (12.5% activity) $\mu$W | 24.03 | 19.16 | 19.28 | 18.53 | 19.82 | 18.33 | 20.02 | 10.40 | 17.89 |
| Average power (0% all-1) $\mu$W | 29.70 | 17.08 | 17.25 | 16.75 | 18.60 | 15.54 | 26.72 | 7.45 | 16.06 |
| Average power (0% all-0) $\mu$W | 16.96 | 17.12 | 17.19 | 16.75 | 18.10 | 16.70 | 11.98 | 7.55 | 16.17 |
| Optimal PDP (25% activity) pJ | 3.03 | 2.72 | 2.98 | 3.58 | 2.91 | 5.54 | 2.84 | 3.78 | 2.13 |

TABLE II
LEAKAGE POWER COMPARISON IN STANDBY MODE (nW)

| FF Designs | ep-DCO | CDFF | SCDFF | ep-SFF | TGFF | SDFF | ACFF | Proposed |
|---|---|---|---|---|---|---|---|---|
| (CLK, Data) = (0, 0) | 51.48 | 53.53 | 58.97 | 48.76 | 40.05 | 39.78 | 58.07 | 52.42 |
| (CLK, Data) = (0, 1) | 57.94 | 51.51 | 52.02 | 54.75 | 51.04 | 45.09 | 58.48 | 52.76 |
| (CLK, Data) = (1, 0) | 59.87 | 59.56 | 65.31 | 61.76 | 63.66 | 46.38 | 84.77 | 59.03 |
| (CLK, Data) = (1, 1) | 66.43 | 67.96 | 74.66 | 71.24 | 74.53 | 53.19 | 85.45 | 70.34 |
| Average | 58.93 | 58.14 | 62.74 | 59.13 | 57.32 | 46.11 | 71.69 | 58.63 |

a different data switching probability, are applied in simulations. Five of them are deterministic patterns, with 0% (all-0 or all-1), 12.5%, 25%, 50%, and 100% data transition probabilities, respectively.

### A. Power Consumption Performance of FF Designs

Table I summarizes the circuit features and the simulation results. For circuit features, although the proposed design does not use the least number of transistors, it has the smallest layout area. This is mainly attributed to the signal feed-through scheme, which largely reduces the transistor sizes on the discharging path. In terms of power behavior, the proposed design is the most efficient in five out of the six test patterns. The savings vary in different combinations of test pattern and FF design. For example, if a 25% data switching test pattern is used, the proposed design is more power-economical than all except the ACFF design. Its power saving against ep-DCO, CDFF, SCDFF, MHLFF, ep-SFF, SDFF, and TGFF are 22.7%, 6.9%, 8.1%, 8.3%, 3.9%, 4.3%, and 8%, respectively. The ep-DCO design consumes the largest power because of the superfluous internal node discharging problem. The ACFF design [2] leads in power efficiency because it uses a simplified pMOS latch design and exhibits a lighter loading to the clock network (only four MOS transistors are connected to the clock source directly). Its power efficiency is even more significant in the cases of zero or low input data switching activity. Similarly, another non-P-FF design, the TGFF, performs slightly better than the proposed one in the case of static input patterns (0% switching activity). However, when a test pattern with 100% switching activity is applied, the proposed deign is 9% and 12% more power efficient than the ACFF design and the TGFF design, respectively. This can be explained by the power overhead of the pulse generator regardless of the data patterns in all P-FF designs. The significance of this overhead, however, decreases as the data switching activity increases.

Table II summarizes the leakage powers of all FF designs under different combinations of clock and input signals. A possible concern on the proposed design arises from the pseudo-nMOS logic in the first stage. Although an always-on MP1 prevents node $X$ from a full voltage swing, it does not result in any dc power consumption problem. A full voltage swing can be expected at node Q because of the charge keeper with two inverters employed at node Q. A degraded "0" signal at node $X$ may affect the transition delay of node Q but not the voltage level. The voltage level of node Q remains at an intact value of $V_{DD}$. Referring to Table II, the leakage power consumption of the proposed design is very close to that of other P-FF designs. The MHLFF design is the one that suffers from a large dc power consumption because of a nonfull-swing internal node. Its dc (leakage) power consumption is much higher than others and is thus excluded from the comparison [18].

Since the proposed signal feed-through scheme requires occasional signal driving from the input node directly to the output node, we also calculate the power drawn by the pass transistor MNx (the extra power consumption caused by the signal feedthrough scheme). Post-layout simulation results show that this part accounts for only 8.47% of the total power consumption when the input data switching activity is 100%. The percentage reduces to 1.62% when the input data switching activity is lowered to 12.5%.

### B. Timing Parameters of FF Designs

After the analysis of power performances, we then examine the timing parameters of these FF designs. In this brief, the set-up time is measured as the optimal timing (with respect to the clock edge) of applying input data to minimize the product of power and D-to-Q delay. In other words, its choice is based on the optimization of PDP$_{DQ}$ instead of the D-to-Q delay alone.

Fig. 3(a) shows the simulation results of PDP curves versus setup time. The PDP values of the proposed design are smaller than other designs in almost all setup time settings. For most P-FF designs, the minimum PDP values occur at negative setup times. This is because of the extra delay introduced by the pulse generator so that input data can be applied after the triggering edge of the clock. Note that SDFF [5] is the only implicit type P-FF design under comparison. The integration of the pulse generation logic with the latch structure gives SDFF an inherent advantage in power consumption. Unfortunately,
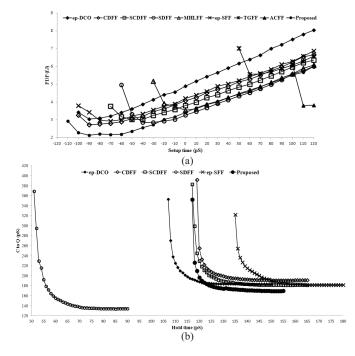
Fig. 3.   Setup time and hold time simulation results. (a) PDP$_{DQ}$ versus setup time settings. (b) C-to-Q delay versus hold time settings.
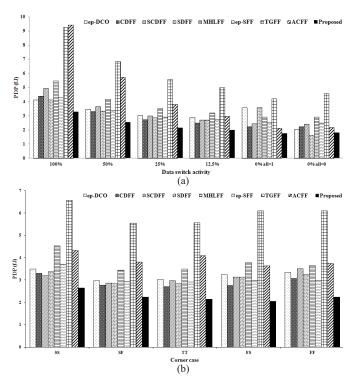


Fig. 4.   PDP performances. (a) Different data switching activity. (b) Different processor corners at 25% data switching activity.



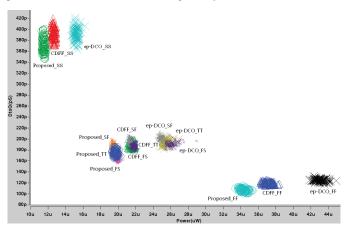Fig. 5.   Monte Carlo simulation results.

this advantage is partially offset by the excessive internal node discharging problem when input data remains high. As a result, its minimal PDP value is inferior to other explicit type P-FF designs.

Given a sufficient setup time, the hold time is measured as the point where the slope of the clock-to-Q delay curves equals –1 [22]. Fig. 3(b) shows the simulation results. Note that the curves of the MHLFF, TGFF, and ACFF designs are not included as they would appear in the leftmost part of the plot. Because of negative setup times, the hold times of P-FF designs are pushed back accordingly. The numbers are thus larger than the two non-P-FF designs, i.e., TGFF and ACFF. The measured setup and hold times of the proposed design are –85.7 and 120.1 ps, respectively. All but one P-FF designs under comparison exhibit similar timing parameters. The exception is the MHLFF design, which has a slightly positive setup time and a shorter hold time than its counterparts because of a simpler pulse generator. A longer hold time mainly affect the design of the driving logic. If P-FFs are adopted in the entire design, the hold time constraint can be easily satisfied because of a prolonged clock-to-Q delay property in P-FF designs. Introducing an input delay buffer is also a simple measure to alleviate the hold time requirement.

Fig. 4(a) shows the PDP$_{DQ}$ performance under different data switching activities. The proposed design outperforms others in all but the case of SDFF at 0% switching activity (all zero). The PDP$_{DQ}$ values obtained under the test pattern with 25% switching activity are also listed in Table I. The percentage of performance margin ranges from 21.7% (against the CDFF design) to 61.6% (against the TGFF design). Although the ACFF design leads in power efficiency, its power-delay performance is inferior to the proposed one. Since pulse generation circuits are sensitive to process variations. Fig. 4(b) shows the PDP$_{DQ}$ performance of these designs at different process corners under the condition of 25% data switching activity. Note that for each process corner (SS = 0.8 V/125 °C, TT = 1 V/25 °C, FF = 1.2 V/ –40 °C, SF = 1 V/25 °C, and FS = 1 V/25 °C), the setup time is scanned to obtain the best PDP$_{DQ}$ number. All P-FF designs function properly subject to process variations. The performance edge of the proposed design is maintained as well. Notably, the MHLFF design

has the worst PDP$_{DQ}$ performance (among the explicit type P-FF designs), especially at the SS process corner due to a large D-to-Q delay and the poor driving capability of its pulse generation circuit.

Fig. 5 shows the Monte Carlo simulations based on the variation in transistor sizes. The variation is modeled by a normal distribution with a standard deviation equal to 5% of the transistor width. Two P-FF type designs, i.e., ep-DCO, CDFF, and the proposed design are simulated. For each process corner, 100 simulation sweeps are conducted. The plot has a format of power as the $x$-axis and the D-to-Q delay as the $y$-axis. Therefore, the closer the point is to the lower left part of the plot, the better the performance of this design. The simulation points corresponding to the same P-FF design are marked with the same symbol (circle for the proposed design, cross for the ep-DCO design and triangle for the CDFF design), while symbol colors are used to distinguish the process corners. From the simulation results, the advantage of the proposed design is obvious in all simulation trials.

## IV. CONCLUSION

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feedthrough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

## ACKNOWLEDGMENT

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