Single-Phase Modified Quasi-Z-Source Cascaded Hybrid Five-Level Inverter

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***Abstract*—This paper proposes the combination of a novel modified quasi-Z-source (MqZS) inverter with a single-phase symmetrical hybrid three-level inverter in order to boost the inverter three-level output voltage. The proposed single-phase MqZS hybrid three-level inverter provides a higher boost ability and reduces the number of inductors in the source impedance, compared with both the single-phase three-level neural-point clamped (NPC) qZSI and the single-phase quasi-Z source cascaded multilevel inverter (CMI). Additionally, it can be extended to obtain the nine-level output voltage by cascading two three-level PWM switching cells with a separate MqZS and dc source, which herein is called a single-phase MqZS cascaded hybrid five-level inverter (MqZS-CHI). A modified modulation technique based on an alternative phase opposition disposition (APOD) scheme is suggested to effectively control the shoot-through state for boosting the dc-link voltage and balancing the two series capacitor voltages of the MqZS. The performances of both the proposed MqZS-CHI and the modulation techniques are verified through simulation and experimental results.**

***Index Terms*—Cascaded inverter, hybrid five-level inverter, modulation technique, quasi-Z-source.**

I. INTRODUCTION

IN traditional voltage source inverters (VSIs), the obtainable ac output voltage is limited to less than the dc input voltage, and thus an additional stage, consisting of a dc-dc boost converter, is required to obtain the desired ac output voltage. The additional dc-dc boost converter increases the cost and decreases the efficiency of the overall power converter. In order to overcome the limitations of traditional VSIs, both the Z-source inverter (ZSI) and the quasi ZSI (qZSI), in which the traditional dc-link is replaced with the Z-source impedance network, have been developed [1]-[5]. The ZSI/qZSI can boost the dc-link voltage by using the shoot-through state of the inverter bridge with a single power conversion stage. Therefore, it can reduce the component count and enhance the reliability. However, because the shoot-through state can only be regulated within a zero state, the practical boost factor of the qZSI/ZSI is usually restricted. This may limit further applications of the qZSI/ZSI in some areas that require high voltage gain for low-voltage energy sources, such as fuel-cell stacks and batteries [6].

Multilevel inverters are suited for high-voltage and high-power applications because they are designed to naturally share the total dc voltage between cascaded power semiconductors. By increasing the number of inverter voltage levels, it becomes possible to achieve high-voltage and low-distortion ac waveforms, as well as reduce the blocking voltage requirement of individual switching devices [7]-[10].

The integration techniques of the Z-source energy conversion concept applied to various multilevel inverters have been introduced to combine the advantages of both the Z-source inverter and the multilevel inverter. A dual Z-source inverter with reduced common-mode switching and voltage buck-boost capability has been designed [11]. However, an ac output transformer connected to dual-bridge ac outputs of dual ZSI is required to provide a five-level ac output voltage.

The three-level Z-source neural-point clamped (NPC) inverter and dc-link cascaded inverter are implemented by using a single impedance network and a single dc source [12]. They can reduce the system cost due to the lower numbers of Z-source impedance networks and dc sources. However, their boost ability is limited, as with the classic ZSI. In [13]-[14], the operation analysis and modulation techniques based on the phase disposition (PD) scheme of the three-level NPC ZSI are presented to achieve voltage boosting, better output voltage quality, and the minimal commutation count. Because those are accomplished by adding the triplen offset and shoot-through time to the sinusoidal references, its implementation is quite complex. The closed-loop control of both the capacitor voltage and the load current for a three-level NPC ZSI is discussed in [15] in order to obtain the desired dynamic response. The operation and modulation techniques for controlling the five-level NPC Z-source inverter, combining the two Z-source impedance networks with a separate dc source and the five-level NPC inverter, are analyzed [16].

Similarly, a three-level NPC quasi-ZSI is discussed in [17]-[19], where a quasi-Z-source impedance network is combined with an NPC structure. It can provide a continuous dc source current and multilevel output voltage. In spite of the fact that the three-level NPC qZSI has two identical quasi Z-source networks, its boost factor is the same as a traditional qZSI. The

Manuscript received May 31, 2017; revised July 10, 2017 and September 09, 2017; accepted November 06, 2017. This work was supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Trade, Industry & Energy (MOTIE) of the Republic of Korea (No. 20174030201490).

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2017.2779419, IEEE Transactions on Industrial Electronics

work in [20]-[25] focuses on the control method and analytic model design of a quasi-Z source cascaded multilevel inverter (qZS-CMI) for photovoltaic (PV) power generation systems. This approach includes distributed maximum power point tracking, voltage balance control, and the grid-current control strategy. Because each PV array connects to a separate qZS H-bridge module at the qZS-CMI, an additional qZS H-bridge module is required as the number of ac output voltage level increases by one step.

The work in [26] presents an inverter topology based on a cascaded Z-source impedance with two switching devices and one H-bridge unit, where the number of power semiconductor switches can be reduced with respect to traditional multilevel inverters. However, three Z-source impedances and three separate dc sources are required in order to generate the output voltage with seven voltage levels. The switching algorithms for five-level quasi-ZSI, combining the quasi-ZSI and the five-level inverter using a coupling inductor, are developed in [27]. The three-level LC-switching-based boost NPC inverter presented in [28] utilizes a lower number of passive reactive components as well as a single split dc source, and it needs the two extra switching devices. Most existing topologies including both the NPC ZSI/qZSI and the qZS-CMI require a large number of components for producing the boosted ac output voltage with five/nine voltage levels. Their boost factor is also limited to the boost factor of a classic ZSI/qZSI.

In order to reduce the number of components, especially inductors and raise the boost factor, this paper proposes a single-phase modified quasi-Z-source (MqZS) hybrid three-level inverter. In addition, a single-phase modified quasi-Z-source cascaded hybrid five-level inverter (MqZS-CHI) is designed by connecting two three-level PWM switching cells in series for producing a nine-level output voltage. The MqZS-CHI can be recommended for applications requiring a high output voltage with lower THD. A modified phase-shift modulation technique based on an alternative phase opposition disposition (APOD) scheme is proposed, in order to effectively control the shoot-through state for boosting the dc-link voltage. This modified modulation technique can offer a simple implementation and balance the two series capacitor voltages of the cascaded hybrid five-level inverter. Simulation and experimental results are carried out to verify the performances of the proposed topologies and modulation techniques.

II. Operation of the Single-Phase Modified Quasi-Z- Source Hybrid Three-Level Inverter

Fig. 1 shows the topology of a single-phase MqZS hybrid three-level inverter, where a MqZS can be implemented by removing two inductors of the quasi-Z-source impedance network and connecting a single diode between the dc voltage source and the upper impedance network [17]-[19], and it is incorporated with a symmetrical hybrid three-level inverter proposed in [29]. A symmetrical hybrid three-level PWM switching cell is linked to a single-phase full-bridge (SPFB) inverter with a low switching frequency, which consists of

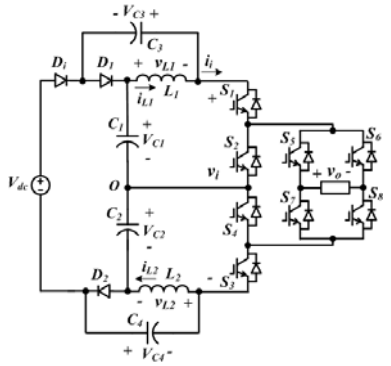

Fig. 1. A single-phase MqZS hybrid three-level inverter.

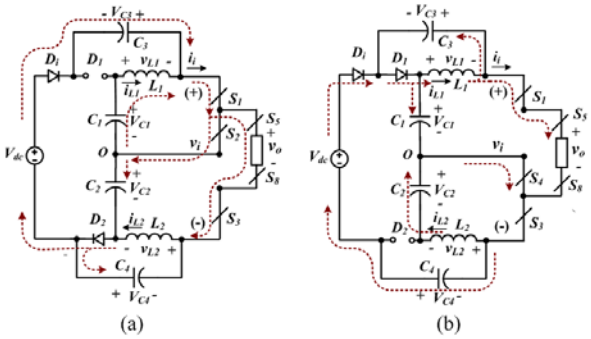

Fig. 2. Equivalent circuits of the MqZS hybrid three-level inverter: (a) upper shoot-through state, (b) lower shoot-through state.

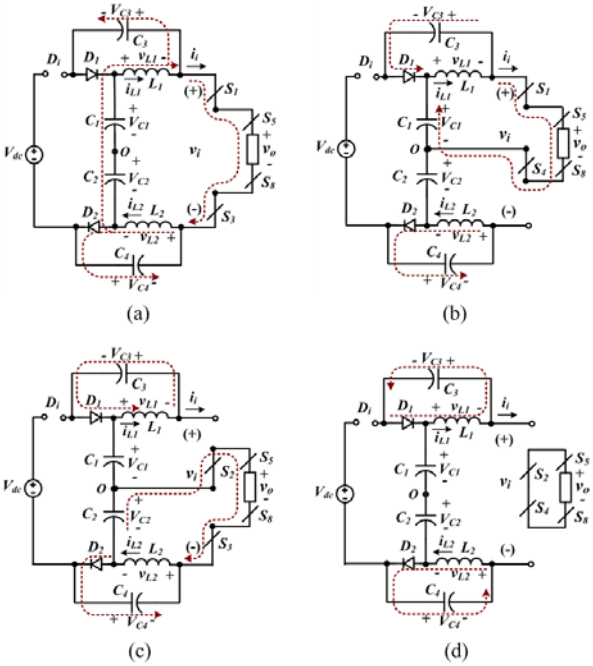

Fig. 3. Equivalent circuits in the non-shoot-through state: (a) active state I, (b) active state II, (c) active state III, (d) zero state.

switches S_5 to S_8. The pairs S_5/S_8 and S_6/S_7 are turned on complementarily according the polarity of the sinusoidal

reference signal in order to generate positive and negative output voltages, respectively. The high-frequency switches S_1 to S_4 are switched by a pulse width modulation pattern in order to generate the required output voltage.

The proposed impedance network consists of two inductors, four capacitors, and three diodes, whereas a conventional three-level quasi-Z-source NPC inverter utilizes four inductors, four capacitors, and two diodes in the q-source impedance, as discussed in [17]-[19]. Its dc-link voltage v_i can be boosted to a level twice as high as a quasi-Z-source NPC inverter. We assume $V_{C1}=V_{C2}$ and $V_{C3}=V_{C4}$ due to the symmetry of the impedance network.

The proposed single-phase MqZS hybrid three-level inverter has two operation modes: the shoot-through state and the non-shoot-through state. The operations of the two operating states are only discussed when the output voltage is positive by conducting the switching devices S_5 and S_8.

A. Shoot-Through State

Due to the neutral-point O at the mid-point between the two series capacitors, the MqZS three-level inverter has two kinds of shoot-through state modes, an upper shoot-through state (U_ST) and a lower shoot-through state (L_ST). Fig. 2 shows the equivalent circuits of the MqZS three-level inverter in the upper shoot-through state and lower shoot-through state. In the upper shoot-through state for the interval of T_{sh}, the switching devices S_1, S_2, and S_3 are turned on and the diodes D_i and D_2 are on, whereas diode D_1 is off, as shown in Fig. 2(a). The inductor L_1 stores energy from capacitor C_1 through S_1 and S_2, and the dc voltage source and capacitor C_3 supply the energy to the load and capacitor C_2. The switching devices S_5 and S_8 are turned on in order to generate a positive output voltage. Two inductor voltages v_{L1} and v_{L2}, and dc-link voltage v_i can be written as

$$v_{L1} = -V_{dc} - V_{C3} + V_{C1} + V_{C2}\ ,\ v_{L2} = -V_{C4} \tag{1}$$

$$v_i = V_{C2} + V_{C4}\,. \tag{2}$$

In the lower shoot-through state for the interval of T_{sh}, the switching devices S_1, S_3, and S_4 are turned on and the diodes D_i and D_1 are on, whereas diode D_2 is off, as shown in Fig. 2(b). The inductor L_2 stores energy from capacitor C_2 through S_3 and S_4, and the dc voltage source and capacitor C_4 supply the energy to the load and capacitor C_1. Two inductor voltages v_{L1} and v_{L2}, and the dc-link voltage v_i can be written as

$$v_{L1} = -V_{C3}\,,\ v_{L2} = -V_{dc} - V_{C4} + V_{C1} + V_{C2} = V_{C2} \tag{3}$$

$$v_i = V_{C1} + V_{C3}\,. \tag{4}$$

B. Non-Shoot-Through State

In the non-shoot-through state for the interval of T_a, diodes D_1 and D_2 are on whereas diode D_i is off. The non-shoot-through state is divided into active state I (AS-I), active state II (AS-II), active state III (AS-III), and the zero state (ZS). Fig. 3 shows the equivalent circuits in the non-shoot-through state. In active state I, the switching devices S_1 and S_3 are turned on, and the maximum dc-link voltage $\hat{v}_i$ is supplied to the load terminal. In active state II, the switching devices S_1 and S_4 are turned on, as shown in Fig. 3(b). Both the capacitor C_1 and inductor L_1 transfer energy to the inverter. In active state III, the switching devices S_2 and S_3 are turned on, as shown in Fig. 3(c). Both the capacitor C_2 and inductor L_2 transfer energy to the inverter. In active states II and III, half of the maximum dc-link voltage is supplied to the load terminal, and the energies stored in the inductors L_1 and L_2 charge the capacitors C_3 and C_4, respectively. In the zero state, a zero voltage is available at the load terminal, as shown in Fig. 3(d).

The two inductor voltages and dc-link voltage v_i for the non-shoot-through state, and the output voltage v_o for the four operating states can be written as

$$v_{L1} = -V_{C3}\ ,\ v_{L2} = -V_{C4} \tag{5}$$

$$v_i = \hat{v}_i = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{6}$$

$$v_o = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \hat{v}_i \quad \text{for active state I} \tag{7}$$

$$v_o = V_{C1} + V_{C3} = 0.5\hat{v}_i \quad \text{for active states II} \tag{8}$$

$$v_o = V_{C2} + V_{C4} = 0.5\hat{v}_i \quad \text{for active states III} \tag{9}$$

$$v_o = 0\,. \quad \text{for zero state} \tag{10}$$

C. Boost Factor

Applying a volt-second balance principle to inductors L_1 and L_2 from (1), (3) and (5) over one switching period T, and using $V_{C1}=V_{C2}$ and $V_{C3}=V_{C4}$ due to the symmetry of the impedance network, the four capacitor voltages can be expressed as

$$V_{C1} = V_{C2} = \frac{1 - T_{sh}/T}{1 - 2(T_{sh}/T)} V_{dc} = \frac{1-D}{1-2D} V_{dc} \tag{11}$$

$$V_{C3} = V_{C4} = \frac{D}{1-2D} V_{dc} \tag{12}$$

where T_{sh} is the shoot-through time during switching period T, and $D = T_{sh}/T$ is the shoot-through duty ratio. Substituting (11) and (12) into (6), the boost factor of inverter B can be derived as

$$B = \frac{\hat{v}_i}{V_{dc}} = \frac{2}{1-2D}\,. \tag{13}$$

D. Comparison with Existing Topologies

The performances of the proposed single-phase MqZS hybrid three-level inverter are compared with those of a single-phase three-level NPC qZSI [17] and single-phase three-level qZS-CMI [21] as the two representative existing topologies for producing a five-level output voltage.

The boost capabilities for the proposed topology and the two different topologies are investigated in Fig. 4. It can be noted that the boost factor of the proposed MqZS hybrid inverter is higher by a factor of two relative to that of the NPC qZSI and one module of qZS-CMI, which is the same as the boost factor of the classic qZSI.

Table I summarizes the required number of inductors, capacitors, switching devices, diode, and dc voltage source of the proposed topology and the two existing topologies for producing a five-level output voltage. The proposed topology can save two inductors with a single dc voltage source.

To properly compare the voltage stress for the three topologies, Table II describes the ratio of the voltage stress of

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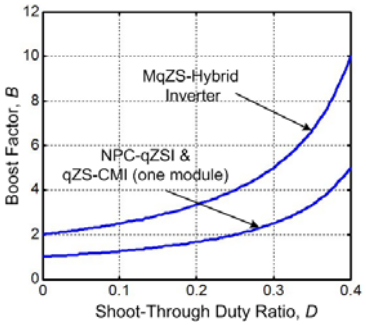

Fig. 4. Boost factor with a variation of the shoot-through duty ratio.

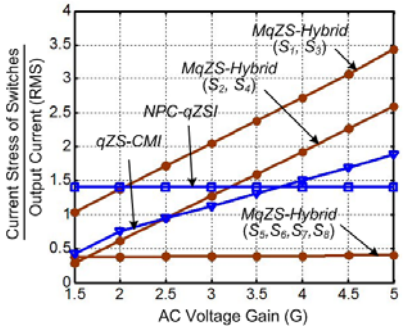

Fig. 5. Current stress of switching devices with a variation of ac voltage gain.

TABLE I

NUMBER OF COMPONENTS FOR PRODUCING FIVE-LEVEL OUTPUT VOLTAGE

Components	MqZS hybrid inverter	NPC-qZSI	qZS-CMI
Inductors	2	4	4
Capacitors	4	4	4
Switching devices	8	8	8
Diodes	3	6	2
DC voltage sources	1	1	2

TABLE II

COMPARISON OF VOLTAGE STRESS

Components	MqZS hybrid inverter		NPC-qZSI		qZS-CMI	
Switching devices	S_1-S_4	$\frac{1}{\sqrt{2}(1-D)}$	$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$	
	S_5-S_8	$\frac{\sqrt{2}}{(1-D)}$				
Capacitors	C_1, C_2	$\frac{1}{\sqrt{2}}$	C_1, C_4	$\frac{1}{\sqrt{2}}$	C_1	$\frac{1}{\sqrt{2}}$
	C_3, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_2, C_3	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_2	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$
Diodes	$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$	

TABLE III

COMPARISON OF CURRENT STRESS

Components	MqZS hybrid inverter		NPC-qZSI		qZS-CMI	
Inductors	L_1, L_2	$\frac{\sqrt{2}(1-D)}{1-2D}$	L_1- L_4	$\frac{1-D}{\sqrt{2}(1-2D)}$	L_1- L_4	$\frac{1-D}{\sqrt{2}(1-2D)}$
Diodes	D_i	$\frac{1-D}{\sqrt{2}D(1-2D)}$	D_1, D_2	$\frac{1-D}{\sqrt{2}(1-2D)}$	D_1, D_2	$\frac{1-D}{\sqrt{2}(1-2D)}$
	D_1, D_2	$\frac{1-D}{\sqrt{2}(1-2D)}$	D_3- D_6	0.25		

the switching devices, diodes, and capacitors to the RMS value of the ac output voltage. Two capacitors among the four capacitors for the three topologies have a lower voltage stress. The voltage stresses of all diodes for the three topologies are the same. The voltage stress across the switches S_5 to S_8 in the SPFB of the proposed topology is twice higher than that of the other switching devices, because the four switches in the SPFB

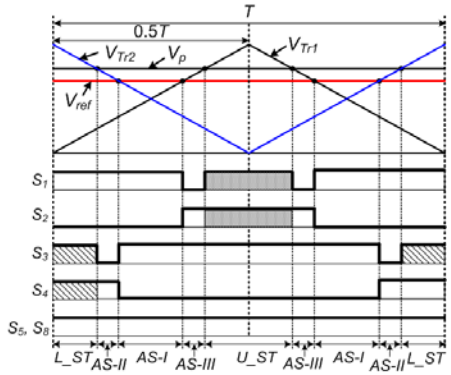

Fig. 6. Modified APOD technique for the MqZS hybrid three-level inverter.

are rated for the full dc-link voltage. On the other hand, the four switches in the SPFB can be implemented with low-frequency switching devices, and the switching loss can be reduced.

Table III describes the ratio of the current stress of inductors and diodes to the RMS value of the ac output current. The current stress of inductors of the proposed topology is twice higher than that of the other topologies. The current stresses of the two diodes D_1 and D_2 for the three topologies are the same. The current stress of diode D_i is higher than that of the two diodes D_1 and D_2, and the current stress of the four diodes of the NPC-qZSI is one-quarter of the load current [17]. Because the current stress of switches is dependent on the modulation index M as well as the short-through duty ratio D, the ratio of the current stress of switches to the RMS value of the ac output current with a variation of ac voltage gain expressed as $G = M{\cdot}D$ is shown in Fig. 5. The two switches S_2 and S_4 of the proposed MqZS hybrid inverter have the highest current stress, because both the shoot-through current and load current flow through both switches. The four switches of the SPFB circuit have the lowest current stress, because each switch of the SPFB circuit flows the load current during half-cycle of the inverter frequency. The current stress of all of switches in the NPC-qZSI is 1.4 times higher than the load current [17].

E. Boost Modulation Technique

A modulation technique of any type of multilevel inverter is quite challenging, and carrier-based PWM forms a common thread in the multilevel inverters [30]. Proper modulation of the

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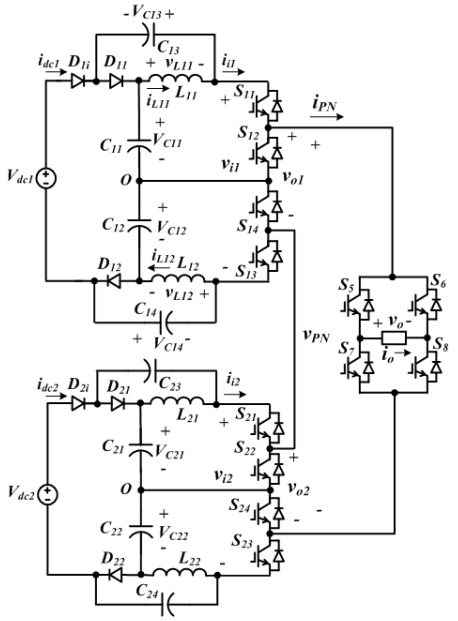

Fig. 7. The single-phase modified quasi-Z-source cascaded hybrid five- level inverter.

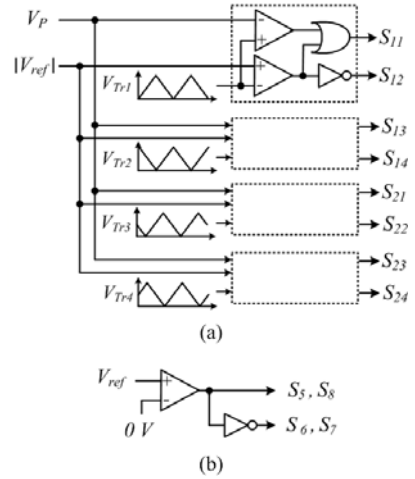

Fig. 8. Modified phase-shift modulation logic: (a) switching signals for PWM switching cells, (b) switching signals for the SPFB inverter.

(quasi-)Z-source multilevel inverters would require integration of the shoot-through sequence for the basic modulation process to achieve voltage boosting, a minimal number of device commutations, a reduction of the common-mode voltage, and minimal harmonic distortions [4], [13], [30]-[35].

A PWM control for the proposed topology is modified to effectively control the shoot-through state for boosting the dc-link voltage, and to balance the two series capacitor voltages of the three-level inverter. Among the various modulation strategies, this paper adapts a modified modulation technique based on an APOD scheme, as shown in Fig. 6 [29], [30]. A modified APOD scheme involves two vertically disposed triangular carriers with a 180° phase shift. Two carrier signals V_{Tr1}, V_{Tr2} are compared with the sinusoidal reference signal V_{ref} and the shoot-through envelope signal V_p. When the reference signal is greater than the carrier signal V_{Tr1}, the switching device S_1 is turned on. When the reference signal is greater than the carrier signal V_{Tr2}, the switching device S_3 is turned on. The other switching signals S_2 and S_4 are complementary to S_1 and S_3, respectively. The upper and lower shoot-through states can be adjusted by a comparison between the shoot-through envelope signal V_P and the two triangular carrier signals V_{Tr1} and V_{Tr2}, respectively. The pairs S_5/S_8 and S_6/S_7 are turned on complementarily according to the polarity of the sinusoidal reference signal, in order to generate positive and negative output voltages, respectively.

It can be seen that the upper and lower shoot-through states and the three kinds of active state (AS-I, AS-II, AS-III) are symmetrical. Both the series capacitor voltages V_{C1} and V_{C2} are used to generate the output voltage during the active state I. The capacitor voltage V_{C1} is used only at the upper shoot-through state, and the capacitor voltage V_{C2} is used only at the lower shoot-through state in order to generate the output voltage. The series capacitor voltages V_{C1} and V_{C2} are used during active states II and III, respectively. Therefore, two series capacitor voltages can be evenly shared to generate the output voltage by using a modified APOD technique. The two series capacitor voltages are kept in balance during one switching cycle due to the symmetry of the shoot-through states and active states.

III. Single-Phase Modified Quasi-Z- Source Cascaded Hybrid Five-Level Inverter

A. Structure of a Single-Phase MqZS-CHI

Fig. 7 shows the topology of the proposed single-phase MqZS-CHI in order to increase the number of output voltage levels. Two three-level PWM switching cells with a separate MqZS and a dc source are connected in series, and an SPFB inverter is connected at the two PWM switching cells, as defined in Fig. 7. A dc-link voltage of the SPFB inverter v_{PN} can be obtained from adding the output voltage of cell 1 v_{o1} to the output voltage of cell 2 v_{o2}. Assuming that the parameters and dc input voltages of two impedance networks are the same, the input voltages of both cells boosted by the Z-source impedance can be expressed as $v_{i1} = v_{i2} = v_i$. The dc-link voltage of the SPFB inverter v_{PN} could have five different voltage levels, namely, $2\hat{v}_i$, $1.5\hat{v}_i$, $\hat{v}_i$, $0.5\hat{v}_i$, or 0 V. Because the SPFB inverter could apply a dc-link voltage or its negative voltage to the load terminal, an output voltage with nine voltage levels can be produced.

B. Modified Modulation Technique of the MqZS-CHI

For a single-phase MqZS-CHI with two cascaded cells, it is necessary to use four triangular carrier signals with phase shifts of 0, π/2, π, and (3/2)π [30]. The switching signals for the PWM switching cell 1 can be obtained by comparing two triangular carriers V_{Tr1} and V_{Tr2} with a sinusoidal reference signal and the shoot-through envelope signal. The switching signals for the PWM switching cell 2 can be obtained by comparing the two triangular carriers V_{Tr3} and V_{Tr4} with the same two signals. The upper and lower shoot-through states of two cells can be generated by a comparison between the

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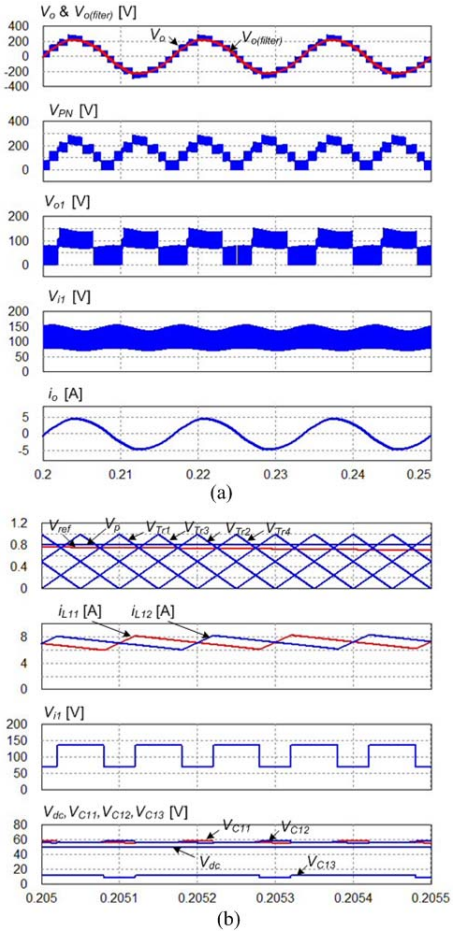

Fig. 9. Simulation results of the proposed MqZS-CHI when $M = 0.8$ and $D = 0.2$; (a) ac output and dc-link voltages, output and dc-link voltages of cell 1 and the ac output voltage, (b) carrier signals, shoot-through signal, reference signal, two inductor currents, dc-link and capacitor voltages of cell 1.

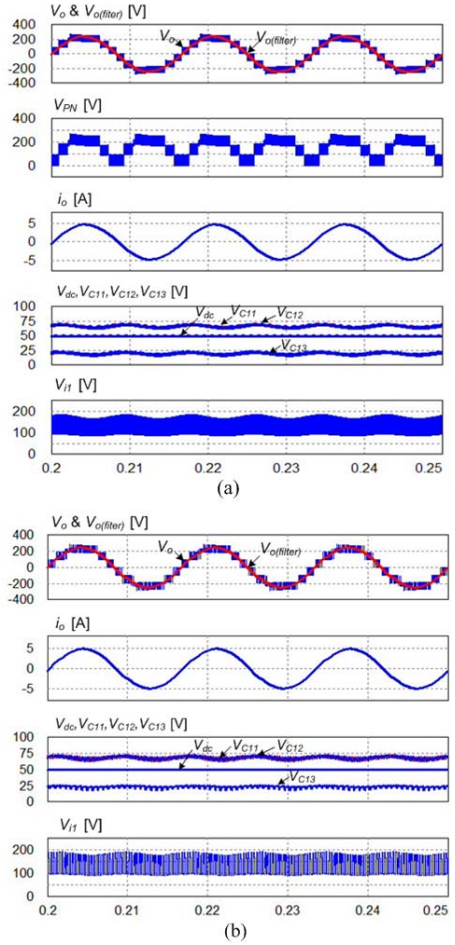

Fig. 10. Simulation results of the proposed inverter when $M = 0.7$, $D = 0.25$: (a) switching frequency = 10 kHz, (b) switching frequency = 3 kHz.

shoot-through envelope signal V_P and the four triangular carrier signals V_{Tr1}, V_{Tr2}, V_{Tr3}, and V_{Tr4}.

A modulation index M is defined as the ratio of the peak of a sinusoidal reference signal to the peak of the triangular carrier. The voltage levels of the dc-link voltage of the SPFB inverter are determined according to the range of the modulation index M. The dc-link voltage has five voltage levels for $0.75 \le M \le 1$, four voltage levels for $0.5 \le M < 0.75$, three voltage levels for $0.25 \le M < 0.5$, and two voltage levels for $0 \le M < 0.25$.

Fig. 8 shows the modified phase-shift modulation logic for generating all of the switching signals of the single-phase MqZS-CHI. In Fig. 8(a), four comparators share the same sinusoidal reference signal, and each triangular carrier has a 90° phase shift. The shoot-through state obtained from a comparison between each triangular carrier and the shoot-through envelope signal is included in only one switching signal among the pair of switching signals. As shown in Fig. 8(b), the four switching signals for the SPFB inverter can be generated by comparing the reference signal with 0 V.

IV. Simulation and Experimental Results

C. Simulation Results

Simulation studies of the proposed circuit are performed using the PSIM program. The dc input voltage V_{dc} is kept to 50 V. The switching frequency of the inverter is 10 kHz, and the inverter frequency is 60 Hz. The types and values of the circuit components used for the simulation and experiment are presented in Table IV.

Fig. 9 shows the simulation results for the proposed single-phase MqZS-CHI, when the modulation index $M = 0.8$ and $D = 0.2$. From Fig. 9(a), the dc-link voltage of cell 1 v_{i1} can be boosted to 140 V from 50 V dc input voltage, and a dc-link voltage of the SPFB inverter v_{PN} has five voltage levels. By performing switching operations of the SPFB inverter, we can obtain the output voltage with nine voltage levels, the RMS value of which is 160 V. From Fig. 9(b), two inductor currents of cell 1 i_{L1} and i_{L2} increase during an upper shoot-through state and a lower shoot-through state, respectively. The two series capacitor voltages V_{C11} and V_{C12} are balanced with 60V, and the capacitor voltage V_{C13} is 10V, which is much lower than the dc input voltage.

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TABLE IV
CIRCUIT PARAMETERS USED FOR SIMULATION AND EXPERIMENT

Components	Type / Value
DSP	TMS320F28335 / 32 bit, 150 MHz
Switching devices	IGBT SKM100GB12T4 / 1200 V, 150 A
Diodes	STTH200L06TC / 600 V, 30 A
Capacitor $C_{11}\cdots C_{22}$	DCMC102T450 /1000 μF
Inductors $L_{11}\cdots L_{22}$	1 mH
LC output filter	L_f = 1.2 mH, C_f = 25 μF
Resistive-inductive load	R_L = 50 Ω, L_L = 10.7 mH

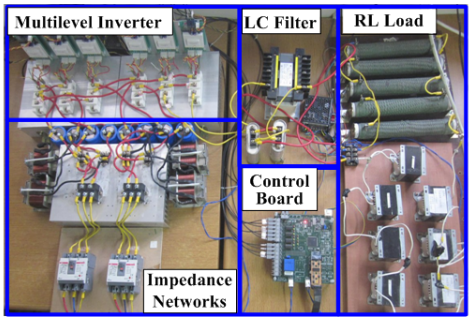

Fig. 11. Photograph of the experimental setup.

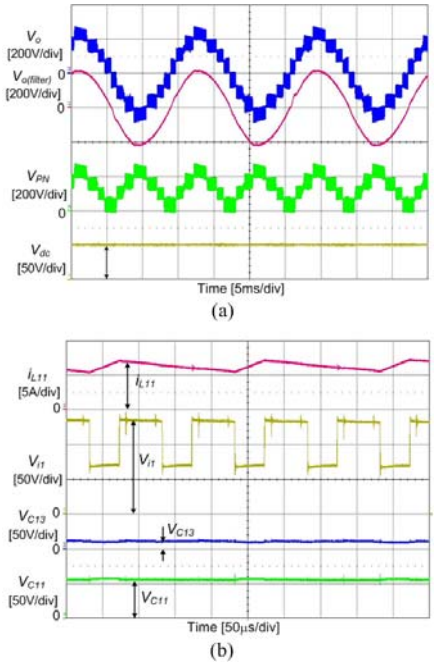

Fig. 12. Experimental results of the proposed cascaded five-level inverter when M = 0.8 and D = 0.2: (a) ac output voltage, dc-link voltage, and dc input voltage, (b) inductor current, dc-link and capacitor voltages of cell 1.

Fig. 10 shows the simulation results, when the modulation index M decreases to 0.7 and D increases to 0.25. The dc-link voltage of cell 1 can be boosted to 175 V, and all of capacitor voltages increase while raising D, where the output voltage has seven voltage levels. Fig. 10(b) shows the simulation results

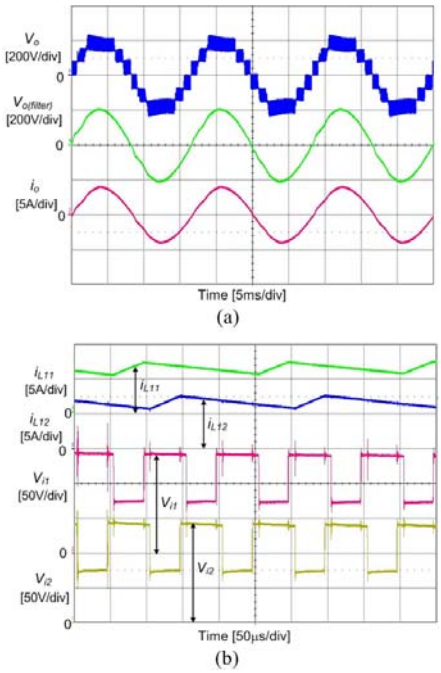

Fig. 13. Experimental results of the proposed cascaded five-level inverter when M = 0.7 and D = 0.2: (a) output voltage and output current, (b) inductor current and dc-link voltage of cell 1 and 2.

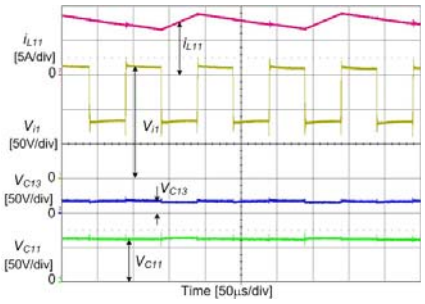

Fig. 14. Experimental results when M = 0.7 and D = 0.25.

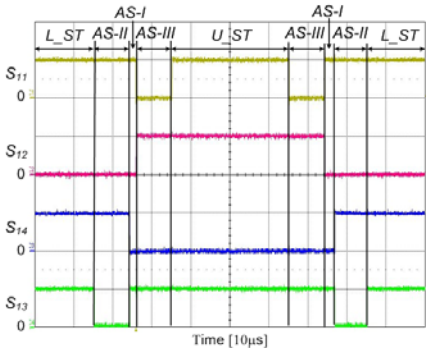

Fig. 15. PWM switching patterns of cell 1.

when the switching frequency of the inverter decreases from 10 kHz to 3 kHz. When the switching frequency of the inverter decreases to 3 kHz, the output voltage and current are nearly the

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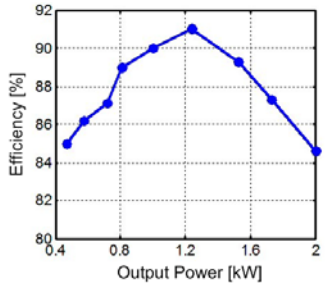

Fig. 16. Efficiency of proposed topology when $M = 0.8$ and $D = 0.15$.

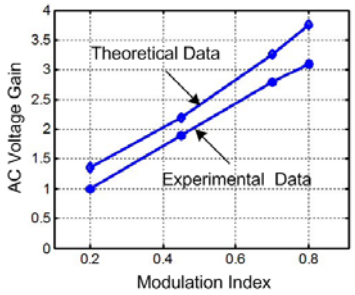

Fig. 17. AC voltage gains with a variation of modulation index.

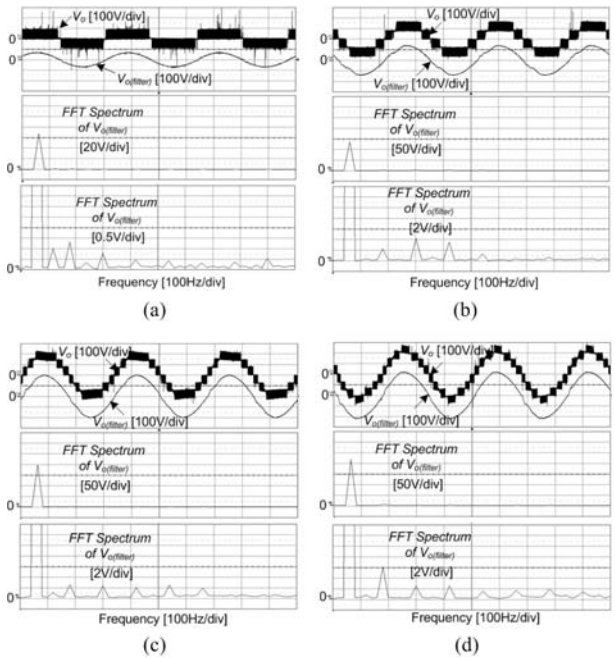

Fig. 18. FFT spectrum of filtered output voltage at $D = 0.2$: (a) $M = 0.2$, (b) $M = 0.45$. (c) $M = 0.7$, (d) $M = 0.8$.

same, and the high-frequency ripple components of the three capacitor voltages are slightly changed.

D. Experimental Results

A photograph of the experimental setup constructed at the laboratory was used to validate the operational analysis and simulation results for the proposed topology and modulation technique, and is shown in Fig. 11. The hardware system is composed of two MqZSs, a cascaded symmetrical hybrid inverter with 12 IGBT switches, an *LC* filter, an *RL* load, and a control board. The ac output is given a resistive-inductive load, and the control system is performed using a 32-bit DSP type TMS320F28335 as described in Table IV.

Fig. 12 shows the experimental results for the proposed MqZS-CHI when $M = 0.8$ and $D = 0.2$, which are the same operating conditions as for the simulation results shown in Fig. 9. The dc-link voltage of cell 1 is boosted to 138 V and the RMS value of the filtered output voltage is about 155 V. The output voltage and current, dc link voltage, inductor current, and capacitor voltages of experimental results shown in Fig. 12 are nearly identical with those of the simulation results shown in Fig. 9.

Fig. 13 shows the experimental results when M is reduced to 0.7 while maintaining $D = 0.2$. The output voltage has seven voltage steps, and its magnitude is reduced slightly to 148 Vrms. The dc link voltages of two cells are not changed, because D is kept at a value of 0.2. From Fig. 13 (b), the inductor currents of two cells i_{L11} and i_{L21} increase during the upper shoot-through period of each cell.

Fig. 14 shows the experimental results when D increases to 0.25 while maintaining $M = 0.7$. The peak of the dc-link voltage is raised to 165 V, and the two capacitor voltages V_{C11} and V_{C13} increase to 63V and 19V, respectively. The dc-link voltage and capacitor voltages of the experimental result are slightly lower than those of theoretical analysis, owing to the equivalent series resistances (ESRs) of the capacitors and inductors and the diode voltage drop.

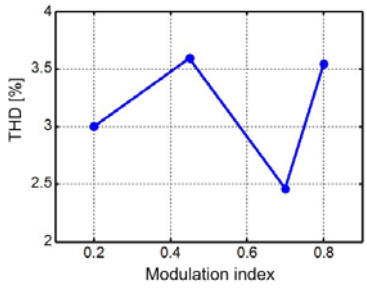

Fig. 19. THD of filtered ac output voltage.

Fig. 15 shows the PWM signals of cell 1 during one switching cycle. It can be seen that the inverter sequentially operates at the lower shoot-through state, the three kinds of active states, and the upper shoot-through state during the half switching period. The PWM patterns over one switching cycle are symmetric. The four switches in the SPFB inverter are switched on the inverter frequency, 60Hz.

Fig. 16 indicates the efficiency of the proposed MqZS-CHI, which ranges from 84.5 % to 91 % according to the output power variations, where the output power is adjusted by changing the load resistance value at the resistive load while the ac output voltage is kept constant. Fig. 17 indicates the theoretical and experimental ac voltage gains of the proposed MqZS-CHI, where the ac voltage gain is defined as the ratio of

the RMS value of the output voltage to the dc input voltage. It can be seen that the theoretical ac voltage gain is lower than the experimental ac voltage gain owing to the ESRs of the capacitors and inductors and the voltage drops of both the diodes and IGBTs.

Fig. 18 shows the FFT spectrum analysis of the filtered ac output voltage when M = 0.2, 0.45, 0.7, and 0.8 while D is kept at the value of 0.2. The output voltages have the low-order harmonics caused by the low-frequency ripple components of the capacitor voltages and dc-link voltage. Fig. 19 shows the THD of the filtered ac output voltage when M = 0.2, 0.45, 0.7, and 0.8, by using Fig. 18. The THD of the filtered ac output voltages with the four different voltage levels can be investigated, and it ranges from 2.49 % to 3.6 %.

V. Conclusions

This paper proposed two novel topologies for a single-phase MqZS hybrid three-level inverter and a single-phase MqZS-CHI designed by cascading two three-level PWM switching cells in order to obtain the output voltage with nine voltage levels. Compared with both the three-level NPC qZSI and the three-level qZS-CMI, the proposed MqZS hybrid three-level inverter reduces the number of inductors by two. Its boost factor is higher by a factor of two relative to that of the NPC qZSI, although dc source current is discontinuous. The proposed topology can produce a nine-level output voltage, which only requires nine high-frequency switching devices and four low-frequency switching devices in the SPFB. However, the voltage stress across the four low-frequency switches is twice or four times higher than that of the high-frequency switches. On the other hand, the four switches in the SPFB can be implemented with the low-frequency high-voltage switching devices, and the switching loss can be reduced.

Through the simulation and experimental results, the dc-link voltage of each cell is boosted by 2.8 times, and an output voltage of 155 Vrms can be obtained from a 50 V dc input voltage at the low shoot-through duty ratio as 0.2. The THD of the filtered ac output voltages with the four different voltage levels ranges from 2.49 % to 3.6 %. The proposed modulation technique offers a simple implementation, and the balance of the two series capacitor voltages of the three-level PWM switching cell can be achieved.

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