A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell

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***Abstract*— A novel 8-transistor (8T) static random access memory cell with improved data stability in subthreshold operation is designed. The proposed single-ended with dynamic feedback control 8T static RAM (SRAM) cell enhances the static noise margin (SNM) for ultralow power supply. It achieves write SNM of 1.4× and 1.28× as that of isoarea 6T and read-decoupled 8T (RD-8T), respectively, at 300 mV. The standard deviation of write SNM for 8T cell is reduced to 0.4× and 0.56× as that for 6T and RD-8T, respectively. It also possesses another striking feature of high read SNM ∼2.33×, 1.23×, and 0.89× as that of 5T, 6T, and RD-8T, respectively. The cell has hold SNM of 1.43×, 1.23×, and 1.05× as that of 5T, 6T, and RD-8T, respectively. The write time is 71% lesser than that of single-ended asymmetrical 8T cell. The proposed 8T consumes less write power 0.72×, 0.6×, and 0.85× as that of 5T, 6T, and isoarea RD-8T, respectively. The read power is 0.49× of 5T, 0.48× of 6T, and 0.64× of RD-8T. The power/energy consumption of 1-kb 8T SRAM array during read and write operations is 0.43× and 0.34×, respectively, of 1-kb 6T array. These features enable ultralow power applications of 8T.**

***Index Terms*— Single ended, static noise margin (SNM), static RAM (SRAM), subthreshold, ultralow power.**

I. Introduction

The portable microprocessor controlled devices contain embedded memory, which represents a large portion of the system-on-chip (SoC). These portable systems need ultralow power consuming circuits to utilize battery for longer duration. The power consumption can be minimized using nonconventional device structures, new circuit topologies, and optimizing the architecture. Although, voltage scaling has led to circuit operation in subthreshold regime with minimum power consumption, but there is a disadvantage of exponential reduction in performance [1]. The circuit operation in the subthreshold regime has paved path toward ultralow power embedded memories, mainly static RAMs (SRAMs) [1], [2]. However, in subthreshold regime, the data stability of SRAM cell is a severe problem and worsens with the scaling of MOSFET to subnanometer technology. Due to these limitations it becomes difficult to operate the conventional 6-transistor (6T) cell at ultralow voltage (ULV) power supply [1]–[6]. In addition, 6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation in [2]. This read decoupling approach is utilized by conventional 8-transistor [read decoupled 8-transistor (RD-8T)] cell which offers read static noise margin (RSNM) comparable with hold static noise margin (HSNM) [2]–[4]. However, RD-8T suffers from leakage introduced in read path. This leakage current increases with the scaling thereby, increasing the probability of failed read/write operations. Similar cells that maintain the cell current without disturbing the storage node are also proposed in [4]–[7].

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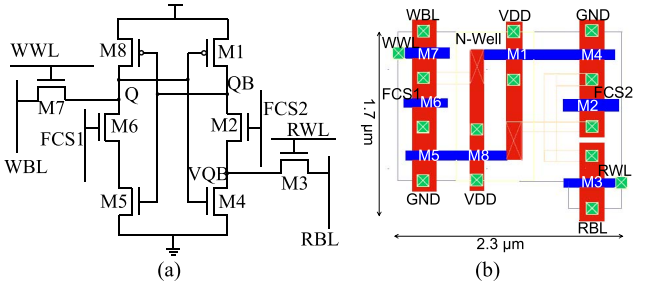

Fig. 1. Proposed 8T. (a) Schematic. (b) Layout.

Furthermore, to reduce the power consumption of differential bit line, a single-ended 5T bit cell is attractive due to its reduced area and considerable active and standby power saving capability as compared with conventional 6T SRAM cell [8]. However, writing 1 through an nMOS pass transistor in 5T is a design challenge. Another problem is to obtain optimized noise margin against process variations at all operations. In addition, the read stability of single ended 5T severely degrades in comparison with conventional 6T SRAM cell [8]. Various approaches like boosted supply (gate voltage of access transistor M5 is greater than VDD) generated from an additional circuit [8], gated-feedback write assist [9], 7T dual V_{TH} [10], asymmetrical write/read-assist 8T [11], and cross-point data-aware 9T [12] have been proposed to mitigate the above issues associated with 5T. Still, none of the cell could fulfill the requirement of improving both read and write stability in subthreshold regime for ultralow power applications.

In this brief, we have designed a new subthreshold 8T SRAM cell that operates in subnanometer technology node at ULV. This 8T SRAM cell uses single-ended write with dynamic feedback cutting to enhance writeability and dynamic read decoupling to avoid read disturb [12]–[16]. Due to read decoupled mechanism, the 9T cell [16] improves the RSNM by 4.1× as compared with conventional 6T cell. The 9T cell not only has larger write margin (WT) but also has faster write time [16]. As 8T is single-ended it can save more power consumption and area as compared with [16]. Here, we focus mainly on the stability of the cell which is affected by the process parameter variations. This brief is an elaborate discussion of our previous work [15] on 8T, including comparisons with other single-ended cells like conventional 5T and 8T [11]. We have also emphasized on delay, power and half-select issues for both row and column. Apart from this, a 1-kb SRAM array for proposed 8T and conventional 6T was also designed. The circuit simulations are done in United Microelectronics Corporation (UMC) 90-nm process technology at different power supplies.

II. Proposed 8T SRAM Cell Design

To make a cell stable in all operations, single-ended with dynamic feedback control (SE-DFC) cell is presented in Fig. 1(a). The single-ended design is used to reduce the differential switching power during read–write operation. The power consumed during switching/toggling of data on single bit line is lesser than that on differential

TABLE I
LAYOUT AREA IN UMC 90-nm TECHNOLOGY

	5T	6T	RD-8T	8T
Area (μm^2)	1.2	1.4	2.1	3.9
Area/(5T area)	1x	1.16x	1.75x	3.2x

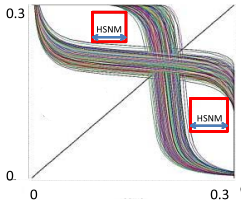

Fig. 2. Butterfly curve of HSNM for 8T.

bit-line pair. The SE-DFC enables writing through single nMOS in 8T. It also separates the read and write path and exhibits read decoupling. The structural change of cell is considered to enhance the immunity against the process–voltage–temperature (PVT) variations. It improves the static noise margin (SNM) of 8T cell in subthreshold/near-threshold region. The proposed 8T has one cross-coupled inverter pair, in which each inverter is made up of three cascaded transistors. These two stacked cross-coupled inverters: M1–M2–M4 and M8–M6–M5 retain the data during hold mode. The write word line (WWL) controls only one nMOS transistor M7, used to transfer the data from single write bit line (WBL). A separate read bit line (RBL) is used to transfer the data from cell to the output when read word line (RWL) is activated. Two columns biased feedback control signals: FCS1 and FCS2 lines are used to control the feedback cutting transistors: M6 and M2, respectively.

A. Cell Layout

For comparison of area, layout of 5T, 6T, RD-8T, and proposed 8T are drawn in UMC 90-nm CMOS technology, as shown in Table I. The sizes of MOSFETs used in proposed 8T cell are depicted in Fig. 1(b). The RD-8T occupies 1.3× area as compared with that of 6T. Due to the design constraints and contact area between M2, M3, M4, and M8 for proposed 8T, there is 2× area overhead as compared with 6T cell. Even though it has 2× area of 6T, but its better built-in process tolerance and dynamic voltage applicability enables it to be employed similar to cells with 1.8 × −2× area overhead [3]–[7].

B. Write Operation

The feedback cutting scheme is used to write into 8T. In this scheme, during write 1 operation FCS1 is made low which switches OFF M6. When the RWL is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1 and WWL is activated (Table II), then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1–M2–M4) changes the state of QB from 1 to 0. To write a 0 at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-up

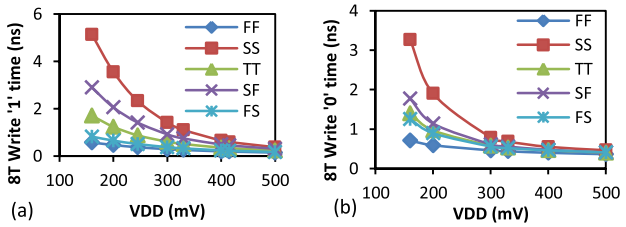

Fig. 3. (a) Write 1 time of 8T. (b) Write 0 time of 8T.

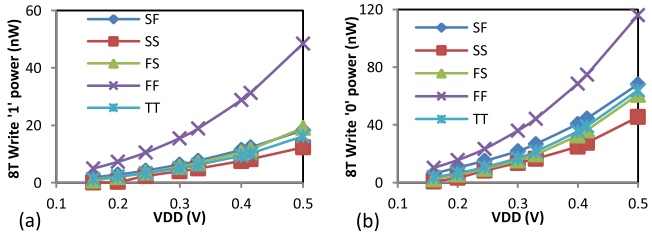

Fig. 4. (a) Write 1 power of 8T. (b) Write 0 power of 8T.

TABLE II
OPERATION TABLE OF PROPOSED 8T SRAM CELL

	Hold	Read	Write '1'	Write '0'	Row half-selected		Column half-selected	
					Write	Read	Write	Read
WWL	'0'	'0'	'1'	'1'	'1'	'0'	'0'	'0'
RWL	'0'	'1'	'0'	'0'	'0'	'1'	'0'	'0'
FCS1	'1'	'0'	'0'	'1'	'1'	'1'	'1'	'0'
FCS2	'1'	'0'	'1'	'0'	'1'	'1'	'0'	'0'
WBL	'1'	'1'	'1'	'0'	'1'	'1'	'1'	'1'
RBL	'1'	Dis-charge	'1'	'1'	'1'	'1'	'1'	'1'

pMOS M1 charges QB to 1. The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other. The simulations for WT were performed at all process corners. The WT (for write 1 and write 0) for 8T increases (Fig. 3) with the decrease in power supply. The WT is highest for slow nMOS and slow pMOS (SS) worst case corner, as shown in Fig. 3(a) and (b). During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS (FF) process corner dominated by the fast switching activities (Fig. 4). As write 0 operation is faster than write 1, the write 0 power consumption during write 0 is more as compared with that of write 1 [Fig. 4(a) and (b)].

C. Read Operation

The read operation is performed by precharging the RBL and activating RWL. If 1 is stored at node Q then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation (Table II), therefore, there is no direct disturbance on true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operation, Q is 0 and RBL holds precharged high value and the inverter sense amplifier gives 0 at output. Since M2 is OFF so virtual QB (VQB) is isolated from QB and this prevents the chance of disturbance in QB node voltage which ultimately reduces the read failure probability and improves the RSNM. During read operation, if FCS1/FCS2

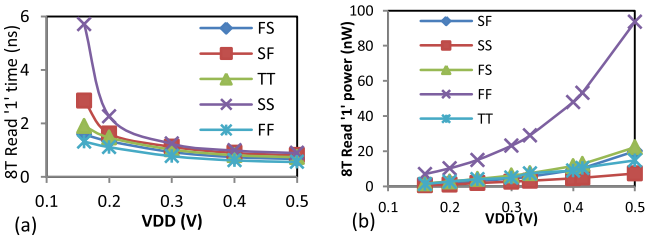

Fig. 5. (a) Read 1 time. (b) Read 1 power of 8T.

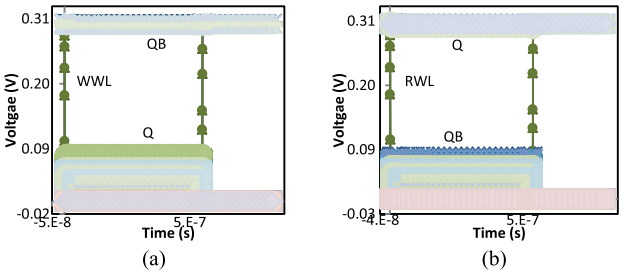

Fig. 6. Thousand MC simulations of row half-selected 8T. (a) Write. (b) Read.

turns 1 before RWL is turned 0 then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and Q, and any disturbance in QB will not affect Q. After that if RWL goes low, the positive feedback will restore the respective states ($Q = 1$ and QB $= 0$).

The read time is measured as the time the RWL signal is activated until the RBL is discharged to 90%. The SS process corner shows maximum read time, as shown in Fig. 5(a). It is followed by the SF corner and then by the other process corners.

Similar to write power, the FF process corner condition draws the highest read power. While read power consumption at other process corners closely follows for different power supplies [Fig. 5(b)].

D. Half-Selected Issue

Whenever a cell is selected for write operation, the voltage of true storage node (Q) of row half-selected cells will rise due to charge transfer from WBL [Fig. 6(a)]. The complementary storage node QB does not have strong connection to the bit line (RWL is OFF) (Table II), and therefore, less chances to flip the cell as compared with conventional 6T/RD-8T cell. This can be verified by 1000 Monte Carlo (MC) simulations, as shown in Fig. 6(a). Similarly, during read operation [Fig. 6(b)], the 1000 MC simulations show leakage immunity in row half-selected cells.

The control signals (FCS2 and FCS2) are common for all the cells connected in a column and during write operation of a cell, the other cells in same column will retain the data successfully. When column half-selected cells QB is 0 and FCS2 goes low (write 0 operation in selected cell in same column), then, QB will be floating for write period. The parasitic and gate capacitance of the transistors M5 and M8 connected to the true storage node QB of column half-selected cells will hold the data during write operation for selected cell [Fig. 7(a)]. The pulsewidth needed for write operation is very small as compared with the data retention time (in microseconds) of half-selected cells while, FCS2 is OFF to write 0 in selected cell. During read operation, FCS1 and FCS2 go low (Table II) in whole column and QB of column half-selected cell will be floating for read period. There is a small variation in the floating QB because of weak driving currents from power supply charging it, as shown

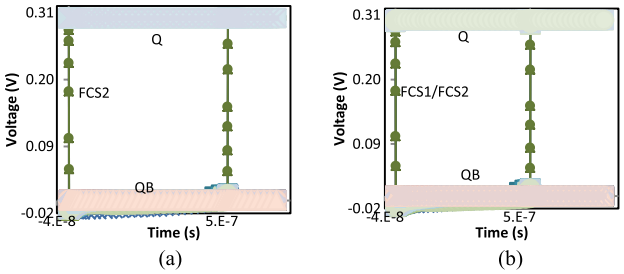

Fig. 7. 1000 MC simulations of column half-selected 8T. (a) Write. (b) Read.

in Fig. 7(b). The column half-selected cells can retain the data successfully even if the write/read or FCS1/FCS2 period greater than the required. To verify leakage immunity, 1000 MC simulations were performed during write [Fig. 7(a)] and read [Fig. 7(b)] operations.

E. Control Signal Generation

The feedback control signals, namely, FCS1 and FCS2 are data dependent. These signals connected in column-wise configuration [14]–[16]. Input data and column address signals are used to generate these control signals. A common circuit is used for a single column, therefore, there would be a small area overhead at array level. The proposed 8T cell has single-ended read port (as conventional read decoupled RD-8T), and therefore, the number of cells per bit line would be smaller as compared with differential 6T. Due to small length RBL the parasitic capacitances are less and the delay/power in read/write operation would not be affected significantly. The operation of proposed cell is based on the conditions of word lines, bit lines, and control signals, as shown in Table I.

III. Comparison and Discussion

To validate the design of proposed 8T, postlayout circuit simulations were performed for the isoarea (6T is upsized to same layout area as proposed 8T) conditions, as discussed in [6]. As RD-8T cell has separate read path, additional area can be used for access transistors to improve the WSNM. Thus, isoarea RD-8T cell has 3× upsized access transistors compared with its min-cell access transistors. The 6T is upsized to 4× of its min-cell (minimum possible W/L ratios for respective technology size). Similarly, 5T is upsized to 5× of its min-cell size. During simulations 25 °C and 50 MHz were maintained. The effect of PVT variations on cells is shown to justify the SNM in subthreshold region at ULV power supply. The MC simulations for 1000 samples considering inter/intra die random variations in threshold voltage (V_{TH}) were performed at different power supplies at different process corners. The approach followed in [7] is used to find WSNM, RSNM, and HSNM from butterfly curve (HSNM of 8T for 1000 MC shown in Fig. 2). This SNM is calculated graphically as the edge of the largest square that can be inserted inside the lobes of the butterfly curve [7].

A. Write Static Noise Margin (WSNM)

In RD-8T and 6T, during write operation there is a fight between access and pull-down transistor. On the other hand, in proposed 8T, during write operation, FCS is low, which turns OFF M4 thereby cutting the feedback and prevent the fight between access and pull-down transistor and restricting current through node Q to ground. When WWL is asserted, this provides unhindered charging of Q through WBL without any boosted supply on the gate of access transistor M7. This SE-DFC scheme enhances WSNM significantly and results in highest μ of WSNM of proposed 8T that is 1.4× and 1.28× as compared with that of isoarea 6T and RD-8T,

TABLE III
COMPARISON OF MEAN (μ) AND STANDARD DEVIATION (σ) FOR PROPOSED 8T, ISOAREA 5T, 6T, AND RD-8T SRAM CELLS

Bit-cell	SNM at worst process corner	VDD=200mV		VDD=300mV		VDD=400mV		VDD=500mV	
		μ (mV)	σ (mV)	μ (mV)	σ (mV)	μ (mV)	σ (mV)	μ (mV)	σ (mV)
Proposed 8T	WSNM (SF)	139.9	6.07	227.2	7.0	314.2	7.34	400.0	7.53
	RSNM (FS)	39.42	6.63	70.33	5.98	83.6	5.60	85.59	6.10
	HSNM (FS)	49.82	4.77	89.57	5.44	123.4	6.93	151.5	8.54
6T	WSNM (SF)	121.3	11.5	163.1	12.3	202.9	11.97	238.5	11.99
	RSNM (FS)	28.45	6.99	53.73	7.04	69.75	15.65	70.51	16.9
	HSNM (FS)	42.22	5.60	72.6	8.55	85.20	10.82	102.9	13.3
RD-8T	WSNM (SF)	139.2	11.6	176.3	11.1	225.6	11.32	271.4	11.63
	RSNM (FS)	45.32	4.70	78.9	8	97.20	11.1	110.93	14
	HSNM (FS)	47.22	4.60	83.69	7.55	99.30	10.82	120.9	13.3
5T	WSNM (SF)	Fails to write							
	RSNM (FS)	22.13	8.7	30.1	8.2	52.4	9.4	75.2	11.2
	HSNM (FS)	39.3	7.60	62.2	8.3	72.3	9.9	89.1	10.4
A-8T [11]	WSNM (SF)	70	Not given	90	Not given	120	Not given	170	Not given

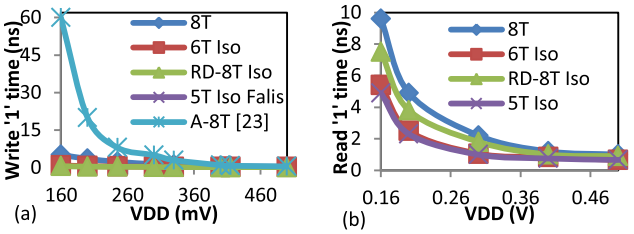

Fig. 8. Comparison at SS corner. (a) Write 1. (b) Read 1 time.

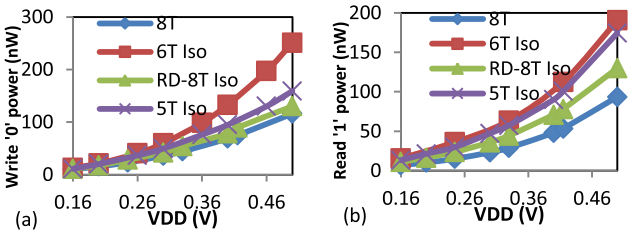

Fig. 9. Comparison of energy at FF corner. (a) Write 0. (b) Read 1.

respectively, where 5T fails to write. Apart from high μ, the proposed cell has the lowest σ of 0.4× and 0.56× of 6T and RD-8T, respectively, at 300 mV, as shown in Table III.

B. Read Static Noise Margin (RSNM)

The conventional read decoupled RD-8T cell has two separate nMOS transistors for read operation. Therefore, there is no read–write design conflict and μ of RSNM is 1.18× as that of proposed 8T. However, the μ of RSNM of proposed cell is good enough for a stable read operation under process variations and σ is 0.79× of RD-8T, as shown in Table III.

C. Hold Static Noise Margin (HSNM)

In data retention mode, all cells (5T, 6T, RD-8T, and 8T) are able to sustain the process variations at 300 mV at FS corner. The μ of HSNM of the proposed 8T is the best among the cells under consideration. Its value is 1.43×, 1.23×, and 1.05× as that of isoarea 5T, 6T, and RD-8T, respectively, as evident from Table III. Moreover, σ is the least among all, i.e., 0.65×, 0.63×, and 0.76× as that of isoarea 5T, 6T, and RD-8T, respectively.

D. Write and Read Time

The write 1 time of proposed 8T is compared with referenced A-8T [11] because 5T fails to perform write 1 operation. Fig. 8(a) compares the time to write 1 at worst case SS corner for different cells. It can be observed that the proposed 8T requires only 0.28× time as taken by A-8T at 300 mV. Being a single-ended SRAM cell, the proposed 8T requires relatively more time over differential cells (in this context 6T and RD-8T) to perform write operation. The write 1 time for proposed 8T is 7.05× and 3.71× as that for RD-8T and 6T, respectively, at 300 mV. In addition, the read 1 time of proposed cell is 2.22× of 5T/6T and 1.22× of RD-8T at 300 mV at SS corner, as shown in Fig. 8(b).

TABLE IV
COMPARISON OF LEAKAGE OF ISOAREA BIT CELLS

	I_{Leak}(nA) at VDD=0.2V	I_{Leak}(nA) at VDD=0.3V	I_{Leak}(nA) at VDD=0.4V	I_{Leak}(nA) at VDD=0.5V
8T	11.43	22.24	37.35	57.72
6T	24.94	50.79	89.44	144.9
RD-8T	13.94	26.78	44.66	68.75
5T	32.06	65.5	115.69	187.94

E. Write and Read Power Consumption

Fig. 9 depicts average write and read power consumption for 5T, 6T, RD-8T, and proposed 8T cells at worst case FF corner. It is evident from Fig. 9(a) that the proposed 8T consumes lesser write 0 power of 0.72×, 0.60×, and 0.85× as that consumed by isoarea 5T, 6T, and RD-8T, respectively, at 300 mV. The read 1 power consumption of proposed 8T is 0.49×, 0.48×, and 0.64× of isoarea 5T, 6T, and RD-8T, respectively, at 300 mV [Fig. 9(b)]. As isoarea 5T, 6T, and RD-8T have wider transistors, they have more leakage, and therefore, the proposed 8T has lowest leakage current (I_{Leak}) during standby mode, as shown in Table IV. The leakage and single-ended write/read operation of proposed 8T allows 64-bit cells/WBL and 32-bit cells/RBL at 200 mV.

F. Array Design

The proposed 8T with feedback cutting and read decoupled schemes is implemented in a 64 × 16-bit SRAM array in 90-nm UMC CMOS technology. To save the power/energy consumption, the array has been operated in subthreshold regime. The 1-kb SRAM comprises of four banks and each bank consists of 16 words ×16 bits. The similar architecture is used to design 1-kb array for 6T SRAM. Both arrays are compared in Table V at 300 mV and 10 MHz. The power/energy consumption of 8T SRAM array during read and write

TABLE V
COMPARISON OF 1-kb ARRAY OF 8T AND 6T SRAM AT 300 mV

UMC 90nm	Write '1' Power(μW) /Energy(fJ)	Write '1' Time (ns)	Write '0' Power(μW) /Energy(fJ)	Write '0' Time (ns)	Read Power(μW) /Energy(fJ)	Read Time (ns)
8T	6.71/6.71	49.88	9.39/9.39	36.25	15.8/15.8	26.37
6T	19.32/19.32	23.94	15.04/15.05	22.92	36.1/36.1	17.93

TABLE VI
COMPARISON OF SNM WITH [6] AND [7] AT 300 mV AND 25 °C

UMC 90nm	SNM (Monte Carlo analysis)	μ (mV)	σ (mV)
Proposed 8T	HSNM (FS corner)	89.57	5.44
	RSNM (FS corner)	70.33	5.98
	WSNM (SF corner)	227.29	7.00
10T cell [6]	HSNM (FS corner)	130	8.6
	RSNM (FS corner)	43.1	13
	WSNM (SF corner)	38.5	28.2
10T cell [7]	HSNM (FS corner)	74.2	11.4
	RSNM (FS corner)	84.3	9.2
	WSNM (SF corner)	44.5	13.3

operations is lower than 6T SRAM array. However, the read and write times are higher than 6T SRAM array.

IV. COMPARISON SUMMARY

The WSNM of proposed 8T is the highest among all other cells under consideration (5T, 6T, RD-8T, and A-8T [11]). RSNM is comparable with that of RD-8T, while the HSNM is slightly improved compared with other (5T, 6T, and RD-8T) cells. The proposed 8T cell has lower delay as compared with single-ended A-8T [11] during write operation and nearly same delay as single-ended RD-8T during read operation. The power consumption during read operation of proposed 8T is 0.49×, 0.48×, and 0.64× as compared with that of 5T, 6T, and RD-8T, respectively, at 300 mV. It can be observed that, the proposed cell has higher power saving capability during read/write operations, over the other cells under consideration. Like proposed 8T, 9T cell [16] also utilizes feedback cutting and dynamic read decoupling. 9T has 23-mV RSNM ($P_{\text{fail}} = 1e{-}9$) and due to differential write operation with feedback cutting, it gives write trip point of 160 mV. The proposed 8T cell is also compared with 10T cells [6], [7] found in the literature and tabulated in Table VI. It is worth noticing that, μ of WSNM of proposed 8T is the highest, while RSNM and HSNM are close to those of 10T cells (Table VI).

V. CONCLUSION

An 8T SRAM cell with high data stability (high μ and low σ) that operates in ULV supplies is presented. We attained enhanced SNM in subthreshold regime using SE-DFC and read decoupling schemes. The proposed cell's area is twice as that of 6T. Still, it's better built-in process tolerance and dynamic voltage applicability enables it to be employed similar to cells (8T, 9T, and 10T) along with $1.8\times - 2\times$ area overhead. The proposed 8T cell has high stability and can be operated at ULV of 200–300 mV power supplies. The advantage of reduced power consumption of the proposed 8T cell enables it to be employed for battery operated SoC design. Future and applications of the proposed 8T cell can potentially be in low/ULV and medium frequency operation like neural signal processor, subthreshold processor, wide-operating-range IA-32 processor, fast Fourier transform core, and low voltage cache operation.

REFERENCES

[1] K. Roy and S. Prasad, *Low-Power CMOS VLSI Circuit Design*, 1st ed. New York, NY, USA: Wiley, 2000.

[2] N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[3] C. Kushwah and S. K. Vishvakarma, "Ultra-low power sub-threshold SRAM cell design to improve read static noise margin," in *Progress in VLSI Design and Test* (Lecture Notes in Computer Science), vol. 7373. Berlin, Germany: Springer-Verlag, 2012, pp. 139–146.

[4] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 680–688, Mar. 2007.

[5] C. B. Kushwah, D. Dwivedi, and N. Sathisha, "8T based SRAM cell and related method," U.S. Patent IN920 130 218 US1, May 30, 2013.

[6] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[7] C.-H. Lo and S.-Y. Huang, "P-P-N based 10T SRAM cell for low-leakage and resilient subthreshold operation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 695–704, Mar. 2011.

[8] I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches," in *Proc. 30th Eur. Solid-State Circuits Conf.*, Sep. 2004, pp. 215–218.

[9] B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "A variation-tolerant sub-200 mV 6-T subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2338–2348, Oct. 2008.

[10] S. A. Tawfik and V. Kursun, "Low power and robust 7T dual-Vt SRAM circuit," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2008, pp. 1452–1455.

[11] M.-H. Tu, J.-Y. Lin, M.-C. Tsai, S. J. Jou, and C.-T. Chuang, "Single-ended subthreshold SRAM with asymmetrical write/read-assist," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3039–3047, Dec. 2010.

[12] M.-H. Tu *et al.*, "A single-ended disturb-free 9T subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1469–1482, Jun. 2012.

[13] K. Takeda *et al.*, "A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 113–121, Jan. 2006.

[14] C. B. Kushwah, S. K. Vishvakarma, and D. Dwivedi, "Single-ended sub-threshold FinFET 7T SRAM cell without boosted supply," in *Proc. IEEE Int. Conf. IC Design Technol. (ICICDT)*, May 2014, pp. 1–4.

[15] C. B. Kushwah and S. K. Vishvakarma, "A sub-threshold eight transistor (8T) SRAM cell design for stability improvement," in *Proc. IEEE Int. Conf. IC Design Technol. (ICICDT)*, May 2014, pp. 1–4.

[16] M.-F. Chang, S.-W. Chang, P.-W. Chou, and W.-C. Wu, "A 130 mV SRAM with expanded write and read margins for subthreshold applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 520–529, Feb. 2011.