A Bridge Modular Switched-Capacitor-Based Multilevel Inverter With Optimized SPWM Control Method And Enhanced Power-Decoupling Ability

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***Abstract*- Micro-inverters operating into the single-phase grid from new energy source with low-voltage output face the challenges of efficiency bottleneck and twice-line-frequency variation. This paper proposed a multilevel inverter based on bridge modular switched-capacitor (BMSC) circuits with its superiority in conversion efficiency and power density. The topology is composed of DC-DC and DC-AC stages with independent control for each stage, aiming to improve system stability and simplify the control method. The BMSC DC-DC stage, which can be expanded to synthesize more levels, not only features multilevel voltage gain but also partially replaces the original bulk input capacitor and functions as an active energy buffer to enhance power decoupling ability between DC and AC sides. In DC-AC stage, the control strategy of optimized unipolar frequency doubling sine-wave pulse-width modulation (UFD-SPWM) is proposed to improve the quality of output waveform. Meanwhile, the multilevel voltage phase has been optimized to reduce the power loss further. Finally, a prototype has been built and tested. Associated with the simulation, the experimental results validate the practicability of these analyses.**

***Index Terms*- Switched-capacitor circuit, multilevel inverter, power decoupling, optimized unipolar frequency doubling SPWM.**

I. INTRODUCTION

In renewable energy generation system (REGS), the low voltage generated by the PV or fuel cells should be boosted to a relatively high-standard DC bus voltage before making it to AC bus for grid-connection [1]-[3]. A thermoelectric generator, a battery, and an ultra-capacitor are typical examples of such low-voltage DC energy sources as well. Review article [4] presented some good insight on the converter topology for small distributed generation (DG) inverters. Recently, numerous converter topologies for the power conversion from low-voltage DC to high-voltage AC for grid-connection have been reported to deal with specific issues such as efficiency, cost, safety and harmonic. Generally speaking, there are two kinds of topology schemes for REGS, including single-stage and cascade-stage. It is possible to combine a DC-DC boost conversion and DC-AC conversion in one stage to realize voltage lift and inversion [5]-[6]. Even that relative less components are required, it is difficult to obtain high voltage gain. Another typical approach requires a boost converter as the front-end stage and an inverter as the back-end stage for the grid-connection. Due to independent control for each stage, high output waveform quality could be relatively easy to obtain. Meanwhile, it is suitable for wide range input voltage because of high gain realization [7]-[8].

Currently, various boost circuits in the front-end of cascade-stage REGS have been widely researched. To avoid conventional boost converter drawbacks under high gain, like extreme duty cycle, high voltage/current stress and heavy recovery loss, z-source, coupled-inductor or switched-capacitor net-work are introduced into boost circuits to finish DC-DC conversion [9] [10]. Especially for switched-capacitor converter, they have became a hot candidate due to magnetic-less components, high efficiency and power density [11]-[12]. Also, switched-capacitor converter could be extended voltage gain through increasing switched-capacitor modular [12]-[14]. However, employment of large switches and bottleneck of wave quality bring about cascade-stage REGS some upsetting.

With the development of multilevel technology, multilevel structure applied in the front-end of inverter has been proposed [15] [16]. In [17], three-level boost circuit is in the front end to boost the bus voltage and diode-clamped five-level inverter locates in the back end. To balance the voltage of series capacitors, two additional balancing circuits are employed, which make the system costly and bulkily. In [18], switched-capacitor modular with four switches and one capacitor is placed in the front of high-frequency-link DC-AC converter to output three voltage levels, but it requires auxiliary circuit to control the capacitor voltage with less than twice voltage gain. In literatures [19][20], two-stage seven-level inverter is proposed, where a switched-capacitor multilevel circuit could output four voltage levels: 0, V_{in}, $2V_{in}$ and $3V_{in}$. It owns advantages in term of switches number and voltage stress compared with conventional multilevel converter, but a complex control strategy is required to balance the capacitor voltage during voltage level transition. Compared with converter in [19][20], converters presented in [21][22] have flexible voltage level extension and voltage gain could be boost further with the switched-capacitor module increasing, the deficiency lies in more components requirement under the same voltage level output.

One of the challenges faced by cascade stage micro-inverter is the need to buffer the twice-line-frequency energy. A number of power decoupling techniques have been employed

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to handle the twice-line-frequency energy concern. Basically, it could be identified three types of power decoupling technique: PV-side decoupling, DC-link decoupling and AC-side decoupling. For PV-side decoupling technique, posing the decoupling capacitor directly across on the PV output terminal would be the best choice from an efficiency aspect. However, the required capacitance will be quite large, which inevitably increases the cost, reduces the power density and shortens the lifetime [23] [24]. As for DC link decoupling technique, generally, the cost is low because no additional circuit is required, leading to relatively high efficiency as well. However, sophisticated control strategy should be employed to allow for higher voltage ripple and to maintain the low current THD injected to the grid [25]. In AC-side decoupling technique, the capacitance can be very small due to the high voltage swing. However, another phase leg is added, which is bound to increase the cost [26] [27].

There are several modulation methods to drive a multilevel inverter: the space vector modulation (SVPWM) [28][29], the selective harmonic elimination (SHEPWM)[30] [31], and the multicarrier SPWM, such as the alternatively phase opposition disposition(APOD)PWM[30][32]. In SHEPWM, the objective is elimination of low-order harmonic, while the fundamental harmonic should be satisfied. If this goal cannot be obtained, the highest possible harmonic optimization is desired. Solving SHEPWM non-liner equations is a major problem in obtaining switching angles. In SVPWM, relative high voltage utilization and low output current ripple could be obtained, but is just suitable for three-phase inverter with low levels output. In APODPWM, it puts more harmonic energy into triple sideband harmonic that cancels on a line-to-line basis. However, the remaining harmonic becomes larger and it has triple sideband harmonic cancelling only in three-phase inverter.

This paper introduces a new conversion technique to address the afore-mentioned challenges. The new technique shares switched-capacitor conversion technology and control strategy of optimized unipolar frequency doubling SPWM (UFD-SPWM), while it enables very high efficiency and low output voltage THD. The proposed converter architecture incorporates a bridge modular switched-capacitor (BMSC) with multilevel gain and H-bridge to achieve compression of the high efficiency multilevel inverter operation range, thereby improving the efficiency of H-bridge converter stage. The BMSC circuit also partially replaces the original bulk input capacitor and provides the twice-line-frequency energy buffering between DC and AC sides.

The reminder of this paper is organized as follows. The proposed converter and operation principle is described in Section II. The optimal design of phase parameters and power decoupling analysis are presented in Section III. Section IV gives the simulation and experimental results and comparison with reported converters. Finally, conclusions are listed in Section V.

II. The Proposed Converter And Operation Principle

A. Topology Description

The general topology of bridge modular switched-capacitor-based multilevel inverter is shown in Fig.1(a). The proposed converter includes switched-capacitor module, as shown in left and middle dashed frames, and H-bridge module, as shown in the right dashed frame. It will increase 4 levels for output voltage with each switched-capacitor modular added. DC-DC step-up conversion is finished in the switched-capacitor module, the first topology description of which is reported in [33]. DC-AC conversion is realized based on H-bridge. Two conversion stages are independent operation with decoupling control. In the paper, a seven-level inverter with one switched-capacitor modular, as shown in Fig.1(b), is implemented for analysis and verification.

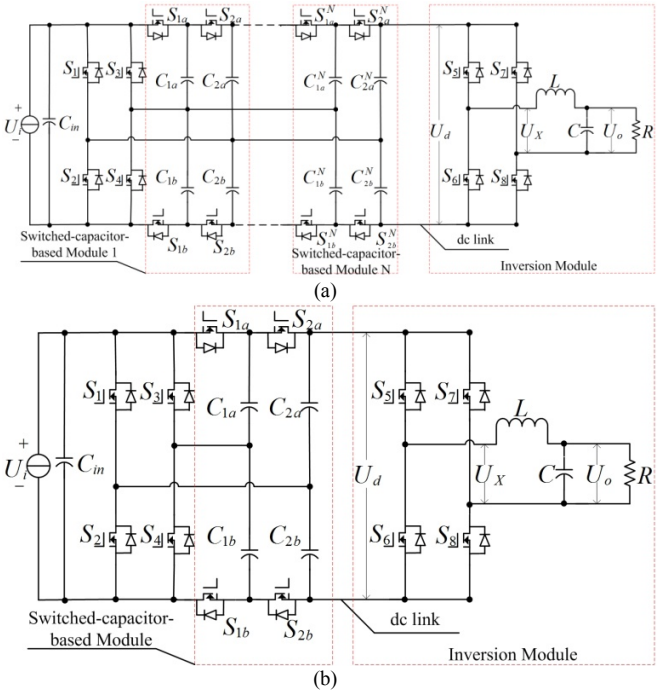

Fig.1 Topology of the proposed converter.(a) General topology of bridge modular switched-capacitor-based multilevel inverter.(b) Seven-level inverter.

B. Operation of Switched-Capacitor Module

The control strategy of switched-capacitor modular is plotted in Fig.2, where three voltage levels (U_i, $2U_i$, $4U_i$) could be outputted for DC link voltage U_d.

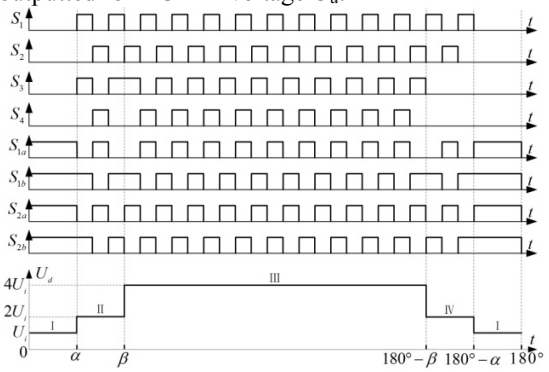

Fig. 2 Control strategy of switched-capacitor modular.

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In consideration of symmetry in a line period, the modes analysis is only based on positive half period ($\theta \in [0,180°)$). The operation states are shown in Fig.3. **Mode I ($\theta \in [0,\alpha) \cup [180°-\alpha,180°)$):** as shown in Fig.3(a), switches S_{1a}, S_{1b}, S_{2a} and S_{2b} are turned on and S_1, S_2, S_3 and S_4 are turned off. Each capacitor suffers $0.5U_i$ and U_i is outputted for U_d. **Mode II ($\theta \in [\alpha,\beta)$):** as shown in Fig.3(b) and Fig.3(c), there will be two sub-circuits, each capacitor suffers U_i and $2U_i$ will be outputted for U_d. **Mode III ($\theta \in [\beta,180°-\beta)$):** there are also two sub-circuits as shown in Fig3(d) and Fig.3(e), respectively. C_{2a} or C_{2b} will be charged into $2U_i$ thus U_d could reach up to $4U_i$. **Mode IV ($\theta \in [180°-\beta,180°-\alpha)$):** being similar to Mode II, $2U_i$ is obtained for U_d in the two sub-circuits. In this mode, the energy stored in C_{2a} or C_{2b} will flows back to source to obtain U_i across C_{2a} or C_{2b}.

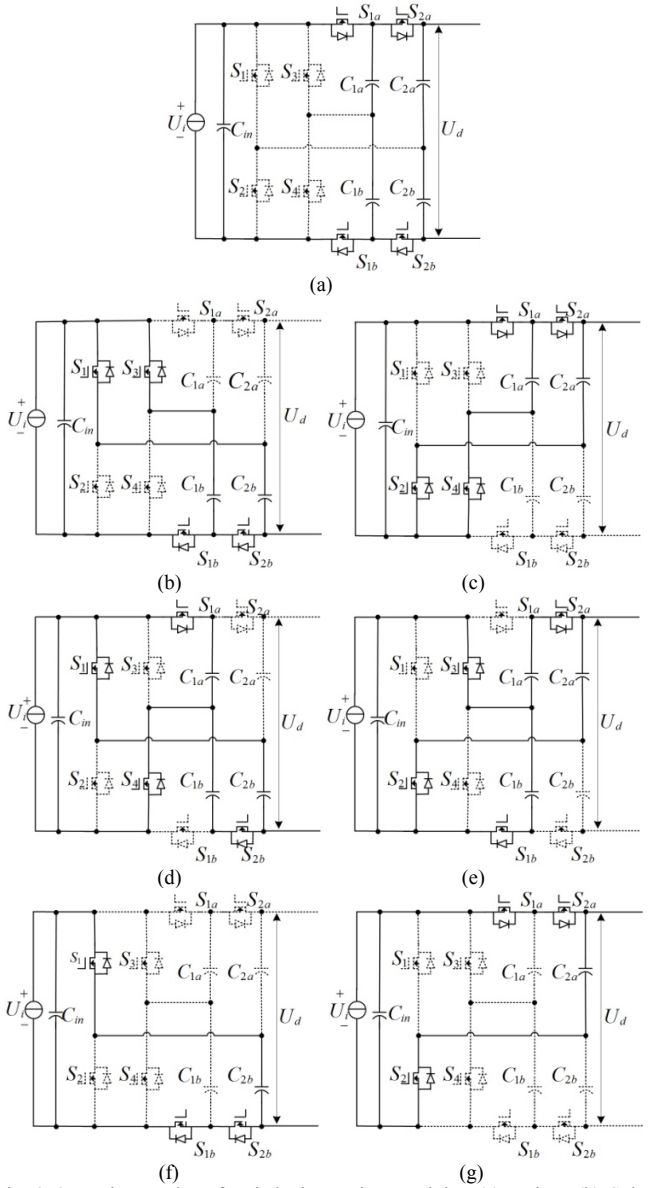

Fig. 3 Operation modes of switched-capacitor modular. (a)Mode I. (b) Sub-circuit 1 in Mode II. (c) Sub-circuit 2 in Mode II. (d) Sub-circuit 1 in Mode III. (e) Sub-circuit 2 in Mode III. (f) Sub-circuit 1 in Mode IV. (g) Sub-circuit 2 in Mode IV.

C. *Operation of inversion module with optimal control*

Considering the independent control for inversion stage and voltage multilevel on DC-link, SPWM with only one carrier, which requires simple calculation, is the best candidate for modulation method. Compared with other SPWM methods, unipolar frequency doubling SPWM (UFD-SPWM) exhibits strong harmonic suppression and doubles equivalent switching frequency without increasing switching loss. To maximize fundamental component in the step wave, the control method of UFD-SPWM with level phase optimization is employed for inversion modular, as shown in Fig.4. The bi-triangle carrier wave u_c with three different voltage levels ($1/4U_c$, $1/2U_c$, U_c) compares to the modulated sine wave u_g with two opposite polarities (u_g and $-u_g$) to produce driving signals for switches S_5~S_8.

To make sure minimized switching loss and achieve better power factor, DC link current I_d should approach zero at zero crossing of the line voltage (when $\theta = 0$ and $\theta = 180°$). However, due to practical continuous operation for switched-capacitor module, it is difficult to keep I_d=0. Hence, a dead-angle δ of several degree is required to set before or after the zero-crossings of the line frequency. At $N = 0,1,2,...$, suppose $\theta = [N \cdot 180° - \delta, N \cdot 180° + \delta]$, all the switches S_5, S_6, S_7 and S_8 are turned off.

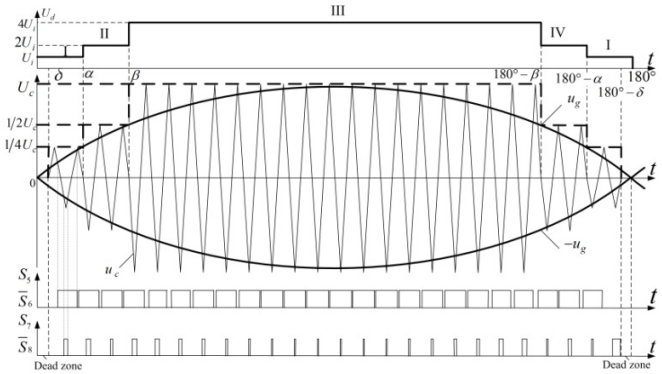

Fig. 4 The waveforms of optimized UFD-SPWM control method.

As shown in Table I, the detailed operation of switches S_5~S_8 in inversion modular is described. Different with conventional unipolar frequency doubling SPWM, the carrier wave u_c in proposed UFD-SPWM has three levels during different phase intervals of modulation wave u_g, whose phase optimization will be discussed in next section. When u_c<u_g, driving signals for S_5 and S_6 are high level and low level, respectively, and contrarily at u_c>u_g. When u_c<-u_g, driving signals for S_7 and S_8 are high level and low level, respectively, and on the contrary when u_c>u_g. At positive half cycle, U_X is determined by driving signals logic of switches S_5 and S_8. Deserve to be mentioned, switches S_6 and S_7 will never be turned-on simultaneously because the high level for driving signal of S_5 is always longer than the low level for driving signal of S_7. At each mode, it will output two levels alternately: (0, U_i) for mode I, (0, $2U_i$) for modes II and IV, (0, $4U_i$) for modes III. Hence, positive voltage levels (U_i, $2U_i$, $4U_i$) and zero level are outputted for U_X during positive half cycle.

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Analogously, U_X has negative voltage levels (-U_i, -2U_i, -4U_i) and zero level during negative half cycle. Because there are two levels switching alternately for output voltage during each switching period, the frequency of output levels doubles the switching frequency. Under the modulation method, the output waveforms at filter front-end and back-end are shown in Fig.5.

Based on mentioned analysis, it could be concluded that, under the proposed control method, not only switching loss could be reduced but also the output voltage harmonic will be cut down due to the increasing voltage levels and doubling equivalent switching frequency.

TABLE I
SWITCHES OPERATION UNDER OPTIMIZED UFD-SPWM METHOD

		S_5	S_6	S_7	S_8	U_X
Positive half cycle						
$u_c>u_g$		OFF	ON	OFF	ON	0
1/4U_c≥u_c≥-1/4U_c 1/2U_c≥u_c≥-1/2U_c U_c≥u_c≥-U_c	u_g≥u_c≥-u_g	ON	OFF	OFF	ON	U_i 2U_i 4U_i
$u_c<u_g$		ON	OFF	ON	OFF	0
Negative half cycle						
$u_c>u_g$		ON	OFF	ON	OFF	0
1/4U_c≥u_c≥-1/4U_c 1/2U_c≥u_c≥-1/2U_c U_c≥u_c≥-U_c	-u_g≥u_c≥u_g	OFF	ON	ON	OFF	-U_i -2U_i -4U_i
$u_c<u_g$		OFF	ON	OFF	ON	0

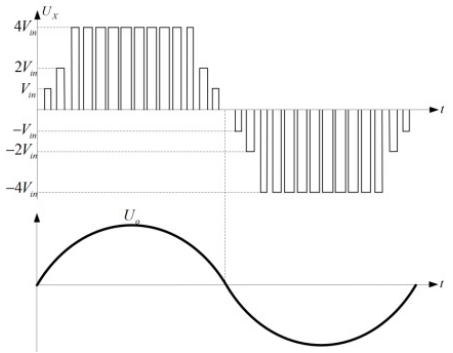

Fig. 5 Output waveform of inversion module.

III. Optimal Design Of Phase Parameters And Decoupling Analysis

A. Optimal Design of Phase Parameters

To minimize the voltage conversion range of inversion and reduce the power loss, U_d should be stepped with the line voltage as shown in Fig.6. Considering maximum value of $4U_i$ for output voltage U_o, it is assumed that $U_o = 4U_i \cdot \sin\theta$. Meanwhile, $U_{X,evp}$ is assumed as the envelop of high frequency output voltage pulse U_X, which is equivalent to U_d. As known from Fig.6, by making $U_o = U_{X,env}$ at $\theta=\alpha$, $\theta=\beta$, the difference between $U_{X,evp}$ and U_o can reach minimization value, It yields:

$$U_o(\alpha) = 4U_i \cdot \sin\alpha = U_i \tag{1}$$

$$U_o(\beta) = 4U_i \cdot \sin\beta = 2U_i \tag{2}$$

The normalized difference between $U_{X,env}$ and U_o, which should be minimized, could be quantified as $\left(U_{X,env}-U_o\right)/U_o$. As shown in Fig.6, it is easy to found that the maximum of this normalized difference only occurs at one of the following line angles: $\theta=\delta$, $\theta=\alpha$, $\theta=\beta$. Hence, the optimization target k to be minimized can be expressed as:

$$k = \max\left[\frac{U_i - 4U_i\cdot\sin\delta}{4U_i\cdot\sin\delta}, \frac{2U_i - 4U_i\cdot\sin\alpha}{4U_i\cdot\sin\alpha}, \frac{4U_i - 4U_i\cdot\sin\beta}{4U_i\cdot\sin\beta}\right] \tag{3}$$

Submit formulas (1) and (2) to formula (3), it yields:

$$k = \max\left[\frac{U_i - 4U_i\cdot\sin\delta}{4U_i\cdot\sin\delta}, 1, 1\right] \tag{4}$$

From formula (4), it can be concluded that when $\frac{U_i - 4U_i\cdot\sin\delta}{4U_i\cdot\sin\delta}=1$, the voltage difference comes to the minimum value. And the results can be calculated out:

$$\begin{cases}\delta = 7.181^\circ\\ \alpha = 14.478^\circ\\ \beta = 30^\circ\end{cases} \tag{5}$$

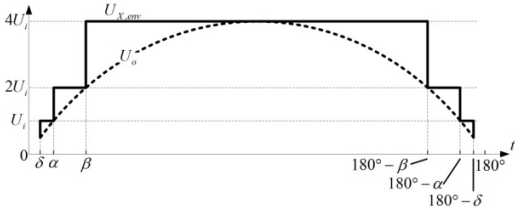

Fig. 6 Output Waveforms of inverter module with dead zone.

B. Power Decoupling Analysis

In a gird-connected single-inverter, the injected current to the grid $i_o(t)$ and the grid voltage $u_o(t)$ are given by

$$\begin{cases}u_o(t) = U_o\sin(\omega_o t)\\ i_o(t) = I_o\sin(\omega_o t+\varphi)\end{cases} \tag{6}$$

Where, ω_o is the grid frequency, U_o and I_o are the amplitudes of the grid voltage and current, respectively. φ is phase shift between the injected current and the grid voltage, which is desirable to be zero for unity power factor. When phase shift φ is zero, the instantaneous output power $P_o(t)$ is yielded as follows:

$$P_o(t) = \frac{1}{2}U_oI_o + \frac{1}{2}U_oI_o\cos(2\omega_o t) \tag{7}$$

The output instantaneous power in (7) consists of two terms: the average output power 1/2U_oI_o, and the pulsating power 1/2U_oI_o·cos(2$\omega_o t$), which oscillates at twice the line frequency. However, the power from the DG source (like PV modular, thermoelectric modular etc.) should be controlled to be constant as possible for maximum power point track (MPPT). Assuming a lossless inverter stage, the power generated by the DG modular equals to the average output power, as show in Fig.7. To maintain power balance, the pulsating power, P_{oac}=P_o-P_i, usually is handled by "decoupling capacitor".

It is assumed that the converter is power lossless, according to energy conservation law, the energy stored in the equivalent DC link capacitor C_d can be expressed as a function of capacitor voltage U_{Cd} at any given time with a sinusoidal shape superimposed on a DC offset. According to the energy balance principle, the energy charged or discharged from the capacitor C_d can be calculated by integrating one of shadowed as shown in Fig.7. Based on optimal design of phase parameters in Section A, modes I, II, IV and partial III will go through storing energy process and the rest mode III goes through delivering energy process.

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$$E_{Cd}=\int_0^{\frac{\pi}{2\omega_O}}\left(P_i-P_o(t)\right)dt=\frac{1}{2}C_d\left(U_{Cd\_\max}-U_{Cd\_\min}\right) \quad (8)$$

Where, $U_{Cd\_\max}$ and $U_{Cd\_\min}$ are the maximum and minimum voltage across the decoupling capacitor. The integration interval [0 π /2 ω o] suggests half power oscillation period for delivered energy or stored energy, the voltage across C_d will reach up to maximum value from minimum value or reach down to minimum value from maximum value.

Combing formulas (7) and (8), the required decoupling capacitance can be given as:

$$C=\frac{P_i}{\omega_O U_{Cd}\Delta U_{Cd}} \quad (9)$$

Where, U_{Cd} is the average DC voltage across C_d, and ΔU_{Cd} is the voltage ripple across C_d.

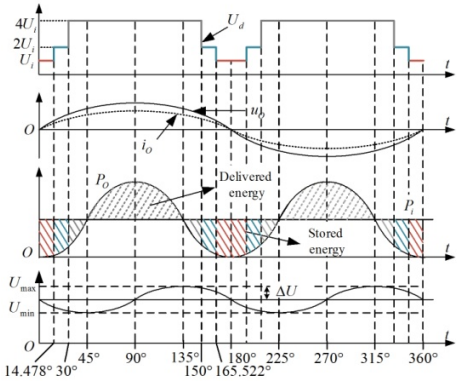

Fig.7 Total power processed by the decoupling capacitor.

In the proposed converter, the low-frequency power pulsation is converted into the voltage pulsation on DC link equivalent capacitor C_d, which serves as partial decoupling capacitor and can be calculated out according to Fig.3, such that the voltage across the input capacitor C_{in} is kept constant as possible and its capacitance can be reduced to a relatively smaller value. It is assumed that capacitors C_{1a} ~ C_{2a} have the same capacitance C, the equivalent decoupling capacitor at different operation modes for switched-capacitor module is shown in Fig.8.

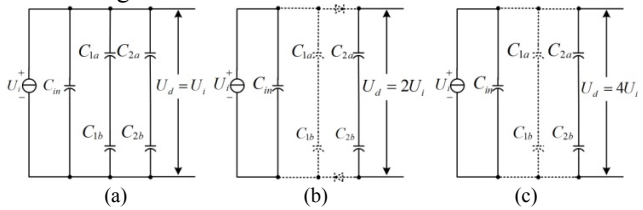

Fig.8 Equivalent decoupling capacitor: (a) C_{dec}= C_{in}+C. (b) C_{dec}= 0.5C. (c) C_{dec}= 0.5C.

When U_d=U_i, the DC link equivalent capacitor C_d can be seen as capacitors C_1 and C_2 connected in parallel, and C_d=C. Hence, at this state, the decoupling capacitor C_{dec} is equal to C_{in}+C, as shown in Fig. 8(a). In Fig. 8(b), the charging current is blocked by the reverse diodes of S_{2a} and S_{2b}, thus C_d is equivalent to C_{2a} and C_{2b} connected in series, and C_d= C_{dec}=0.5C. When U_d=4U_i, C_d is equivalent to C_{2a} and C_{2b} connected in series, and C_{dec}= 0.5C as well.

Considering different phases at different modes, as shown in Fig.7, the DC link capacitor will absorb power from input side when U_d steps into 2U_i from U_i, but absorb power from inversion side when U_d steps into 2U_i from 4U_i. Therefore, if a path is provided at the moment when the power flows back, the power decoupling ability will be promoted. Based-on the idea of increasing equivalent DC link capacitance, a improved control strategy is proposed, as shown in Fig.9. Accordingly, the modes II and IV are improved as Fig.10(a), Fig.10(b), Fig.10(c) and Fig.10(d), respectively. Under the improved control strategy, switches S_{2a} and S_{2b} are kept on when U_d=2U_i. With the improved control strategy, switching losses is partly reduced, and capacitance value of C_d will increase due to two capacitors bridges (bridge 1 with C_{1a}, C_{1a} and bridge 2 with C_{2a}, C_{2b}) connected in parallel. Thus, C_{dec}=C, as shown in Fig. 10(e).

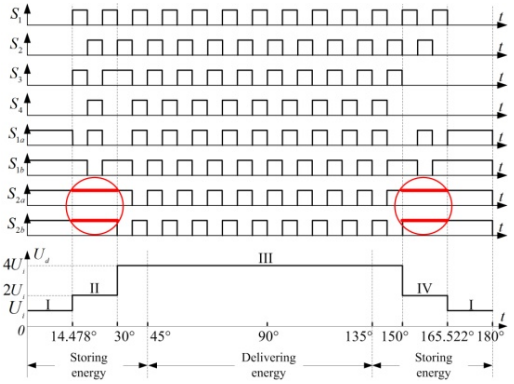

Fig. 9 Improved control strategy of the proposed converter.

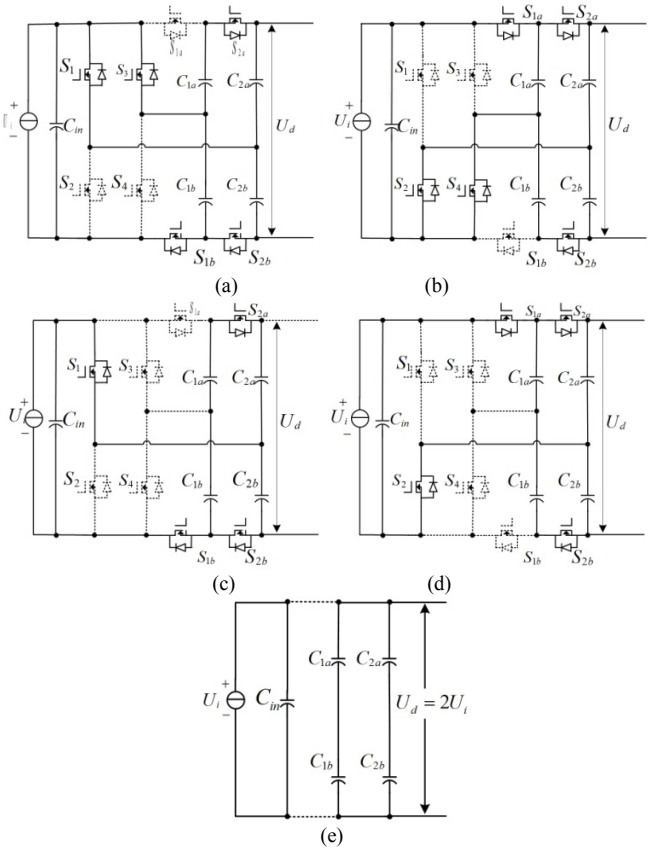

Fig. 10 Operation modes under improved control: (a) Sub-circuit 1 at Mode II. (b) Sub-circuit 2 at Mode II. (c) Sub-circuit 1 at Mode IV. (d) Sub-circuit 2 at Mode IV. (e) Equivalent decoupling capacitor: C_{dec}= C, when U_d=2U_i.

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The discussion of power decoupling operation results in the following effects:

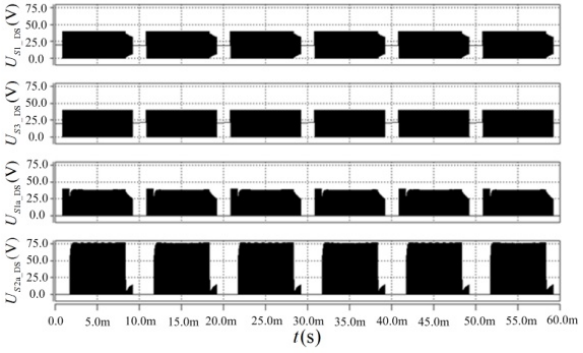
1. For a micro-inverter with a given power rating and line frequency, the size of the required decoupling capacitance is determined by the DC voltage and maximum allowable voltage ripple. As the capacitor voltage U_{Cd} is much higher than the input voltage U_i, energy transferring would occur when the voltage fluctuation on C_d is increased.

2. The DC input energy is stored in equivalent DC link capacitor C_d and the output energy is supplied from the same capacitor. Consequently, the low-frequency power pulsation caused by the inversion modular is transferred into capacitor C_d, and the voltage on input capacitor C_{in}, which is same as that of DG module, is kept constant.

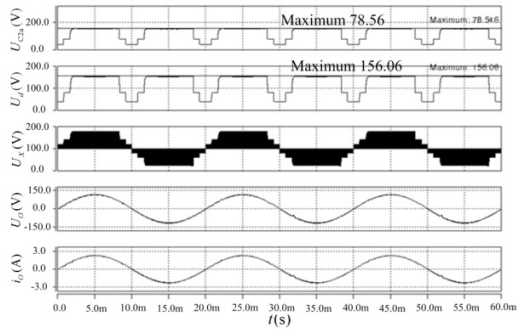
Therefore, capacitance value of C_{in} can be minimized without increasing the ripple voltage on DC input and a large electrolytic capacitor can be substituted with a film capacitor.

IV. Simulation And Experimental Results

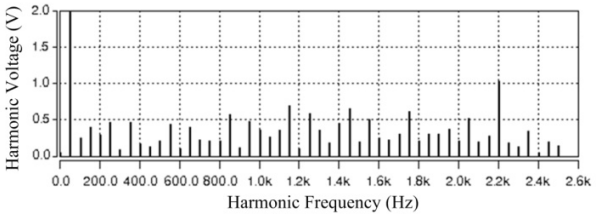
The simulation parameters are as follows: input voltage U_i=40V, switching frequency f_s=15kHz for DC-AC conversion modular and f_s=50kHz for DC-DC conversion modular, line frequency capacitors f_l=50Hz, C_{1a}=C_{1b}=C_{2a}=C_{2b}=40μF, modulation index M=0.8, output load R_o=50Ω, filter inductor L_f=2.5mH, filter capacitor C_f=3.3μF. It is noticed that switching frequency f_s will increase to 50KHz during mode transition to overcome the current spike. Meanwhile, due to resistance distributed in wire, ON-switches, capacitor and the distribute/stray inductance, the current spike will be limited in some extent. The typical simulation results are shown in Fig.11. The voltage stress of switches U_{S1_DS}, U_{S3_DS}, U_{S1a_DS} and U_{S2a_DS} are shown in Fig.11(a), it is easy to conclude that the voltage stress of switches S_1-S_4, S_{1a} and S_{1b} equals to U_i, and the voltage stress of switches S_{2a} and S_{2b} equals to $2U_i$. The voltages across capacitor C_{2a} and the output of switched-capacitor module are shown in Fig.11(b), where the three voltage levels (U_i, $2U_i$, $4U_i$) are obtained for U_d. Also, the output voltage of inversion module U_X, output voltage U_o and output current I_o of the inverter through the LC filter are shown in Fig.11(b). Finally, the spectrum of output voltage U_o with the total harmonic distortion (THD) of 3.43% is shown in Fig.11(c).



(a)



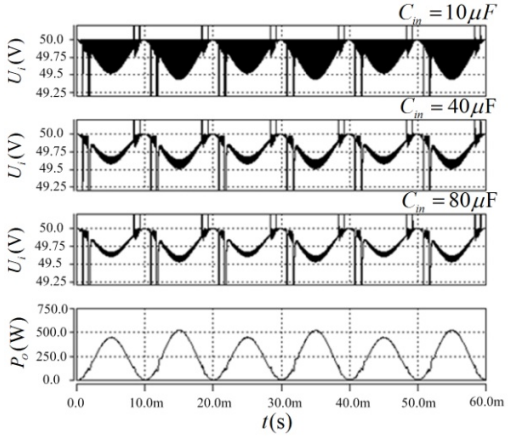
(b)



(c)

Fig.11 Simulation waveforms of seven-level inverter.(a) U_{s1_DS}, U_{s3_DS}, U_{s1a_DS} and U_{s2a_DS}. (b) U_{C2a}, U_d, U_X, U_o and i_o. (c) Spectrum of U_o.

To verify the enhanced performance of power decoupling for the proposed converter, a conventional control strategy based on the same prototype is employed to validate in simulation and experiment. Thus, it works with the same value for most parameters but input voltage rises up to 50V for a convincing verification. Under this strategy, switched-capacitor modular is operated as mode III to obtain 4 times voltage gain and conventional unipolar frequency doubling SPWM control strategy is employed for inversion modular. Fig.12(a) and Fig.12(b) show the input voltage U_i and the output voltage U_d of switched-capacitor module under proposed control strategy, respectively. For comparison, Fig.12(c) and Fig.12 (d) give out the input voltage U_i and the switched-capacitor output voltage U_d under conventional control strategy. Larger input capacitance value could enhance the power decoupling ability under proposed control strategy as well as conventional control strategy. However, it is obvious that the voltage ripple will be suppressed under the proposed control strategy compared with conventional control strategy.



(a)

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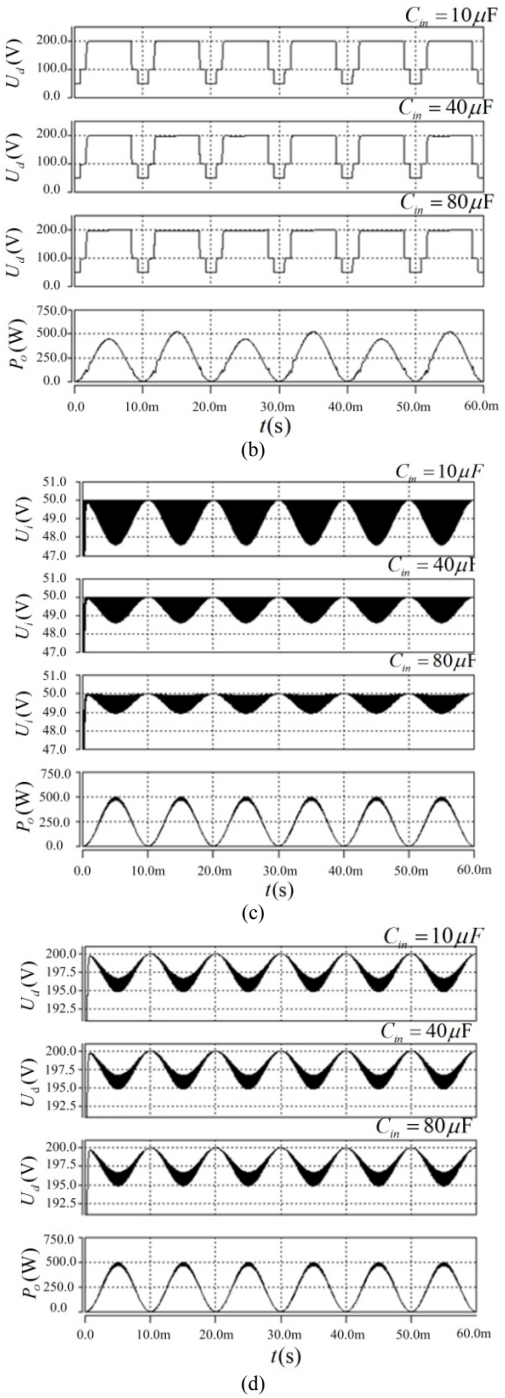


Fig.12 Simulation comparison of power decoupling ability at different C_{in}. Under proposed control strategy:(a)U_i and P_o. (b)U_d and P_o. Under conventional control strategy:(c) U_i and P_o. (d) U_d and P_o.

Same as the simulation parameters, a seven-level inverter prototype is built in Fig.13. IRFP260N and IXTK62N25 are employed for switches S_1-S_4, S_{1a}-S_{2b} and switches S_5-S_8, respectively. SHB-500-40 is utilized as capacitors. The experimental results under resistive load are shown in Fig.14. The voltage stress of the switches is shown in Fig.14(a), which agrees well with the theoretic analysis and the simulation results. And Fig.14(b) plots the voltage across capacitors C_{1a} and C_{2a}, the output voltage of switched-capacitor module U_d, the output voltage of inversion module U_X, and the inverter output voltage/current U_o/i_o. In Fig.14(b), U_{C1a} has two levels of 20V and 40V, and U_{C2a} owns three levels of 20V, 40V and 80V. The output voltage U_d doubles U_{C2a} with three levels of 40V, 80V and 160V, which is in accord with the theoretic analysis results. U_X, at the filter front-end, obtains seven voltage levels of ±160V, ±80V, ±40V and 0V through inversion operation. The spectrums of output voltage at filter front-end U_X and back-end U_o are shown in Fig.14(c) and Fig.14(d), respectively. The THD of U_X amounts to 11.207% and U_o is about 3.865% after LC filtering. Given LC parameter optimization, the lower THD could be achieved across U_o.

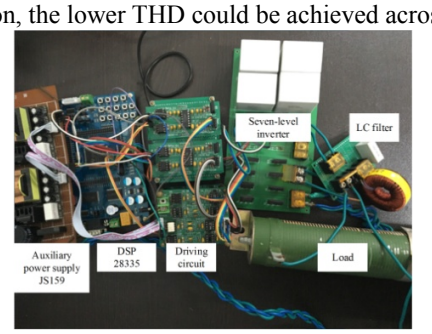
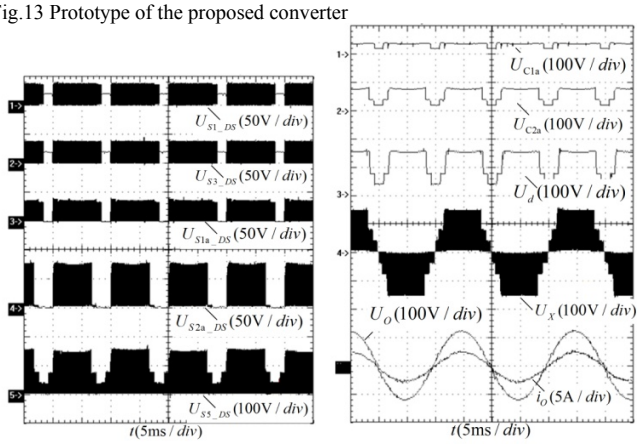


Fig.13 Prototype of the proposed converter



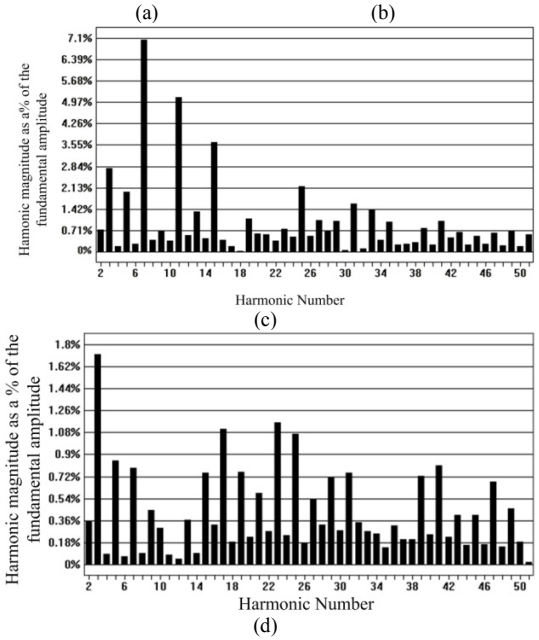


Fig.14 Experiment results under R-load.(a) U_{s1_DS} , U_{s3_DS}, U_{S1a_DS}, U_{s2a_DS} and U_{s5_DS}.(b) U_{C1a}, U_{C2a}, U_d, U_X, U_o and i_O. (c)Spectrum of U_X. (d) Spectrum of U_o.

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The experimental waveforms under RL-load with resistor of 50Ω and inductor of 20mH is shown in Fig.15. It is seen that the THD of output voltage is about 3.614%, approaching to the THD under R-load. Hence, the proposed inverter could work normally at RL-load, which makes it potential in stand-alone or grid-connected applications.

The experimental waveforms of U_i, U_d and U_o with different C_{in} to validate power decoupling ability are shown in Fig.16. It is noticed that the input voltage is increased to 50V from 40V. The results suggest that the voltage ripple across input source will be significantly reduced with C_{in} of 10μF as well as 40μF when the proposed converter is operated under proposed control strategy. Hence, the conclusion that proposed converter is qualified with enhanced power decoupling ability could be derived.

Keeping parameters the same as simulation, the converter works with changing load R (163Ω to 25Ω) to obtain different output power level (50W to 310W) under open loop control. The efficiency curve is measured based on Power Analyzer PA310, as plotted in Fig.17. It shows high efficiency of more than 92% at full-load range and peak efficiency goes up to 97.6% for the proposed converter.

The comprehensive comparison with other reported topologies has been made and shown in Table II, where N is an odd number representing output voltage levels.

All the converters reported in [19][20][21] and proposed converter have two power conversion stages: switched-capacitor boost converter for DC-DC and H-bridge inverter for DC-AC. Converters in [19] and [20] share the same topology with different modulation methods. Being superior to the converters in [19][20][21], the proposed converter owns merit in reducing twice-line-frequency variations. Compared with converters in [19][20], the proposed converter extends its output levels conveniently by increasing switched-capacitor modular. Meanwhile, it features higher efficiency even at lower switching frequency of 15KHz (inversion modular), lower THD of output voltage at filter front-end and higher voltage gain under the same output levels. Actually, the THD of output voltage at filter back-end could be reduced further through optimization of filter design parameters, which will be discussed in future work. In [21], even that the converter could extend its output levels as the proposed converter as well, its current path goes through more power device resulting in more switching and conduction loss, which has been validated by the index of peak efficiency under the same power rating of 300W. Higher voltage gain at same output levels is another important advantage for the proposed converter as well compared to the converter in [21]. In terms of modulation method, UFD-SPWM exhibits merit of only one carrier requirement, which reduces the control complexity. Most importantly, different with the reported converters, the proposed converter could be controlled independently for two cascading parts, bringing about higher stability and reliability. However, the proposed converter should employ a few more active switches under occasion of low output levels. When N goes up to 11, the utilization number of active switches in proposed converter is still more than converter in [21] but less than converter in [19][20]. Actually, if considering diode requirement, converter in [21] takes up the most device among the compared converters.

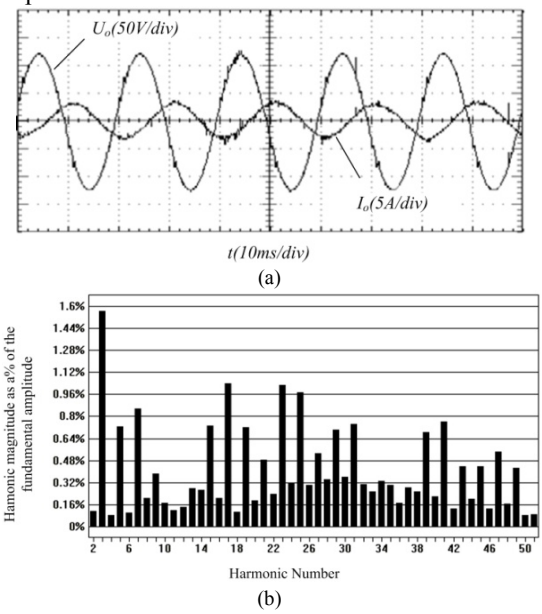

Fig.15 Experiment waveforms under R-L load: R_o=50Ω, L_o=20mH.(a) U_o and i_O.(b) Spectrum of U_o.

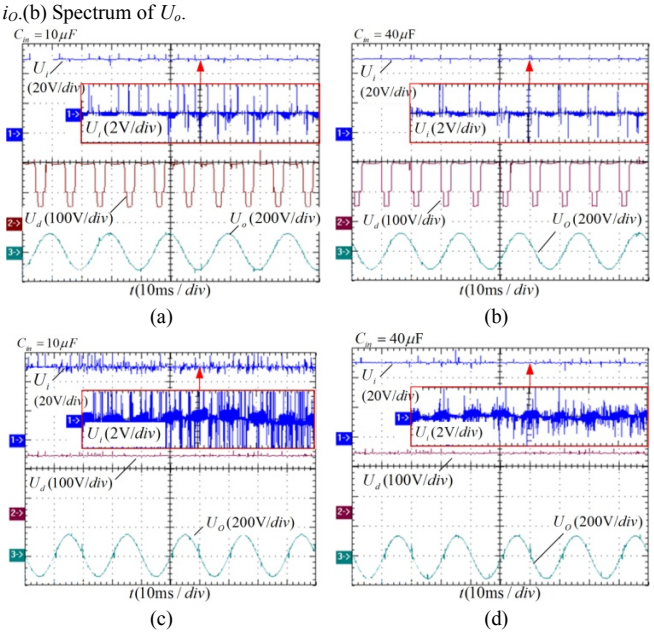

Fig.16 Experiment waveforms of U_i, U_d and U_o with different C_{in}. Under proposed control strategy:(a) with C_{in} of 10μF. (b) with C_{in} of 40μF. Under compared control strategy:(c) with C_{in} of 10μF. (d) with C_{in} of 40μF.

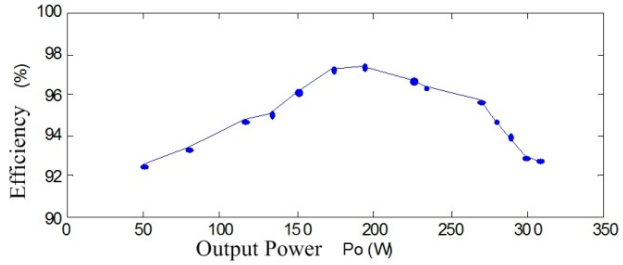

Fig.17 Measured efficiency curve.

TABLE II
COMPREHENSIVE COMPARISON BETWEEN THE PROPOSED CONVERTER AND REPORTED CONVERTERS

	[19]	[20]	[21]	Prototype
Topology	DC-DC-AC	DC-DC-AC	DC-DC-AC	DC-DC-AC
Modulation method	Multicarrier LS/LPS-SPWM	Multicarrier LS-SPWM	Multicarrier LS-SPWM/SHE	Optimized UFD-SPWM
Independent control	No	No	No	Yes
Rated power(W)	3.13/3.27	5.76	300	300
Input voltage(V)	8	8	36	20
Switching frequency(KHz)	40/20	40	40	15
Line frequency(KHz)	0.05	1	0.4	0.05
PK: peak efficiency	94.9%/95.4	84.9%	89.2%/91.6%	97.6%
Power factor	R-load	R-load	R-load	R-load
THD of output vol. at filter back-end	1.7%/1.4%	-	Without LC filter	3.865%
THD of output vol. at filter front-end	11.7%/5.13%	19.5%	-	11.2%
Twice-line-frequency variations reduction	-	-	-	Yes
Levels	7/N	7/N	11/7/N	7/N
Num. of device	10/0.5*(3N-1) switches 4/0.5*(N-1) Cap.	10/0.5*(3N-1) switches 4/0.5*(N-1) Cap.	9/7/0.5*(N+7)Switches 8 /4/(N-3)Diodes 4 /2/0.5*(N-3)capacitors	12/N+5 Switches 4 /N-3 Cap.
Vol. gain	3/0.5*(N-1)	3/0.5*(N-1)	5/3/0.5*(N-1)	4/N-3
Num. of carrier	6/N-1	6/N-1	10/6/N-1	1

V. Conclusion

A bridge modular switched-capacitor-based multilevel inverter with optimized UFD-SPWM control method is proposed in the paper. The switched-capacitor-based stage can obtain high conversion efficiency and multiple voltage levels. Meanwhile, it functions as an active energy buffer, enhancing the power decoupling ability and conducing to cut the total size of the twice-line energy buffering capacitance. Furthermore, voltage multi-level in DC-link reduces the switching loss of inversion stage because turn-off voltage stress of switches changes with phase of output voltage rather than always suffers from one relatively high DC voltage. Most importantly, the control method of UFD-SPWM, doubling equivalent witching frequency, is employed in the inversion stage for a high quality output waveform with reduced harmonic. In addition, the optimized voltage level phase maximizes the fundamental component in output voltage pulses to reduce harmonic backflow as possible. Hence, the comprehensive system efficiency has been promoted and up to peak value of 97.6%. Finally, two conversion stages are controlled independently for promoting reliability and decreasing complexity. In future work, detailed loss discussion, including theoretic calculation and validation of loss breakdown, will be presented.

Acknowledge

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