Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers

Omid Akbari, Mehdi Kamal, Ali Afzali-Kusha, and Massoud Pedram

***Abstract*— In this paper, we propose four 4:2 compressors, which have the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these dual-quality compressors provide higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors has its own level of accuracy in the approximate mode as well as different delays and power dissipations in the approximate and exact modes. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of these compressors in a 32-bit Dadda multiplier are evaluated in a 45-nm standard CMOS technology by comparing their parameters with those of the state-of-the-art approximate multipliers. The results of comparison indicate, on average, 46% and 68% lower delay and power consumption in the approximate mode. Also, the effectiveness of these compressors is assessed in some image processing applications.**

***Index Terms*— 4:2 compressor, accuracy, approximate computing, configurable, delay, power.**

I. Introduction

AMONG different arithmetic blocks, the multiplier is one of the main blocks, which is widely used in different applications especially signal processing applications [1]. There are two general architectures for the multipliers, which are sequential and parallel. While sequential architectures are low power, their latency is very large. On the other hand, parallel architectures (such as Wallace tree and Dadda) are fast while having high-power consumptions [2]. The parallel multipliers are used in high-performance applications where their large power consumptions may create hot-spot locations on the die [3]. Since the power consumption and speed are critical parameters in the design of digital circuits, the optimizations of these parameters for multipliers become critically important. Very often, the optimization of one parameter is performed considering a constraint for the other parameter. Specifically, achieving the desired performance (speed) considering the limited power budget of portable systems is challenging task. In addition, having a given level of reliability may be another obstacle in reaching the system target performance.

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To meet the power and speed specifications, a variety of methods at different design abstraction levels have been suggested. Approximate computing approaches are based on achieving the target specifications at the cost of reducing the computation accuracy [4]. The approach may be used for applications where there is not a unique answer and/or a set of answers near the accurate result can be considered acceptable [5]. These applications include multimedia processing, machine learning, signal processing, and other error resilient computations. Approximate arithmetic units are mainly based on the simplification of the arithmetic units circuits [6]. There are many prior works focusing on approximate multipliers (see [1], [10]–[17], [22]), which provide higher speeds and lower power consumptions at the cost of lower accuracies. Almost, all of the proposed approximate multipliers are based on having a fixed level of accuracy during the runtime. The runtime accuracy reconfigurability, however, is considered as a useful feature for providing different levels of quality of service during the system operation [4], [6]–[8]. Here, by reducing the quality (accuracy), the delay and/or power consumption of the unit may be reduced. In addition, some digital systems, such as general purpose processors, may be utilized for both approximate and exact computation modes [4]. An approach for achieving this feature is to use an approximate unit along with a corresponding correction unit. The correction unit, however, increases the delay, power, and area overhead of the circuit. Also, the error correction procedure may require more than one clock cycle (see [9]), which could, in turn, slow down the processing further.

In this paper, we present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked.

The rest of this paper is organized as follows. In Section II, some prior works on the approximate multipliers are reviewed. The internal structures of the proposed dual-quality 4:2 compressors (DQ4:2Cs) are explained in Section III. Section IV evaluates the accuracy of the Dadda utilizing the proposed compressors while the effectiveness of the proposed compressors is assessed in Section V. Finally, this paper is concluded in Section VI.

II. Related Work

While there are many works in designing approximate multipliers, the research efforts on accuracy configurable approximate multipliers are limited. In this section, we review some of these works. In [10], a static segment method (SSM) is presented, which performs the multiplication operation on an m-bit segment starting from the leading 1 bit of the input operands where m is equal to or greater than $n/2$. Hence, an $m \times m$ multiplier consumes much less energy than an $n \times n$ multiplier. Also, a dynamic range unbiased multiplier (DRUM) multiplier, which selects an m-bit segment, starting from the leading 1 bit of the input operands, and sets the least significant bit of the truncated values to "1," has been proposed in [11]. In this structure, the truncated values are multiplied and shifted to the left to generate the final output. Although, by exploiting smaller values for m, the structure of [11] provides higher accuracy designs than those of [10], its approach requires utilizing extra complex circuitry.

A bioinspired approximate multiplier, called broken array multiplier, has been proposed in [13]. In this structure, some carry save adder cells, in both vertical and horizontal directions during the summation of the partial products, have been omitted to save the power and area and reduce the delay. In [14], two approximate 4:2 compressors have been proposed and utilized in Dadda multiplier. The proposed compressors only operated in the approximate mode. In [1], by modifying the Karnaugh map of a 2×2 multiplier (omitting one term in the Karnaugh map), an approximate 2×2 multiplier with a simpler structure has been proposed. This block may be used for constructing larger multipliers. Also, in this paper, an error detection and correction (EDC) circuit has been proposed. An inaccurate multiplier design strategy based on redesigning the multiplier into two multiplication and nonmultiplication parts was introduced in [12]. The multiplication part was constructed based on the conventional multipliers while the nonmultiplication part was implemented in an approximate structure with a specified value of error. It should be noted that both of the approaches presented in [1] and [12] suffer from high relative errors.

In [15], a high accuracy approximate 4×4 Wallace tree multiplier was proposed. This multiplier employed a 4:2 approximate counter leading to delay and power reductions of the partial product stage of the 4×4 Wallace tree. In this paper, the proposed small multiplier was used to form larger multipliers. Due to the array structure of this approximate multiplier, its delay was large. In addition, an EDC unit was suggested to be used at the output of the approximate 4×4 Wallace tree. The unit generated the exact output in the case of the exact operating mode. In [16], by proposing an approximate adder with a small carry propagation delay, the partial product reduction stage was sped up. In this paper, an OR-gate-based error reduction unit was also proposed. In [17], a rounding-based approximate multiplier (ROBA) has been proposed that round the input operands into the nearest exponent of two. This way the multiplication operation became simpler. It should be noticed that the error recovery unit (those in [1], [12], [15], and [16]) increases the power consumption and delay of the multiplier. This implies that accuracy configurable multipliers would have large delay and power overheads. In this paper, we propose compressors, which have the ability of switching between the approximate and exact modes with very small delay and power overheads.

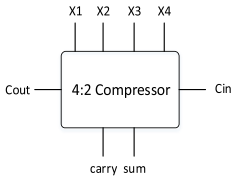

Fig. 1. Block diagram of 4:2 compressor.

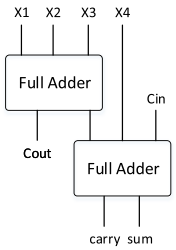

Fig. 2. Structure of the conventional 4:2 compressor.

III. Proposed 4:2 Compressors

In this section, first, the details of an exact compressor are discussed. Next, the overall structures and the details of the suggested dual-quality approximate compressors are described.

A. Exact 4:2 Compressor

To reduce the delay of the partial product summation stage of parallel multipliers, 4:2 and 5:2 compressors are widely employed [18]. Some compressor structures, which have been optimized for one or more design parameters (e.g., delay, area, or power consumption), have been proposed [18], [19]. The focus of this paper is on approximate 4:2 compressors. First, some background on the exact 4:2 compressor is presented. This type of compressor, shown schematically in Fig. 1, has four inputs (x_1–x_4) along with an input carry (C_{in}), and two outputs (*sum* and *carry*) along with an output C_{out}.

The internal structure of an exact 4:2 compressor is composed of two serially connected full adders, as shown in Fig. 2. In this structure, the weights of all the inputs and the s*um* output are the same whereas the weights of the *carry* and C_{out} outputs are one binary bit position higher. The outputs *sum*, *carry*, and C_{out} are obtained from

$$\text{sum} = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin \tag{1}$$

$$\text{carry} = (x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4 \tag{2}$$

$$\text{Cout} = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1. \tag{3}$$

B. Proposed Dual-Quality 4:2 Compressors

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the

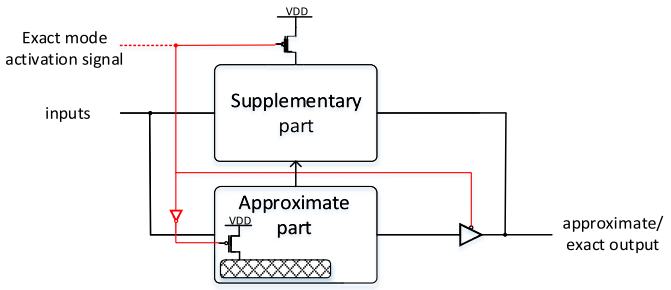

Fig. 3. Block diagram of the proposed approximate 4:2 compressors. The hachured box in the approximate part indicates the components, which are not shared between this and supplementary parts.

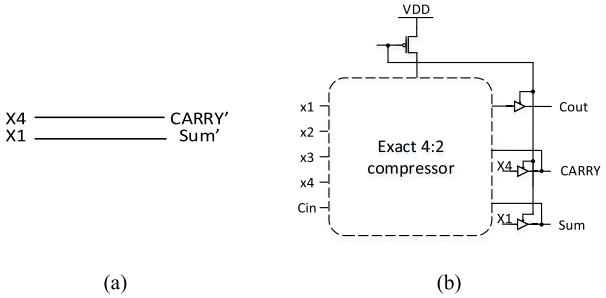

Fig. 4. (a) Approximate part and (b) overall structure of DQ4:2C$_1$.

compressors is shown in Fig. 3. The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized. In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, as is evident from Fig. 3, in the exact operating mode, tristate buffers are utilized to disconnect the outputs of the approximate part from the primary outputs. In this design, the switching between the approximate and exact operating modes is fast. Thus, it provides us with the opportunity of designing parallel multipliers that are capable of switching between different accuracy levels during the runtime. Next, we discuss the details of our four DQ4:2Cs based on the diagram shown in Fig. 3. The structures have different accuracies, delays, power consumptions, and area usages. Note that the ith proposed structure is denoted by DQ4:2C$_i$. The basic idea behind suggesting the approximate compressors was to minimize the difference (error) between the outputs of exact and approximate ones. Therefore, in order to choose the proper approximate designs for the compressors, an extensive search was performed. During the search, we used the truth table of the exact 4:2 compressor as the reference.

1) Structure 1 (DQ4:2C1): For the approximate part of the first proposed DQ4:2C structure, as shown in Fig. 4(a), the approximate output carry (i.e., $carry'$) is directly connected to the input x_4 ($carry' = x_4$), and also, in a similar approach, the approximate output sum (i.e., sum') is directly connected to

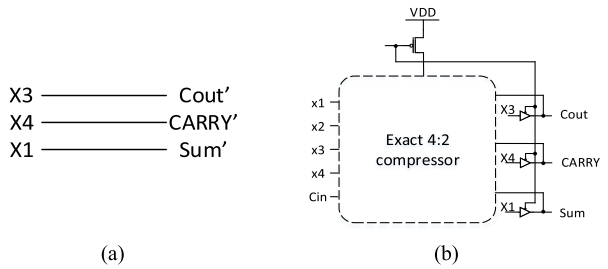

Fig. 5. (a) Approximate part and (b) overall structure of DQ4:2C$_2$.

input x_1 ($sum' = x_1$). In the approximate part of this structure, the output C_{out} is ignored. While the approximate part of this structure is considerably fast and low power, its error rate is large (62.5%).

The supplementary part of this structure is an exact 4:2 compressor. The overall structure of the proposed structure is shown in Fig. 4(b). In the exact operating mode, the delay of this structure is about the same as that of the exact 4:2 compressor.

2) Structure 2 (DQ4:2C2): In the first structure, while ignoring C_{out} simplified the internal structure of the reduction stage of the multiplication, its error was large. In the second structure, compared with the DQ4:2C$_1$, the output C_{out} is generated by connecting it directly to the input x_3 in the approximate part. Fig. 5 shows the internal structure of the approximate part and the overall structure of DQ4:2C$_2$. While the error rate of this structure is the same as that of DQ4:2C$_1$, namely, 62.5%, its relative error is lower.

3) Structure 3 (DQ4:2C3): The previous structures, in the approximate operating mode, had maximum power and delay reductions compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed. In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown in Fig. 6(a). In this structure, the accuracy of output sum' is increased. Similar to DQ4:2C$_1$, the approximate part of this structure does not support output C_{out}. The error rate of this structure, however, is reduced to 50%.

The overall structure of DQ4:2C$_3$ is shown in Fig. 6(b) where the supplementary part is enclosed in a red dashed line rectangle. Note that in this structure, the utilized NAND gate of the approximate part (denoted by a blue dotted line rectangle) is not used during the exact operating mode. Hence, during this operating mode, we suggest disconnecting supply voltage of this gate by using the power gating.

4) Structure 4 (DQ4:2C4): In this structure, we improve the accuracy of the output $carry'$ compared with that of DQ4:2C$_3$ at the cost of larger delay and power consumption where the error rate is reduced to 31.25%. The internal structure of the approximate part and the overall structure of DQ4:2C$_4$ are shown in Fig. 7. The supplementary part is indicated by red dashed line rectangular while the gates of the approximate part, powered OFF during the exact operating mode, are indicated by the blue dotted line.

Note that the error rate corresponds to the occurrence of the errors in the output for the complete range of the input.

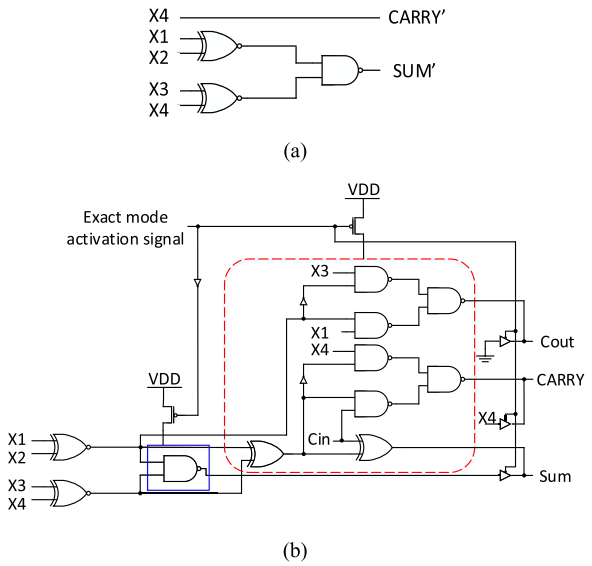

Fig. 6. (a) Approximate part of DQ4:2C$_3$ and (b) overall structure of DQ4:2C$_3$.

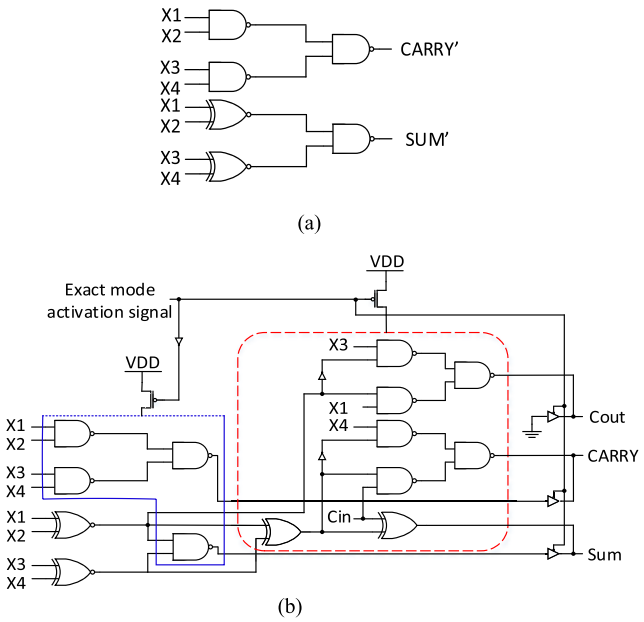

Fig. 7. (a) Approximate part of DQ4:2C$_4$ and (b) overall structure of DQ4:2C$_4$.

The output quality is determined by the error distance (ED) parameter, which is the difference between the exact output and the output of the approximate unit. In addition to the ED, there are other closely related parameters, namely, normalized ED (NED) and mean relative ED (MRED), which are more important in determining the output quality. Therefore, to judge the appropriateness of an approximate unit for an error resilient application for a given output quality, one should consider these parameters, which are explained in Section IV.

IV. Accuracy Study of Multiplier Realized by the Proposed Compressors

In this section, first, the accuracy metrics considered in this paper are introduced. Next, the accuracy of 8-, 16-, and 32-bit

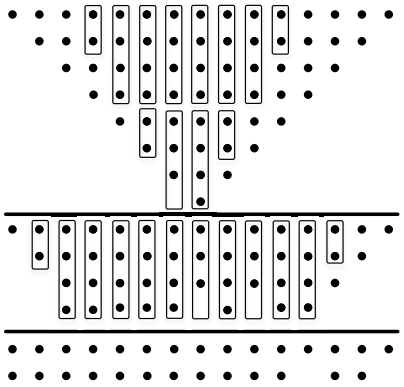

Fig. 8. Reduction circuitry of an 8-bit Dadda mutiplier.

Dadda multipliers realized by the proposed compressors is studied. A proper combination of the proposed compressors may be utilized to achieve a better tradeoff between the accuracy and design parameters. As an option, the use of both DQ4:2C$_1$ and DQ4:2C$_4$ for the LSB and MSB parts in the multiplication, respectively, is suggested here. The results for this multiplier are denoted by DQ4:2C$_{\text{mixed}}$. These multipliers are compared by the approximate Dadda multipliers implemented by two prior proposed approximate 4:2 compressors discussed in [14] as well as the configurable multiplier suggested in [15]. In addition, some state-of-the-art approximate multiplier designs, which do not use approximate compressors, are considered. These multipliers include 32-bit unsigned ROBA (U-ROBA) [17], SSM with a segment size 8 (SSM8) [10], and DRUM with a segment size 6 (DRUM6) [11]. The general structure of the reduction circuitry in an 8-bit Dadda multiplier, which makes use of 4:2 compressors, is drawn in Fig. 8.

A. Error Metrics

The four error metrics considered here for the accuracy evaluation include mean ED (MED), MRED, average NED, and number of the correct output. MED or mean absolute error is defined by [20]

$$\text{MED} = \frac{1}{2^{2N}} \sum_{i=1}^{2^{2N}} |\text{ED}_i| \tag{4}$$

where ED$_i$ is the distance between the accurate and approximate output. Also, MRED, which is defined based on the calculation of the ED between the approximate and exact output for each combination of input operands divided by the exact output, is expressed by [4]

$$\text{MRED} = \frac{1}{2^{2N}} \sum_{i=1}^{2^{2N}} \frac{|\text{ED}_i|}{S_i}. \tag{5}$$

In addition, in order to compare the approximate multipliers almost independent of their sizes, NED is defined as [4]

$$\text{NED} = \frac{\text{MED}}{D} = \frac{1}{2^{2N}} \sum_{i=1}^{2^{2N}} \frac{\text{ED}_i}{D} \tag{6}$$

TABLE I
ACCURACY OF APPROXIMATE DADDA MULTIPLIERS IN THE CASES OF DIFFERENT APPROXIMATE 4:2 COMPRESSORS

Architecture	4:2 Compressor Structure	8-bit				16-bit				32-bit			
		MED	MRED	NED	#CO	MED	MRED	NED	#CO	MED	MRED	NED	#CO
Dadda	[14] Design 1	3.99E+03	4.5410	0.0613	111	2.66E+08	12.8228	0.0620	0	1.15E+18	15.5756	0.0621	0
	[14] Design 2	3.52E+03	4.2463	0.0541	458	2.38E+08	12.1657	0.0555	1	1.02E+18	14.7724	0.0555	0
	DQ4:2C$_1$	3.54E+03	0.3692	0.0545	968	2.11E+08	0.3873	0.0492	70	9.14E+17	0.3927	0.0495	0
	DQ4:2C$_2$	2.40E+03	0.2932	0.0370	974	1.50E+08	0.3165	0.0349	70	6.46E+17	0.3205	0.0350	0
	DQ4:2C$_3$	3.22E+03	0.3281	0.0496	3349	2.19E+08	0.3287	0.0509	333	9.44E+17	0.3318	0.0511	0
	DQ4:2C$_4$	1.39E+03	0.0809	0.0213	11012	9.44E+07	0.0906	0.0220	1277	4.07E+17	0.0912	0.0221	0
	DQ4:2C$_{mixed}$	1.46E+03	0.1194	0.0225	2206	9.50E+07	0.0918	0.0221	141	4.07E+17	0.0912	0.0221	0
[15]	-	1.81E+01	0.0004	0.0003	64575	1.19E+06	0.0004	0.0003	948320	5.05E+15	0.0004	0.0003	867220
U-ROBA	-	-				-				1.30E+17	0.0292	0.0069	0
SSM8	-	-				-				2.20E+16	0.0053	0.0012	0
DRUM6	-	-				-				6.30E+16	0.0147	0.0034	0

where D is the maximum possible ED of an approximate multiplier. For most of the approximate multipliers, this value is $(2^N - 1)^2$. Thus, by replacing D in (6) by $(2^N - 1)^2$, the NED may be obtained from [14]

$$\text{NED} = \frac{\text{MED}}{(2^N-1)^2} = \frac{1}{(2^N-1)^2} \sum_{i=1}^{2^{2N}} \frac{|\text{ED}_i|}{2^{2N}}. \tag{7}$$

B. Accuracy Analysis

The accuracy metrics of the 8-, 16-, and 32-bit approximate multipliers are presented in Table I. The results were obtained by applying 65 536 (1 million uniform random) numbers in the case(s) of 8-bit (16- and 32-bit) multiplier(s). The results indicate that, almost in all the cases, the accuracies of the multipliers equipped with the proposed compressors are larger than those obtained by using the approximate compressors proposed in [14]. Specifically, the MED, MRED, and NED values of the Dadda multipliers realized using DQ4:2C$_i$ are, on average, 31.9%, 96.6%, and 31.9%, respectively, smaller than those of [14]. Also, the use of the proposed compressors in the cases of 8- and 16-bit multipliers provides more correct outputs (e.g., on average, about 14.3× more in the case of 8-bit multiplication) compared with the proposed compressors of [14]. In the cases of multiplier of [15], U-ROBA, SSM8, and DRUM6, the proposed approximate multipliers in this paper yield lower accuracies while providing better design parameters, namely, delay, power, and energy (see Section V). Also, compared with the multiplier realized by pure DQ4:2C$_4$, the design parameters of DQ4:2C$_{mixed}$ are considerable better at the price of slightly lower accuracy.

Finally, Table II shows the percentages of the outputs with NED smaller than a specific value for the approximate multiplier designs. As may be observed from Table II, in the case of NED smaller than 10%, the design of DQ4:2C$_4$, DQ4:2C$_{mixed}$, SSM8, and DRUM6 lead to higher numbers of correct outputs. For NED larger than 20%, all the designs show about the same performances.

TABLE II
PERCENTAGES OF THE OUTPUTS WITH NED SMALLER THAN A SPECIFIC VALUE FOR DIFFERENT APPROXIMATE MULTIPLIER DESIGNS

Architecture	4:2 Compressor Structure	≤ 5%	≤ 10%	≤ 15%	≤ 20%	≤ 25%
Dadda	[14] Design 1	46%	78%	99%	100%	100%
	[14] Design 2	50%	81%	100%	100%	100%
	DQ4:2C$_1$	53%	84%	95%	99%	100%
	DQ4:2C$_2$	67%	97%	100%	100%	100%
	DQ4:2C$_3$	62%	79%	92%	99%	100%
	DQ4:2C$_4$	83%	96%	99%	100%	100%
	DQ4:2C$_{mixed}$	85%	96%	99%	100%	100%
[15]	-	73%	100%	100%	100%	100%
U-ROBA	-	72%	99%	100%	100%	100%
SSM8	-	100%	100%	100%	100%	100%
DRUM6	-	99%	100%	100%	100%	100%

V. RESULTS AND DISCUSSION

In this section, first, the efficacies of the proposed 4:2 compressors in the approximate operating mode are investigated. In the investigation, which is performed by utilizing them in the Dadda structure, the design parameters of the multipliers are compared with those of the exact Dadda multiplier, approximate Dadda multipliers realized using the two approximate 4:2 compressors proposed in [14], and the approximate multiplier presented in [15]. Also, Synopsys DesignWare was used to synthesis the best architecture that it can find (multiplier expressed by "$*$"). The results for this exact multiplier are denoted by Syn. D.W. In addition, U-ROBA, SSM8, and DRUM6 approximate multipliers are also considered in this paper. Next, the effectiveness of the proposed compressors in their exact operating mode utilized in the Dadda multiplier will be compared with that of the proposed approximate multiplier by [15] in the same mode. To extract the design parameters of the multipliers, we employed Synopsys Design Compiler using a 45-nm technology [21]. Then, the performances of the approximate multipliers are assessed in some image processing applications. Finally, all the studied approximate multipliers are compared by a figure of merit (FOM) parameter and ranked based on different accuracy and design parameters.

A. Approximate Operating Mode

The design parameters of different approximate Dadda multipliers for different bit lengths are given in Table III. Note that, for the comparison purposes, the design parameters of the exact Dadda and Syn. D.W. multipliers have been

TABLE III
DESIGN PARAMETERS OF THE APPROXIMATE (AND EXACT) CONSIDERED MULTIPLIERS FOR DIFFERENT BIT LENGTHS

Architecture	Utilized 4:2 Compressors	8-bit					16-bit					32-bit				
		Delay (ns)	Area (μm^2)	Power (μW)	Energy (fJ)	EDP (ns×fJ)	Delay (ns)	Area (μm^2)	Power (μW)	Energy (fJ)	EDP (ns×fJ)	Delay (ns)	Area (μm^2)	Power (μW)	Energy (fJ)	EDP (ns×fJ)
Syn. D.W.	-	0.75	423	424	318	239	1.15	1739	2139	2460	2829	1.47	7719	9779	14375	21131
Dadda	Exact (Conv.)	0.77	526	433	333	257	1.18	1991	2320	2738	3230	1.51	8195	10500	15855	23941
	[14] Design 1	0.6	341	217	130	78	0.88	1514	1120	986	867	1.13	5699	4580	5175	5848
	[14] Design 2	0.57	312	197	112	64	0.78	1356	860	671	523	1.01	5317	3330	3363	3397
	DQ4:2C_1	0.35	206	98	34	12	0.48	326	154	74	35	0.57	735	346	197	112
	DQ4:2C_2	0.46	170	93	43	20	0.52	344	169	88	46	0.57	811	387	221	126
	DQ4:2C_3	0.49	276	194	95	46	0.69	936	651	449	310	0.92	4398	2870	2640	2429
	DQ4:2C_4	0.53	319	205	108	57	0.77	1174	841	648	499	1	4550	3260	3260	3260
	DQ4:2C_{mixed}	0.52	223	135	70	37	0.68	765	519	353	240	0.91	2572	1770	1611	1466
[15]	-	0.89	472	361	322	286	1.62	2150	2080	3370	5459	2.5	8537	9350	23375	58438
U-ROBA	-	-	-	-	-	-	-	-	-	-	-	1.12	13224	5370	6014	6736
SSM8	-	-	-	-	-	-	-	-	-	-	-	1.44	8740	4380	6310	9080
DRUM6	-	-	-	-	-	-	-	-	-	-	-	1.31	5700	5250	6880	9010

TABLE IV
DESIGN PARAMETERS OF THE CONSIDERED EXACT MULTIPLIER DESIGNS FOR DIFFERENT BIT LENGTHS

Architecture	Utilized 4:2 Compressors	8-bit					16-bit					32-bit				
		Delay (ns)	Area (μm^2)	Power (μW)	Energy (fJ)	EDP (ns×fJ)	Delay (ns)	Area (μm^2)	Power (μW)	Energy (fJ)	EDP (ns×fJ)	Delay (ns)	Area (μm^2)	Power (μW)	Energy (fJ)	EDP (ns×fJ)
Syn. D.W.	-	0.75	423	424	318	239	1.15	1739	2139	2460	2829	1.47	7719	9779	14375	21131
Dadda	Exact (Conv.)	0.77	526	433	333	257	1.18	1991	2320	2738	3230	1.51	8195	10500	15855	23941
	DQ4:2C_1	0.78	530	431	336	262	1.19	2034	2333	2776	3304	1.54	8296	10500	16170	24902
	DQ4:2C_2	0.79	539	434	343	271	1.19	2005	2337	2781	3309	1.55	8381	10551	16354	25349
	DQ4:2C_3	0.79	543	435	344	272	1.2	2124	2336	2803	3364	1.55	8595	10530	16322	25298
	DQ4:2C_4	0.8	560	437	349	280	1.2	2339	2344	2813	3375	1.56	8881	10560	16474	25699
	DQ4:2C_{mixed}	0.79	541	433	342	270	1.19	2117	2339	2783	3312	1.55	8412	10553	16357	25353
[15]	-	0.91	509	399	363	331	1.66	2292	2090	3469	5759	2.54	8678	9410	23901	60710

provided as well. As the results indicate, for all the design parameters under different bit lengths (except for the area usage of DQ4:2C_4 for the bit length of 8), the proposed DQ4:2Cs lead to better parameters. For the 8-bit structures, the comparison between the area usages of DQ4:2C_4 and the second design of [14] reveals that, while the gate count for the former is smaller, the area of the latter is slightly smaller due to the optimization performed by the synthesis tool. Also, in the case of the 8-bit multiplication, the delay, area, power, energy, and EDP of the proposed multipliers are, on average, 41%, 54%, 66%, 79%, and 87%, respectively, better than those of the exact Dadda multiplier. Also, compared with the average values of the parameters of the compressor of design 1 and design 2 in [14] (see [15]), the same parameters are lower, on average, by 22%, 26%, 39%, 53%, and 63% (49%, 49%, 74%, 86%, and 93%), respectively. The improvements increase as the bit length increases. For the 16-bit multipliers, the delay, area, power, energy, and EDP of the Dadda multipliers using the proposed approximate compressors are improved compared with those of the Dadda multipliers employing the proposed compressors of [14] (and also the multiplier proposed in [15]), on average, by 25.9% (62%), 51.6% (67.7%), 54.2% (78.2%), 62% (90.7%), and 68% (95.9%), respectively. Also, the delay, area, power, energy, and EDP of approximate Dadda multipliers utilizing our proposed compressors are better compared with the exact Dadda multiplier, on average, by 47.9%, 65.1%, 80.4%, 88.5%, and 93.1% (93.4%), respectively.

Finally, the delay, area, power, energy, and EDP of the approximate 32-bit Dadda multipliers using the proposed compressors are lower compared with the exact Dadda multiplier, on average, by 49.3%, 68%, 83.7%, 90%, and 93.8%, respectively. Also, when compared with the Dadda multiplier realized by the proposed approximate compressors of [14] (and the approximate multiplier proposed in [15]), the delay, area, power, energy, and EDP of the approximate 32-bit Dadda multipliers realized by our proposed compressors are better, on average, by 29% (69%), 52% (69%), 57% (82%), 63% (93%), and 68% (98%), respectively. The comparison with other approximate multipliers, which do not use compressors in their structure shows that the delay, area, power, energy, and EDP of the our approximate Dadda multipliers are smaller than those of U-ROBA (SSM8 and DRUM6), on average, by 32% (47% and 42%), 80% (70% and 54%), 68% (61% and 67%), 74% (75% and 77%), and 78% (84% and 84%), respectively.

B. Exact Operating Mode

The design parameters of exact multipliers are presented in Table IV, which reveals that the Dadda multipliers using the proposed DQ4:2Cs have smaller delays, energies, and EDPs for all the cases compared with those of the multiplier proposed in [15]. In the exact mode, due to use of tristate buffers as the output isolators, the design parameters are slightly larger than those of the corresponding exact multiplier. For the 8-bit (16- and 32-bit) multiplication, the Dadda multiplier implemented by the DQ4:2C structures has, on average,

TABLE V
MSSIMS OF THE OUTPUTS OF SMOOTHING AND SHARPENING FILTERS WHEN USING DIFFERENT APPROXIMATE COMPRESSORS DESIGNS IN MULTIPLICATION UNIT

	Smoothing								Sharpening							
Bench.	Design 1 [14]	Design 2 [14]	DQ4:2 C_1	DQ4:2 C_2	DQ4:2 C_3	DQ4:2 C_4	DQ4:2 C_{mixed}	U-ROBA	Design 1 [14]	Design 2 [14]	DQ4:2 C_1	DQ4:2 C_2	DQ4:2 C_3	DQ4:2 C_4	DQ4:2C $_{mixed}$	U-ROBA
girl	0.28	0.28	0.29	0.29	0.58	0.62	0.50	0.64	0.00	0.00	0.50	0.52	0.59	0.67	0.64	0.70
Tiffany	0.65	0.65	0.40	0.40	0.49	0.76	0.65	0.77	0.00	0.00	0.44	0.46	0.55	0.70	0.67	0.72
moon	0.37	0.37	0.29	0.29	0.51	0.56	0.46	0.58	0.00	0.00	0.64	0.66	0.75	0.80	0.79	0.84
cameraman	0.30	0.30	0.40	0.40	0.57	0.60	0.50	0.62	0.00	0.00	0.59	0.60	0.64	0.68	0.66	0.69
Einstein	0.31	0.31	0.26	0.26	0.56	0.62	0.50	0.64	0.00	0.00	0.55	0.58	0.68	0.75	0.72	0.79
Elaine	0.30	0.30	0.39	0.39	0.62	0.70	0.60	0.71	0.00	0.00	0.66	0.68	0.78	0.83	0.82	0.86
Lena	0.23	0.23	0.31	0.31	0.64	0.68	0.55	0.70	0.00	0.00	0.59	0.60	0.69	0.75	0.73	0.78
house	0.29	0.29	0.31	0.31	0.59	0.66	0.54	0.68	0.00	0.00	0.65	0.66	0.77	0.80	0.77	0.82
peppers	0.26	0.26	0.37	0.37	0.63	0.68	0.59	0.70	0.00	0.00	0.61	0.62	0.70	0.74	0.73	0.78
tulips	0.18	0.18	0.41	0.41	0.71	0.79	0.68	0.80	0.00	0.00	0.71	0.73	0.84	0.89	0.87	0.91
Average	0.32	0.32	0.34	0.34	0.59	0.67	0.56	0.68	0.00	0.00	0.59	0.61	0.70	0.76	0.74	0.79

2.6% (1.3% and 2.6%), 3.2% (6.7% and 4.2%), 0.3% (0.8% and 0.3%), 2.9% (2% and 3%), and 5.6% (3.3% and 5.7%) larger delay, area, power, energy, and EDP, respectively, compared with the exact conventional multiplier. On the other hand, the 8-bit (16- and 32-bit) our suggested multiplier provides, on average, 13% (28% and 39%), 6% (20% and 38%), and 18% (42% and 58.3%) lower delay, energy, and EDP, respectively, compared with the proposed multiplier in [15]. The proposed 8-bit (16- and 32-bit) multiplier in [15] leads to smaller power by 8.1% (10.6% and 10.7%) compared with those of the Dadda multiplier enhanced by the DQ4:2C structures. In addition, in terms of the area, the proposed multiplier of [15] has 6.3% smaller area for the 8-bit multiplier, while for the 16- and 32-bit multipliers, the multipliers realized by the proposed DQ4:2C structures provide, on average, 7.3% and 1.6% lower area usages, respectively. Finally, the switching time overheads for the proposed compressors were analyzed using HSpice simulations. The results indicated transition times of 22–26 ps for different types of the compressors for the technology used in this paper. Obviously, during the transition, the outputs are not valid.

C. Image Processing Applications

In this section, to assess the effectiveness of the proposed compressors in real applications, they are utilized in three image processing applications. Here, we used six 8-bit approximate multipliers modeled using our proposed compressors along with the two compressors proposed in [14]. The three studied image processing applications were smoothing, sharpening, and image multiplication. In all the considered image processing applications, the output image qualities obtained by employing the multipliers of [15], SSM8, and DRUM6 were larger than 0.9, which is very close to one as the value for the perfect quality, and hence, their results have not been reported here.

In the sharpening application [22], the output sharpened image is obtained from

$$Y(i,j) = 2.X(i+m, j+n) - \frac{1}{273}\sum_{m=-2}^{2}\sum_{n=-2}^{2} \times X(i+m, j+n)\cdot \text{Mask}_{\text{Sharpening},1}(m+3, n+3) \quad (8)$$

where X and Y are the input and output images, and $\text{Mask}_{\text{Sharpening}}$ matrix is

$$\text{Mask}_{\text{sharpening}} = \begin{bmatrix} 1 & 4 & 7 & 4 & 1 \\ 4 & 16 & 26 & 16 & 4 \\ 7 & 26 & 41 & 26 & 7 \\ 4 & 16 & 26 & 16 & 4 \\ 1 & 4 & 7 & 4 & 1 \end{bmatrix}. \quad (9)$$

For the smoothing application, the following equation [23] is used to determine the smoothed output image:

$$Y(i,j) = \frac{1}{60}\sum_{m=-2}^{2}\sum_{n=-2}^{2} \times X(i+m, j+n)\cdot \text{Mask}(m+3, n+3) \quad (10)$$

where $\text{Mask}_{\text{Smoothing}}$ is given by

$$\text{Mask}_{\text{smoothing}} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 4 & 4 & 4 & 1 \\ 1 & 4 & 12 & 4 & 1 \\ 1 & 4 & 4 & 4 & 1 \\ 1 & 4 & 7 & 4 & 1 \end{bmatrix}. \quad (11)$$

In this paper, ten standard benchmark images from [24] were used. Peak signal-to-noise ratio is one of the parameters, which is used for investigating the quality of (approximate) images [25]. This parameter does not necessarily has appropriate consistency with the image quality perceived by the human [25]. A better parameter for this purpose is mean structural similarity index metric (MSSIM), which works based on measuring the structural similarity of the exact and approximate images [25]. It is based on the principle that the human visual system is capable of extracting information based on the image structure. The expression for this parameter, which is rather complex, is explained in detail in [25]. Table V reports the MSSIMs of the outputs of the smoothing and sharpening filters when different approximate compressor designs are employed in the multiplication unit (the MSSIM of the exact filtered image is one). As the results show, U-ROBA leads to the highest MSSIMs among the considered approximate multipliers. In the case of the smoothing application, except for the three images, our proposed compressors provide the higher MSSIMs for all the benchmarks compared with the those of

TABLE VI
MSSIMS OF THE OUTPUTS OF IMAGE MULTIPLICATION WHEN USING DIFFERENT APPROXIMATE COMPRESSORS DESIGNS IN MULTIPLICATION UNIT

	Design 1 [14]	Design 2 [14]	DQ4:2C$_1$	DQ4:2C$_2$	DQ4:2C$_3$	DQ4:2C$_4$	DQ4:2C$_{mixed}$	U-ROBA
moon × cameraman	0.65	0.69	0.64	0.68	0.66	0.91	0.90	0.94
cameraman × Einstein	0.65	0.71	0.63	0.73	0.75	0.94	0.93	0.89
Einstein × Elaine	0.68	0.72	0.60	0.72	0.62	0.92	0.91	0.96
Elaine × Lena	0.67	0.70	0.61	0.73	0.69	0.93	0.93	0.97
Lena × house	0.62	0.65	0.63	0.77	0.75	0.95	0.95	0.93
house × peppers	0.67	0.71	0.64	0.76	0.71	0.94	0.93	0.93
peppers × tulips	0.70	0.73	0.64	0.77	0.73	0.94	0.94	0.95
Average	0.66	0.70	0.63	0.74	0.70	0.93	0.93	0.94

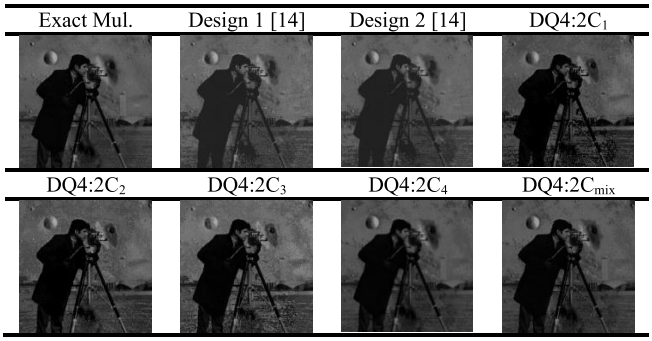

Fig. 9. Multiplied images of the moon and the camera man images employing different approximate multipliers.

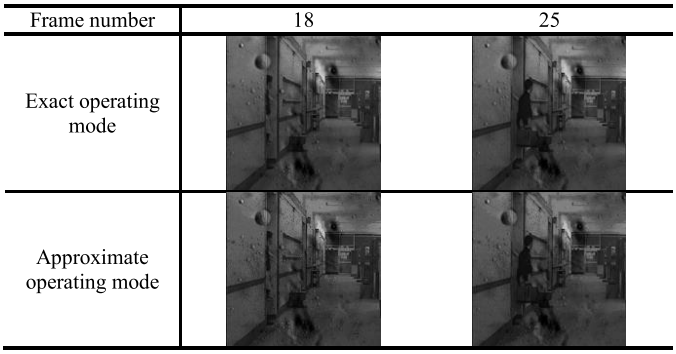

Fig. 10. Images obtained using the exact and approximate mode multiplication of the frames 18 and 25 of the Hall_Monitor video benchmark by the Moon image.

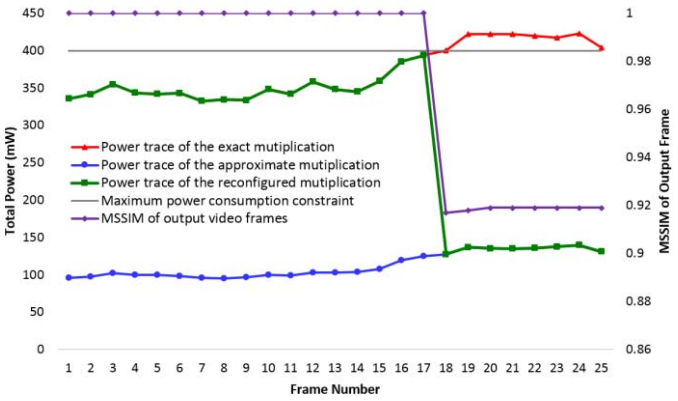

Fig. 11. Total powers consumed during the exact and approximate modes of multiplication as well as the MSSIM of the output frames.

the multipliers realized based on the approximate compressors of [14]. In the smoothing application, on average, DQ4:2Cs provide 52% larger MSSIMs compared with the average of the values of the compressor design 1 and design 2 in [14].

For the sharpening filter application, using the compressors of [14] leads to the MSSIMs of zero for all the benchmarks due to its low quality. Finally, Table VI gives the MSSIMs of the image multiplication by using different approximate multiplier designs. In this case, except for DQ4:2C$_1$, our proposed compressors provide higher MSSIMs for almost all the benchmark images compared with multipliers realized approximate compressors of [14]. As the results indicate, using DQ4:2C$_4$ provides the highest MSSIMs compared with the other multipliers realized by the approximate compressors. Similar to smoothing and sharpening applications, U-ROBA (most of the times) leads to higher MSSIMs compared with the multipliers realized our proposed compressors in multiplication application. However, the MSSIMs of DQ4:2C$_4$ and DQ4:2C$_{mix}$ in this application are very close to those of the U-ROBA (only 0.8% smaller).

In the image multiplication application, the suggested multipliers of this paper provide, on average, 10% higher MSSIMs, when compared with the average of those of [14]. To provide some tangible feeling about the effect of the approximate multiplications on the image qualities, as an example, here, we have shown the multiplied images of the moon and the camera man images employing different approximate multipliers in Fig. 9.

Finally, we provide some results for demonstrating the use of the reconfigurability feature of the multiplier here. The multiplier based on DQ4:2C$_{mixed}$ approximate compressor is considered here. The results are for 25 frames of "Hall_Monitor" video benchmark [26], which have been multiplied by the "Moon" image benchmark [24]. For this paper, a maximum power consumption constraint of 400 mW is set, such that if the multiplication power consumption exceeds this amount, then the multiplication switches from the exact operating mode to the approximate one. In Fig. 10, the images obtained using the exact and approximate mode multiplication of the frames 18 and 25 of the Hall_Monitor video benchmark by the Moon image are compared. The differences between the corresponding images are not easily distinguishable.

Fig. 11 shows the power traces of the exact (red triangle-marked line) and approximate multiplications (blue circle-marked line), as well as the MSSIM value of the output video frames (violet diamond-marked line). In Fig. 11,

TABLE VII
RANKINGS OF THE APPROXIMATE MULTIPLIERS BASED ON THE NED, DESIGN, MSSIM, AND FOM PARAMETER

	NED	Delay	Power	EDP	MSSIM (for Smoothing)	MSSIM (for Sharpening)	MSSIM (for Image Mul.)	(Energy×Delay×Area) /(1 – NED)
Design 1 [14]	11	8	7	7	11	11	10	7
Design 2 [14]	10	7	6	6	10	10	9	6
DQ4:2C_1	8	1	1	1	9	9	11	1
DQ4:2C_2	7	2	2	2	8	8	7	2
DQ4:2C_3	9	4	4	4	6	7	8	4
DQ4:2C_4	5	5	5	5	5	5	5	5
DQ4:2C_{mixed}	6	3	3	3	7	6	6	3
[15]	1	11	11	11	1	1	1	11
U-ROBA	4	6	10	8	4	4	4	10
SSM8	2	10	8	10	2	2	2	9
DRUM6	3	9	9	9	3	3	3	8

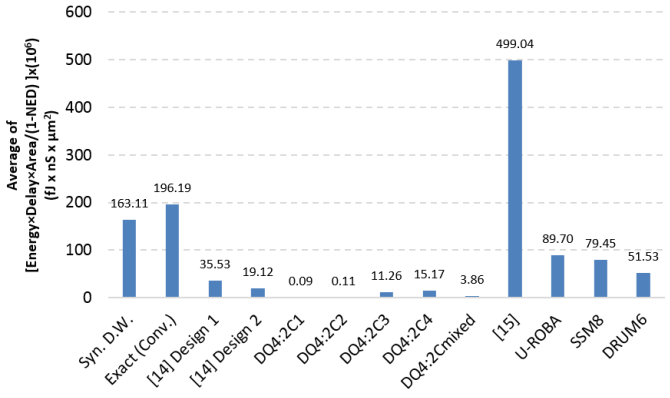

Fig. 12. FOM parameter of the considered approximate multipliers.

the power consumption of the reconfigured multiplication is also plotted (green square-marked line). As the results reveal, in the approximate mode, the power consumption decreases, on average, by about 68% when compared with that of the exact mode.

D. Efficacy Comparison of Considered Approximate Multipliers

In order to provide more insight on the effectiveness of the approximate units, we define an FOM based on the accuracy and design parameters as (Energy × Delay × Area)/((1 − NED)). This FOM has been used in comparing the approximate 32-bit multipliers where the results have been presented in Fig. 12. The comparison indicates that the multipliers realized based on the suggested compressors have smaller FOM values, which shows the superiority of the proposed compressors compared with the other structures. In addition, the ranks of the studied approximate multipliers based on different parameters are presented in Table VII.

As the results indicate, in general, the increase in the error parameters may be the result of more simplification (approximation) of the unit while providing better design parameters. This trend may not follow the rule when the multiplier structure changes from one to another. Specifically, for most of the parameters, the rankings of the proposed multipliers in this paper are better than those of the multipliers proposed in [14].

VI. CONCLUSION

In this paper, we presented four DQ4:2Cs, which had the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these compressors provided higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors had its own level of accuracy in the approximate mode as well as different delays and powers in the approximate and exact modes. These compressors were employed in the structure of a 32-bit Dadda multiplier to provide a configurable multiplier whose accuracy (as well as its power and speed) could be changed dynamically during the runtime. Our studies revealed that for the 32-bit multiplication, the proposed compressors yielded, on average, 46% and 68% lower delay and power consumption in the approximate mode compared with those of the recently suggested approximate compressors. Also, utilizing the proposed compressors in 32-bit Dadda multiplier provided, on average, about 33% lower NED compared with the state-of-the-art compressor-based approximate multipliers. When comparing with noncompressor-based approximate multipliers, the errors of the proposed multipliers were higher while the design parameters were considerably better. Finally, our studies showed that the multipliers realized based on the suggested compressors have, on average, about 93% smaller FOM value compared with the considered approximate multipliers.

REFERENCES

[1] P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in *Proc. 24th Int. Conf. VLSI Design*, Jan. 2011, pp. 346–351.
[2] D. Baran, M. Aktan, and V. G. Oklobdzija, "Multiplier structures for low power applications in deep-CMOS," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 1061–1064.
[3] S. Ghosh, D. Mohapatra, G. Karakonstantis, and K. Roy, "Voltage scalable high-speed robust hybrid arithmetic units using adaptive clocking," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 9, pp. 1301–1309, Sep. 2010.
[4] O. Akbari, M. Kamal, A. Afzali-Kusha, and M. Pedram, "RAP-CLA: A reconfigurable approximate carry look-ahead adder," *IEEE Trans. Circuits Syst. II, Express Briefs*, doi: 10.1109/TCSII.2016.2633307.
[5] A. Sampson *et al.*, "EnerJ: Approximate data types for safe and general low-power computation," in *Proc. 32nd ACM SIGPLAN Conf. Program. Lang. Design Implement. (PLDI)*, 2011, pp. 164–174.
[6] A. Raha, H. Jayakumar, and V. Raghunathan, "Input-based dynamic reconfiguration of approximate arithmetic units for video encoding," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 3, pp. 846–857, May 2015.

[7] J. Joven *et al.*, "QoS-driven reconfigurable parallel computing for NoC-based clustered MPSoCs," *IEEE Trans. Ind. Informat.*, vol. 9, no. 3, pp. 1613–1624, Aug. 2013.
[8] R. Ye, T. Wang, F. Yuan, R. Kumar, and Q. Xu, "On reconfiguration-oriented approximate adder design and its application," in *Proc. IEEE/ACM Int. Conf. Comput. Aided Design (ICCAD)*, Nov. 2013, pp. 48–54.
[9] M. Shafique, W. Ahmad, R. Hafiz, and J. Henkel, "A low latency generic accuracy configurable adder," in *Proc. 52nd ACM/EDAC/IEEE Design Autom. Conf. (DAC)*, Jun. 2015, pp. 1–6.
[10] S. Narayanamoorthy, H. A. Moghaddam, Z. Liu, T. Park, and N. S. Kim, "Energy-efficient approximate multiplication for digital signal processing and classification applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 6, pp. 1180–1184, Jun. 2015.
[11] S. Hashemi, R. I. Bahar, and S. Reda, "DRUM: A dynamic range unbiased multiplier for approximate applications," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Austin, TX, USA, Nov. 2015, pp. 418–425.
[12] K. Y. Kyaw, W. L. Goh, and K. S. Yeo, "Low-power high-speed multiplier for error-tolerant application," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Dec. 2010, pp. 1–4.
[13] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 4, pp. 850–862, Apr. 2010.
[14] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," *IEEE Trans. Comput.*, vol. 64, no. 4, pp. 984–994, Apr. 2015.
[15] C. H. Lin and I. C. Lin, "High accuracy approximate multiplier with error correction," in *Proc. IEEE 31st Int. Conf. Comput. Design (ICCD)*, Oct. 2013, pp. 33–38.
[16] C. Liu, J. Han, and F. Lombardi, "A low-power, high-performance approximate multiplier with configurable partial error recovery," in *Proc. Conf. Design, Autom. Test Eur. (DATE)*, 2014, Art. no. 95.
[17] R. Zendegani, M. Kamal, M. Bahadori, A. Afzali-Kusha, and M. Pedram, "RoBA multiplier: A rounding-based approximate multiplier for high-speed yet energy-efficient digital signal processing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, doi: 10.1109/TVLSI.2016.2587696.
[18] C. H. Chang, J. Gu, and M. Zhang, "Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 10, pp. 1985–1997, Oct. 2004.
[19] D. Baran, M. Aktan, and V. G. Oklobdzija, "Energy efficient implementation of parallel CMOS multipliers with improved compressors," in *Proc. ACM/IEEE Int. Symp. Low-Power Electron. Design (ISLPED)*, Aug. 2010, pp. 147–152.
[20] J. Liang, J. Han, and F. Lombardi, "New metrics for the reliability of approximate and probabilistic adders," *IEEE Trans. Comput.*, vol. 62, no. 9, pp. 1760–1771, Sep. 2013.
[21] (2016). *NanGate—The Standard Cell Library Optimization Company*. [Online]. Available: http://www.nangate.com/
[22] M. S. K. Lau, K. V. Ling, and Y. C. Chu, "Energy-aware probabilistic multiplier: Design and analysis," in *Proc. Int. Conf. Compil., Archit., Synth. Embedded Syst.*, 2009, pp. 281–290.
[23] H. R. Myler and A. R. Weeks, *The Pocket Handbook of Image Processing Algorithms in C*. Englewood Cliffs, NJ, USA: Prentice-Hall, 2009.
[24] Sipi.usc.edu. (2016). *SIPI Image Database*. [Online]. Available: http://sipi.usc.edu/database/
[25] Z. Wang, A. C. Bovik, H. R. Sheikh, and E. P. Simoncelli, "Image quality assessment: From error visibility to structural similarity," *IEEE Trans. Image Process.*, vol. 13, no. 4, pp. 600–612, Apr. 2004.
[26] Trace.eas.asu.edu. (2016). *YUV Sequences*. [Online]. Available: http://trace.eas.asu.edu/yuv/

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