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Single-phase hybrid cascaded H-bridge and diode-clamped multilevel inverter with capacitor voltage balancing

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Abstract: Diode-clamped and cascaded H-bridge multilevel inverters are two of the main multilevel inverter topologies; each has its distinct advantages and drawbacks. Regarding the latter, cascaded H-bridge inverters require multiple separate dc sources, whereas (semi-active) diode-clamped inverters contain capacitors that require a means to balance their voltages. This paper investigates a hybrid-topology inverter, comprising a single-phase five-level semi-active diode-clamped inverter and a single-phase cascaded H-bridge inverter with their outputs connected in series, as one way to mitigate the drawbacks of each topology. The proposed control scheme for this inverter operates the switches at fundamental frequency to achieve capacitor voltage-balancing while keeping the switching losses low. Moreover, the step-angles are designed for the 13-level and 11-level output voltage waveform cases (as examples) for a fixed modulation index to achieve optimal total harmonic distortion. Furthermore, the scheme also achieves capacitor voltage-balancing for modulation indices that are close to the optimal modulation index, and for a wide range of load power factors, albeit at the cost of increased output voltage distortion. Simulation results are presented to help explain the processes of capacitor recharging and voltage-balancing, while experimental results are shown as verification of the expected behaviour of this inverter and the proposed control scheme.

1 Introduction

Dual-use ac power generators that are operated to provide peak shaving on a regular basis and to provide backup/emergency power on an as needed basis are beneficial in several ways. For customers, using these on-site generators in a dual role maximises their value, especially since peak shaving can often help them avoid paying (the higher) demand charges. For utilities, this helps them to possibly avoid the higher costs of bringing additional capacity online to meet the peak demand [1]. However, most backup generators currently available are powered by diesel engines, while the rest are fuelled by natural gas or a combination of diesel and gas. Thus, to use them for peak shaving regularly would result in undesirable emissions that are strictly regulated by governmental agencies, e.g. [2, 3]. Therefore, efforts are being undertaken to develop alternative dual-use ac power supplies. This paper investigates a multilevel converter – possibly supplied by a combination of fuel cells, solar arrays and batteries – that could be used in such applications. One example, but not limited to this, is placing the ac power supply in a hospital's parking garage (these will likely be key power nodes as electrified cars proliferate) and connecting it to adjacent buildings, where a higher supply voltage would lower the distribution losses.

In 1975, the cascaded H-bridge converter [4] was introduced as the first topology of multilevel inverters (MLIs). This was followed by the diode-clamped (neutral-clamped) topology [5], which utilised a bank of series capacitors for supplying the input dc voltages. Subsequently, the flying capacitor (capacitor-clamped) topology [6] was also introduced, employing floating capacitors rather than series capacitors for maintaining dc voltages. The common concept underlying these topologies is to have various input dc voltages 'added' together at the inverter output, via judicious switching of power semiconductor devices, so as to produce an ac waveform that is sinusoidal together with some acceptable amount of higher harmonics. This approach is advantageous due to the higher voltage capability obtained from lower-rated devices, reduced switching losses, better electromagnetic compatibility and less required filtering [7]. However, drawbacks of MLIs include the need for separated dc sources (in the cascaded H-bridge case), and the need for capacitor voltage balancing (in the diode-clamped and flying capacitor cases) [7]; in particular, for the diode-clamped MLI, it is unable to balance its capacitors' voltages during real power conversion without sacrificing output voltage performance [8].

Due to the need for diode-clamped and capacitor-clamped MLIs to require additional circuits to balance their capacitors' voltages and avoid impaired performance, a generalised three-phase MLI topology using diodes, capacitors and transistors for clamping purposes was proposed by Peng [9]. This subsumes two topologies that use fewer transistors, one with only passive clamping devices proposed by Suh and Hyun [10], and the other with both passive and active clamping devices proposed by Chen and He [11]. However, although the MLI topologies of [9, 11] can keep their capacitor voltages balanced during purely reactive conversions, the MLI topology of [10] cannot.

Then in [12], a hybrid nine-level inverter consisting of a three-phase three-level diode-clamped inverter, with a two-level H-bridge in series with each phase was proposed for drive application. The H-bridges are connected to capacitors instead of power sources, thus can only supply reactive power. A complex non-linear model-predictive controller was proposed to stabilise the floating capacitor voltages of the H-bridges and the diode-clamped inverter by deliberately varying the common-mode voltage of the drive's three-phase output. The same topology was also studied by the authors of [13, 14] and others, with various control algorithms offered to regulate the floating dc links to desired values while striving to minimise the lowest harmonics present in the converter's output. On the other hand, work on a single-phase asymmetric seven-level diode-clamped inverter with its output connected in series with a three-level H-bridge inverter was described in [15]. However, a multi-output boost converter connected to the dc link's capacitors was the means for regulating the capacitors' voltages, rather than a process 'internal' to the inverter.

Regarding capacitor voltage balancing, a key principle relied on is the existence of inverter redundant states, i.e. different combinations of the inverter transistors' on or off states yielding the same output voltage level, whether it be a phase voltage or a line voltage. This has motivated a substantial amount of research on various modulation schemes for both single-phase and three-phase inverters that rely on per-phase redundancy and/or joint-

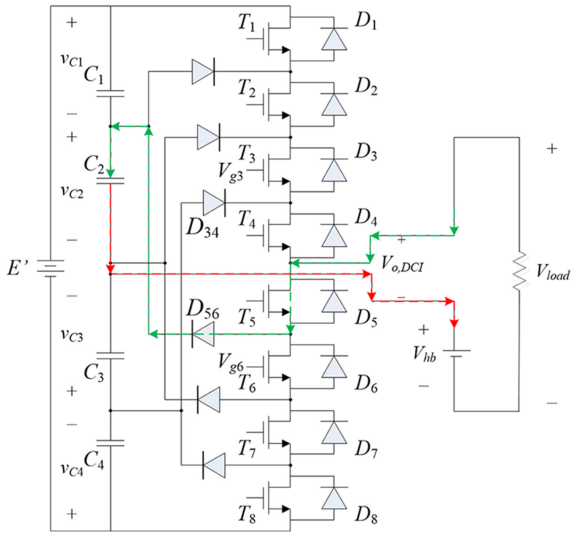

Fig. 1 *Five-level 1ϕ-DCMLI with semi-active front end*

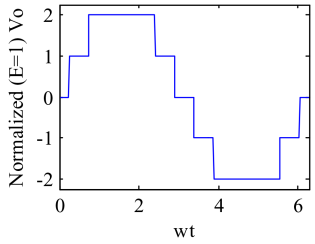

Fig. 2 *Five-level (two-step) waveform with equal levels*

phase redundancy, respectively, to achieve capacitor voltage balancing [16–21]. Interestingly, although several single-phase and three-phase MLI circuits are presently known to possess redundant states, the single-phase diode-clamped MLI (1ϕ-DCMLI) has been characterised as not having such states [22].

To obtain an advantageous embodiment of a MLI with a reduced number of separate dc sources, one possibility is to use the 'mixed-level hybrid multilevel cells' [7] approach, with multilevel diode-clamped or capacitor-clamped inverters replacing one or more H-bridge cells in a cascaded inverter [23]. However, a means of maintaining the capacitor voltages at the desired levels is needed, otherwise the waveform will become increasingly distorted over time, especially with smaller-sized capacitors. Recently, Diong *et al.* [24] had proposed replacing a subset of cascaded H-bridge inverter cells by a 1ϕ-DCMLI to reduce the required number of separate dc sources. In addition, they had proposed a means of re-charging the 1ϕ-DCMLI's inner capacitors for the semi-active front-end case, based on the discovery that a 1ϕ-DCMLI with its output connected in series with a voltage source can exhibit redundant states, depending on this source's magnitude and its polarity; a feature referred to as forced redundant states in [25], which studied this behaviour in greater detail.

This present paper describes how the series connection of a single phase cascaded H-bridge MLI (1ϕ-CHBMLI) and a five-level 1ϕ-DCMLI can balance its capacitors' voltage internally, which improves upon [15]. It will illustrate the advantage over a CHBMLI-only circuit of having reduced number of dc sources, and the advantage over a DCMLI-only circuit of having built-in, i.e. integral, capacitor voltage balancing capability. The next section will briefly review how the 1ϕ-DCMLI can be made to exhibit redundant states and how this behaviour corresponds to being able to recharge its capacitors. Later sections will introduce the new hybrid 1ϕ-CHBMLI plus 1ϕ-DCMLI topology, and a way to operate it to maintain balanced capacitor voltages while minimising transistor switching losses. Compared with the above-mentioned three-phase hybrid circuits [12–14], voltage balancing of the *inner* capacitors in the DCMLI half is needed, instead of controlling the voltages of *floating* capacitors. Also, the proposed control scheme is simpler than those in [12–14]. Simulation and experimental results are presented to verify the theoretical work, followed by brief concluding remarks.

2 Forced redundant states of 1ϕ-DCMLI

To briefly review this phenomenon first described in [24] and then detailed by Chaulagain and Diong [25], we restrict our attention to the five-level 1ϕ-DCMLI with a semi-active (a single voltage source applied across a bank of series-connected capacitors) front-end as diagrammed in Fig. 1, with the voltage source $V_{hb} = 0$ for the time being. In addition, it is assumed that the diodes are ideal, the load is purely resistive and the equally-sized capacitors – supplied by a single paralleled dc power source – nominally have equal voltages across each of them. Then, according to the usual practice [5, 7, 22], various combinations of four out of the eight transistors are switched on (the remaining four being switched off, in a complementary fashion) to produce one of five different levels at the 1ϕ-DCMLI's output. To illustrate, let the states of transistors T_4, T_3, T_2 and T_1 be represented by (σ_4, σ_3, σ_2, σ_1), respectively, with $\sigma_i = 0$ (off) or 1 (on), $i = 1$ to 4; then the states of transistors T_8, T_7, T_6 and T_5 represented by (σ_8, σ_7, σ_6, σ_5), respectively, are the bit-complement of (σ_4, σ_3, σ_2, σ_1). As has been the convention, the stepped waveform shown in Fig. 2, starting with the 0 V level, can be obtained by periodic staircase modulation of the switches through states (σ_4, σ_3, σ_2, σ_1) = (1, 1, 0, 0), (1, 1, 1, 0), (1, 1, 1, 1), (1, 1, 1, 0), (1, 1, 0, 0), (1, 0, 0, 0), (0, 0, 0, 0), (1, 0, 0, 0), and (1, 1, 0, 0). However, this modulation scheme causes the inner capacitors C_2 and C_3 to be discharged over longer intervals than C_1 and C_4, resulting in $|v_{c2}| < |v_{c1}|$ and $|v_{c3}| < |v_{c4}|$, so this circuit not possessing redundant states means that some form of external intervention is needed to balance the capacitors' voltages so as to obtain the desired unimpaired ac output.

Recently though, it was shown in [25] (among other results) that when dc source V_{hb} in Fig. 1 is negative with a magnitude greater than v_{c2}, switch state (1, 0, 1, 0) results in $V_{\text{load}} = V_{hb} + v_{c2}$ while simultaneously adding charge to C_2 via current flow and thereby increasing v_{c2}; the key point being that T_5 is on while T_6 is off causing diode D_{56} to conduct current flowing from V_{hb}. In a symmetrical fashion, when V_{hb} is positive with a magnitude greater than v_{c3}, switch state (1, 0, 1, 0) results in $V_{\text{load}} = V_{hb} - v_{c3}$ while simultaneously adding charge to C_3 and thereby increasing v_{c3}. Since it is necessary for V_{hb} to be present and large enough to produce these and other results using the 1ϕ-DCMLI's non-conventional states, this behaviour has been named forced redundancy [25].

3 Proposed hybrid cascaded H-bridge and diode-clamped inverter

The proposed inverter circuit is a series connection of the above-mentioned 1ϕ-DCMLI and a 1ϕ-CHBMLI (taking the place of dc source V_{hb} in Fig. 1, for producing either positive or negative voltages). As is well-known, the 1ϕ-CHBMLI consists of a series connection of H-bridge cells that is typically operated to output a voltage waveform having $2n + 1$ levels, where n is the number of cells. This is illustrated by the five-level (two-cell) 1ϕ-CHBMLI diagrammed in Fig. 3, which can be operated to produce the five-level (two-step) waveform of Fig. 2 for $E_1 = E_2 = E = 1$.

3.1 13-level waveform case

To make the hybrid inverter's advantages clearer, and its proposed method of operation more easily understood, we now focus on the series connection of a nine-level 1ϕ-CHBMLI with a five-level 1ϕ-DCMLI where the CHBMLI's input voltages and the DCMLI's input voltage satisfy the conditions

$$E_4 = E_3 = E_2 = E_1 (= E) \tag{1}$$

$$4E > E' \tag{2}$$

First note that only five separate dc sources are needed to produce a 13-level output voltage instead of six sources with a purely CHBMLI topology. Next, while the CHBMLI is operated as usual to produce a voltage with nine levels (corresponding to step angles θ_{C1}, θ_{C2}, θ_{C3}, θ_{C4}, as illustrated by the MATLAB Simulink simulation result shown in Fig. 4), let us consider the DCMLI being operated with its states cycling through $(\sigma_4, \sigma_3, \sigma_2, \sigma_1) = (1, 0, 1, 0)$, $(1, 1, 1, 0)$, $(1, 1, 1, 1)$, $(1, 1, 1, 0)$, $(1, 0, 1, 0)$, $(1, 0, 0, 0)$, $(0, 0, 0, 0)$, $(1, 0, 0, 0)$ and $(1, 0, 1, 0)$, which will be shown below to result in the recharging of the DCMLI's capacitors C_2 and C_3. One way to view this new operating method is that the usual control signals for transistors T_2 and T_3 have been swapped, as have the usual control signals for transistors T_6 and T_7 (being complementary to T_2 and T_3, respectively). Importantly, this is still a fundamental-frequency modulation scheme, which results in minimal switching losses.

Let θ_{D1} and θ_{D2} be the step angles associated with the first and second transitions, respectively, of the DCMLI's output $V_{o,\mathrm{DCI}}$ as shown in Fig. 4; θ_{D1} determines when T_2, T_3, T_6 and T_7 turn on (or off), while θ_{D2} determines when T_1, T_4, T_5 and T_8 turn on (or off). From a functional viewpoint, when $\theta_{C1} < \theta_{C2} < \theta_{C3} < \theta_{C4} < \theta_{D1} < \theta_{D2}$, as shown in Fig. 4, this operating method is a (DCMLI) capacitor voltage balancing scheme since C_3 is being charged during the part of the output voltage cycle between step angles θ_{C1} and θ_{D1}, and from $180°-\theta_{D1}$ to $180°-\theta_{C1}$, when the CHBMLI's output $V_{\mathrm{o,chb}}$ is positive, while C_2 is being charged during the part of the output voltage cycle between step angles $180° + \theta_{C1}$ and $180° + \theta_{D1}$, and from $360°-\theta_{D1}$ to $360°-\theta_{C1}$, when $V_{\mathrm{o,chb}}$ is negative.

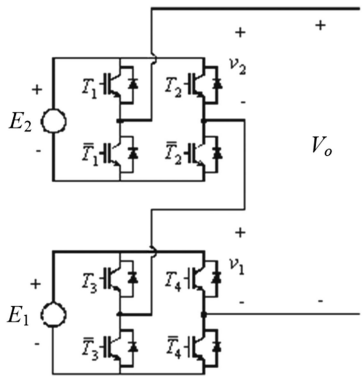

Fig. 3 *Cascaded five-level (two-cell) H-bridge MLI*

During these intervals, Fig. 4 shows the output (load) voltage V_{load} magnitude being equal to $|V_{\mathrm{o,chb}}|$ minus either $|v_{c3}|$ or $|v_{c2}|$ when either C_3 or C_2, respectively, is being charged from the sources of the CHBMLI; the waveform cycles when this occurs will be referred to as the recharging mode (RM) cycles. On the other hand, cycling the DCMLI through these same states but with $\theta_{D1} < \theta_{C1} < \theta_{C2} < \theta_{C3} < \theta_{C4} < \theta_{D2}$, so that it is in state (1, 0, 1, 0) only when $V_{\mathrm{o,chb}}$ is at 0, results in a net loss of charge from C_3 and C_2 during each cycle; these cycles will be referred to as the discharging mode (DM) cycles. It must be noted that while 13-level waveforms are produced during both of these operating modes, their shapes are slightly different. This is because each level of $V_{\mathrm{o,chb}}$ typically would not be equal in magnitude to each level of $V_{\mathrm{o,dci}}$, and during the RM the first positive level of $V_{\mathrm{o,dci}}$ produces the fifth positive level of V_{load}, while during the DM the first positive level of $V_{\mathrm{o,dci}}$ produces the first positive level of V_{load}. These two waveform shapes are exemplified in Fig. 4, where each level of $V_{\mathrm{o,chb}}$ is more than twice as large as each level of $V_{\mathrm{o,dci}}$. Note that in this simulation, v_{c2} is sampled and the decision is made to either change or not change operating mode, at the rising zero crossings of the V_{load} waveform. In contrast to the active balancing shown in Fig. 4, and to re-emphasise the need for proper control to maintain the voltages of C_2 and (by symmetry) of C_3, C_1 and C_4 also, at the desired magnitude of $E'/4$, Fig. 5 shows how the usual modulation of 1ϕ-DCMLI results in the discharge of C_3 and C_2 towards zero energy and voltage.

Minimising the total harmonic distortion (THD) of the inverter's output voltage is important for several well-known practical reasons. Hence, we optimised the RM waveform's THD, assuming in the basic case that $V_{\mathrm{o,chb}}$ has equal levels and $V_{\mathrm{o,dci}}$ has equal levels, rather than the general case of unequal levels. However, a waveform's actual THD (including all of its harmonics) is not a practical measure, whereas accounting for the lowest 50 of its harmonics – as specified by the IEEE 519-2014 standard [26] – is a practical and useful metric (to be referred to as THD_{50}), which was the objective function used for the optimisation. The process followed to find the requisite step angles and voltage levels (thus

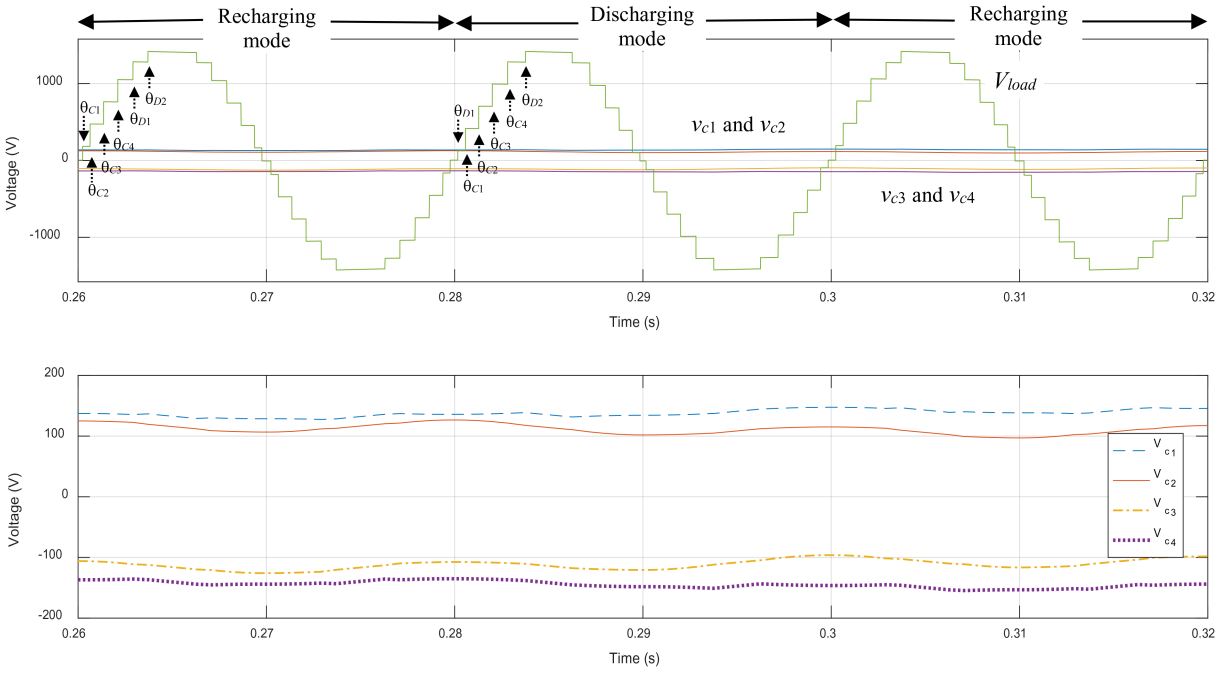

Fig. 4 *Simulated 13-level hybrid inverter output V_{load} (with waveform alternating between RM and DM cycle patterns), and capacitor voltages v_{c1}, v_{c2}, v_{c3} and v_{c4}*

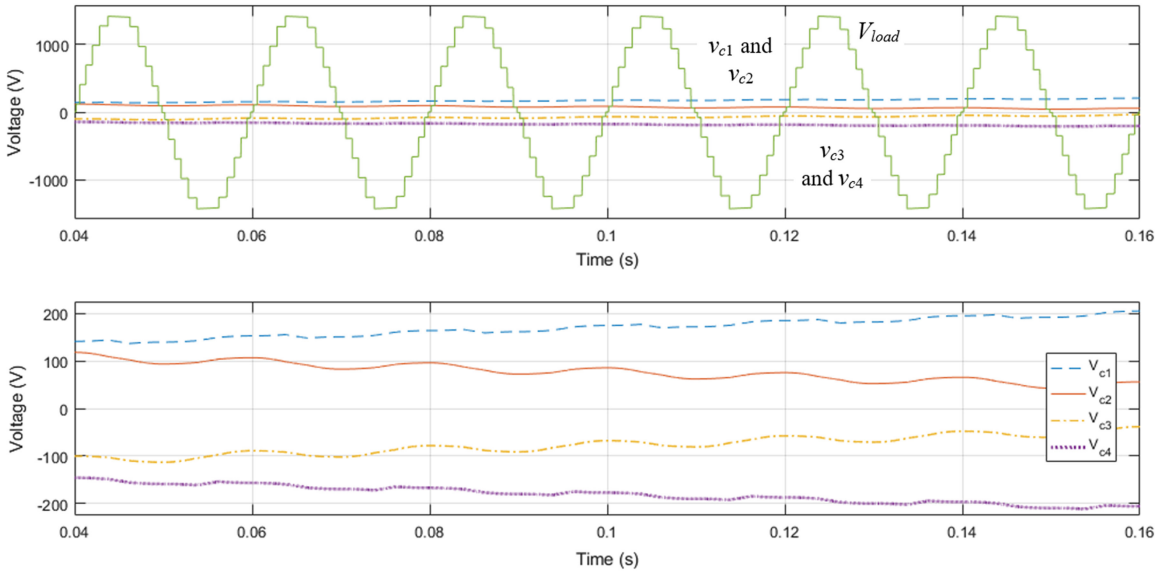

Fig. 5 *Simulated 13-level hybrid inverter output V_{load} (with waveform always in DM cycle pattern), and capacitor voltages v_{c1}, v_{c2}, v_{c3} and v_{c4}*

yielding E_i, $i = 1$ to 4, as a multiple of E') mimics what has been described in [27] and hence will not be detailed here.

Thus, steps at (θ_{C1}, θ_{C2}, θ_{C3}, θ_{C4}) = (3.29°, 11.4°, 24.3°, 37.9°) and (θ_{D1}, θ_{D2}) = (52.3°, 66.7°) are needed from the CHBMLI and the DCMLI, respectively, with the CHBMLI source values E_i = 2.30*E'/4, $i = 1$ to 4, to yield a THD_{50} of 5.161% for V_{load}; hence this result satisfies condition (2). Note that this THD value is for the ideal situation when the capacitor voltages of the DCMLI with semi-active front end remain constant, which is not true in practice so the actual distortion value will be a little different and is load dependent. For the DM waveform, steps at (θ_{C1}, θ_{C2}, θ_{C3}, θ_{C4}) = (10.3°, 22.9°, 35.9°, 50.7°) and (θ_{D1}, θ_{D2}) = (2.96°, 67.7°) are needed to yield a THD_{50} of 5.525%; again, this is the ideal-case value. Note that the THD_{50} values for both operating modes satisfy the IEEE 519-2014 standard limiting voltage distortion to 8% for ac sources that are at or below 1 kVrms and <5% for individual harmonics, which was the main motivation for focusing our study on the 13-level inverter case.

Finally, closed-loop control to alternate transistor switching commands between the two sets of step angles is needed to either actively recharge C_2 and C_3 or allow them to discharge. The approach taken was to sample the voltage v_{c2} once every output voltage cycle (implemented for the proof-of-concept testing by a sample-and-hold circuit based on the LF398 IC), then compare that sampled value to a voltage representing its desired value of E'/4 (implemented for the proof-of-concept testing using a circuit based on the LM211 IC with component values selected to provide a hysteresis band of 5% about that desired value, to make the hybrid inverter not switch between the operating modes too often). Since this control scheme is based on C_2's voltage value sampled once per cycle, it is actually controlling the energy lost or gained per cycle by that capacitor. Thus, allowing a ± 5% capacitor voltage deviation corresponds to allowing about a ± 10% change in its stored energy.

As an example for simulation purposes, to achieve a value of 960 Vrms (as a simple integer multiple of common single-phase voltages) for the output voltage's fundamental component, the DCMLI's E' was chosen to be 485 V, so that the CHBMLI's $E_i = E$ = 278 V (for optimal THD_{50}). Moreover, the resistive load value of 60 Ω was chosen, somewhat arbitrarily, to draw current of 16 Arms and power of 15.4 kW.

Regarding capacitor selection, recall that C_3 is being charged during the part of the output voltage cycle between step angles θ_{C1} and θ_{D1}, and from 180°−θ_{D1} to 180°−θ_{C1}, when the CHBMLI's output $V_{o,chb}$ is positive. This results in current of almost constant values ($4E-|V_{c3}|$)/R to ($E-|V_{c3}|$)/R supplying charge to C_3, causing voltage increases of about Δ_{t4}*($4E-|V_{c3}|$)/(R*C_3) to Δ_{t1}*($E-|V_{c3}|$)/(R*C_3) in $|V_{c3}|$ during the intervals Δ_{t4}, …, Δ_{t1}, when $4E-|V_{c3}|$, …, $1E-|V_{c3}|$, respectively, are applied in succession; so the ratios of voltage increase to applied voltage are $\Delta_{t4}/(R*C_3)$ to $\Delta_{t1}/(R*C_3)$, respectively. Clearly, these voltage increases are inversely proportional to capacitance value C_3, so information about E, E' (across DCMLI input) and (minimum) R, and the optimal-THD step angles can be used to select the value of C_3 sufficiently large to avoid its overcharging. As a rough estimate of C_3 (and thus C_2, C_1 and C_4 also), it was supposed (conservatively) that $4E-|V_{c3}|$ (with $|V_{c3}|$ about equal to E'/4) was applied for $2*(\Delta_{t4}+\Delta_{t3}+\Delta_{t2}+\Delta_{t1}) \cong 6.66$ ms within a 20 ms period, continuing the 13-level inverter simulation example. Then for $R = 60\ \Omega$, and a ratio of voltage increase to applied voltage no larger than 0.05 (i.e. 5%), C_3 needs to be >2 mF. In addition to the capacitors' value selection, their voltage rating should be chosen to be >E'/2, which is $|V_{c3}|$'s upper limit under symmetrical operation of the top and bottom halves of the DCMLI; this also helps avoid capacitor overcharging. Moreover, the closed-loop control should ensure that V_{c2} does not exceed, on a sample-per-cycle basis, the $E'/4 \pm 5\%$ values set as the (example) hysteresis band limits for switching between RM operation and DM operation. By symmetry, this closed-loop control limiting applies to V_{c3}, and also V_{c1} and V_{c4}.

The result of simulating this example hybrid inverter using Simulink®, with DCMLI capacitance values of 2 mF, desired DCMLI capacitor voltage (with feedback of V_{c2}) value set at 121.25 V and a hysteresis band of ± 6.0625 V are shown in Fig. 4, indicating alternations between the RM and DM, thereby balancing the voltages of the DCMLI's capacitors. It was noted that the six voltage levels during the increasingly positive quarter-cycle of the RM portions were $E-V_{c3}$, $2E-V_{c3}$, $3E-V_{c3}$, $4E-V_{c3}$, $4E+V_{c2}$ and $4E+V_{c2}+V_{c1}$, as expected from the analysis; while the six voltage levels during the increasingly positive quarter-cycle of the DM portions were V_{c2}, $E+V_{c2}$, $2E+V_{c2}$, $3E+V_{c2}$, $4E+V_{c2}$, $4E+V_{c2}+V_{c1}$, also as expected.

An analysis was then performed to determine the amplitudes of this waveform's harmonic components during RM operation and during DM operation as a percentage of the fundamental components' amplitudes; these are graphed in Fig. 6. Moreover, the THD_{50} of the first RM cycle shown in Fig. 4 was determined to be 5.257%, while the THD_{50} of the DM cycle shown in Fig. 4 was determined to be 6.175%. Note that the deviation from the ideal THD_{50} values is to be expected due to the capacitor voltages' variation over time and the non-negligible deviation from their desired values.

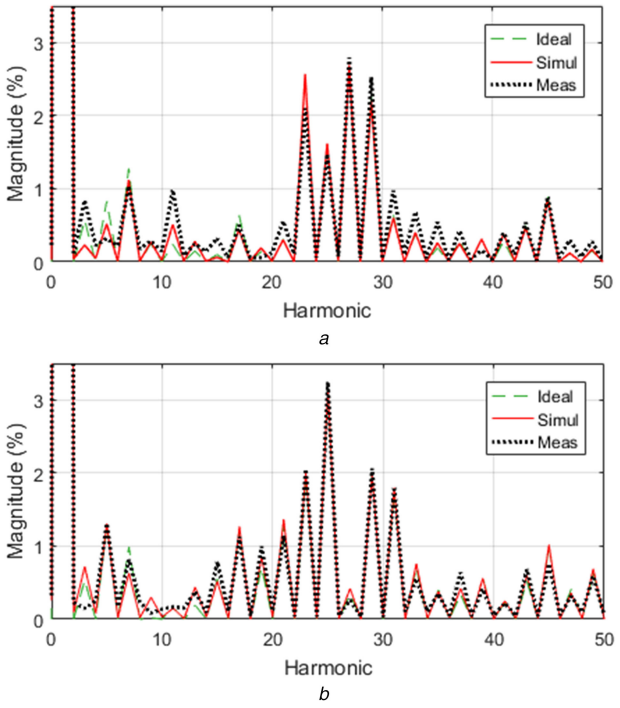

Fig. 6 *Normalised harmonic spectra of the V_{load} waveforms obtained for the ideal, simulated and measured cases*
(a) For RM operation, ***(b)*** For DM operation

3.2 11-level waveform case

Using the IEEE 519-2014 standard for ac voltage sources that are at or below 1 kVrms to guide our hybrid inverter design, it was found that a seven-level 1ϕ-CHBMLI connected to a five-level 1ϕ-DCMLI producing a 11-level output voltage is also satisfactory when its waveform is ideal with constant levels. While this design is slightly simpler and less costly than the 13-level hybrid inverter described previously, its output voltage's THD_{50} may not satisfy IEEE 519-2014 under real-world operating conditions with non-idealities present and using reasonably sized capacitors, which lead to non-negligible reduction of their voltages when transferring energy to the (rated) load. However, the results that were obtained for this design are also presented herein for completeness.

For this case, the CHBMLI part is operated as usual to produce a voltage with seven levels (corresponding to step angles θ_{C1}, θ_{C2}, θ_{C3}), while the five-level DCMLI is operated identically to the 13-level waveform case during the RM. Thus, steps at (θ_{C1}, θ_{C2}, θ_{C3}) = (3.85°, 16.7°, 31.6°) and (θ_{D1}, θ_{D2}) = (50.5°, 65.9°) are needed, with CHBMLI source values $E_i = 2.51*E'/4$, $i = 1$ to 3, to yield a THD_{50} of 6.648%; again, this is an ideal-case distortion value. Then the DM waveform's THD_{50} was similarly optimised but with the constraints that its fundamental frequency component should have the same amplitude as the THD_{50}-optimal RM 11-level waveform's fundamental frequency component, and with $E_i = 2.51*E'/4$. For the DM waveform, steps at (θ_{C1}, θ_{C2}, θ_{C3}) = (13.65°, 28.32°, 47.75°) and (θ_{D1}, θ_{D2}) = (2.41°, 66.8°) are needed to yield a THD_{50} of 7.232%; again, this is an ideal-case value. Note that this design does not provide much margin with respect to achieving acceptable THD, based on IEEE 519-2014, especially during DM operation when the margin is only about 0.7% of THD_{50} versus a margin of about 2.4% of THD_{50} for the 13-level inverter case. Simulation results were again obtained to back up the above theoretical results; the THD_{50} of the RM cycle just before a DM cycle was determined to be 6.602%, while the THD_{50} of the DM cycle was determined to be 7.542%.

3.3 Discussion

It should be noted that the voltage balancing method as proposed above is different from the typical one that uses redundant switching states. That method usually selects two switch states in one period to output the same voltage level, whereby one switch state charges the dc-link capacitors and the other switch state discharges them. Consequently, over one period the capacitor voltages can keep their balance by first discharging and then charging: an example of this method is the phase-shift pulse-width modulation proposed for flying-capacitor multilevel converters [6]. While this approach can also be taken for the proposed hybrid inverter, e.g. by having some of the CHBMLI sources be equal to $E'/2$ (to force capacitor recharging) and the rest be equal to $E'/4$ (to provide redundant states), our investigation in conjunction with this work indicated it has at least two drawbacks: it will result in higher THD_{50} values for the same number of output voltage waveform levels, and it seems to require some transistors to be switched more than once each period thereby incurring higher device power losses.

Another point of note is that the recharging scheme described above, with $\theta_{D1} < \theta_{C1}$, allows for the longest intervals of inner capacitor charging. However, possible variants of this scheme include designs with θ_{D1} re-positioned so that either $\theta_{C1} < \theta_{D1} < \theta_{C2}$, or $\theta_{C2} < \theta_{D1} < \theta_{C3}$, or $\theta_{C3} < \theta_{D1} < \theta_{C4}$. Although these designs would increasingly shorten the intervals of inner capacitor charging, the resulting (ideal case) THD_{50} values could be a little lower than for the proposed step-angle design due to the different RM waveform shapes.

Although the main motivation for this described study was for applications with (ideally) a fixed modulation index and a load power factor (PF) that is close to unity, some effort was made to determine how the proposed hybrid converter and hysteretic control scheme would behave when the modulation index and/or load PF deviate(s) from the assumed value(s).

3.3.1 Variation of modulation index: Regarding converter performance as the modulation index (defined as the ratio of the phase voltage amplitude to the maximum inverter output voltage) $m_1 = V_1/(E' + 4E)$ varies, if so desired. The proposed design can be viewed as for the optimal modulation index m_1* (equal to almost 1 for the 13-level case). Variation of the index in a moderate range (e.g. $0.9 \leq m_1/m_1* \leq 1.1$), if the application requires it, still achieves voltage balancing using the proposed alternating-mode hysteretic control method. However, the THD of the resulting waveform will increase as the voltage levels are fixed while the step angles of the recharging waveform and the discharging waveform are adjusted to produce the desired modulation index. There is considerable freedom in designing the step angles even with this constraint. The proposed approach is to mimic what has been done to select the step angles of the discharging waveform for the baseline case with THD_{50} minimisation as the design objective. Once these step angles have been determined for a range of modulation index values, these can be used online via a lookup table during the converter's operation. Fig. 7 shows the optimal THD_{50} and corresponding step angles calculated at modulation indices of 0.9, 0.95, 1 (optimal), 1.05 and 1.1. Note that at the lower end of this range, the largest step angle reaches 90°, while at the upper end, the THD_{50} reaches 8%. The waveforms look similar to those for the m_1* case except that the durations of the various levels vary, especially the top-most and bottom-most levels.

3.3.2 Variation of load PF: Regarding voltage balancing as the load PF varies, although the control design proposed is primarily for a near-unity PF load. Simulation results indicate that this is still achieved using the proposed scheme as the load PF angle varies between −90° and +85° (Figs. 8*a* and *b*), although the THD of the resulting waveform typically increases. However, purely inductive loads yield unacceptable behaviour (especially for smaller inductances) due to resonance effects. For the moderately-leading PF case, the leading current crossover yields an extra step in the RM voltage waveform as shown in Fig. 8*c* for the PF angle of −18.19° (0.95 PF leading). For the moderately-lagging PF case, the lagging current crossover produces extraneous voltage pulses in the RM voltage waveform when the PF angle increases beyond θ_{C1}

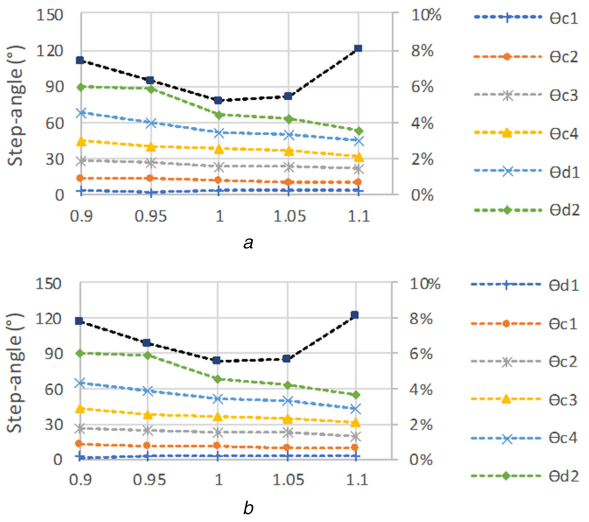

Fig. 7 *Step angles and corresponding (optimal) THD_{50} at various modulation indices for*
(a) RM waveform, ***(b)*** DM waveform

(3.2885°) as shown in Fig. 9*a* for the PF angle of 18.19° (0.95 PF lagging); this is unsurprising as it also happens with the 'pure' CHBMLI topology under similar conditions [27]. Research is ongoing on control designs that will ameliorate those effects; that work will be reported on when completed.

4 Experimental results

A hardware/software platform (see photograph of the test setup in Fig. 10) was used as a low-power prototype to experimentally verify the theory and simulations presented above. The control signals for the five-level 1ϕ-DCMLI and the nine-level 1ϕ-CHBMLI were generated using a National Instruments Digital Electronics FPGA Board with a Xilinx Spartan-3E chip that was programmed using LabVIEW software. The prototype inverters, which had been fabricated as two separate printed circuit boards for previous work, were connected as diagrammed in Fig. 1 (the CHBMLI taking the place of dc source V_{hb}).

As an example, E' was chosen to be 48 V, so that $E_i = E = 27.6$ V, these voltage values being constrained by the available power supplies. We performed tests of the 13-level waveform optimal-THD_{50} (for recharging) case with a single dc power supply applying 48 V across the five-level DCMLI's four pairs of capacitors (each of the electrolytic-type capacitors being 1 mF), four other dc power supplies each providing about 27.6 V to each H-bridge cell, and a load resistance of 45 Ω, thus yielding output voltage with fundamental component of 95.0 Vrms, load current (I_{load}) of 2.13 Arms and output power of 202 W. Correspondingly, the sample-and-hold plus comparator circuit (also fabricated as a printed circuit board, with a few adjustable resistors to accommodate different threshold and hysteresis band settings) processing the DCMLI capacitor voltage v_{c2}, was configured to output a binary output indicating if v_{c2} was either less than or more than 12 V with a hysteresis band having upper limit of 12.57 V and lower limit of 11.43 V (as constrained by the standard component values used). This mode command signal was then input to the FPGA board, which caused the code to output either the transistor switch signals to enable recharging of the DCMLI inner capacitors, or the transistor switch signals to allow discharging of those capacitors.

The resulting 13-level inverter output (V_{load}) waveform, with the step angles as designed in Section 3.1 to achieve minimal THD_{50}, is shown as Fig. 11*a*, along with the load current waveform and the output of the sample-and-hold plus comparator circuit commanding either recharging (when high) or discharging (when low) operation. Fig. 11*b* shows the transition from RM to DM of operation in greater detail, while Fig. 11*c* shows the transition from DM to RM of operation in greater detail. As was the case with the

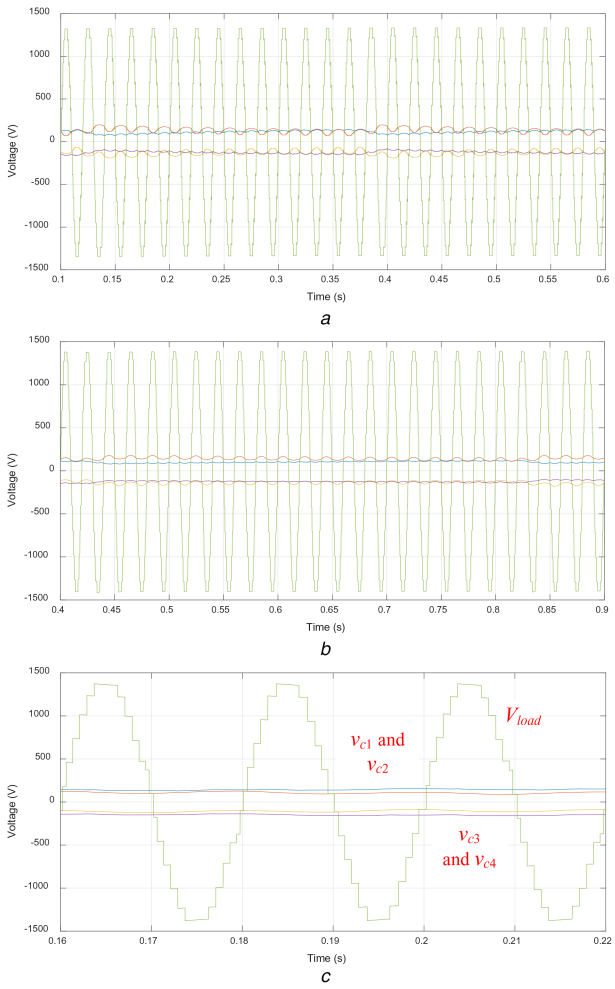

Fig. 8 *Simulation and test results for the 13-level hybrid inverter with various load PFs*
(a) 0 PF leading, ***(b)*** 0.1 PF lagging, ***(c)*** 0.95 PF leading

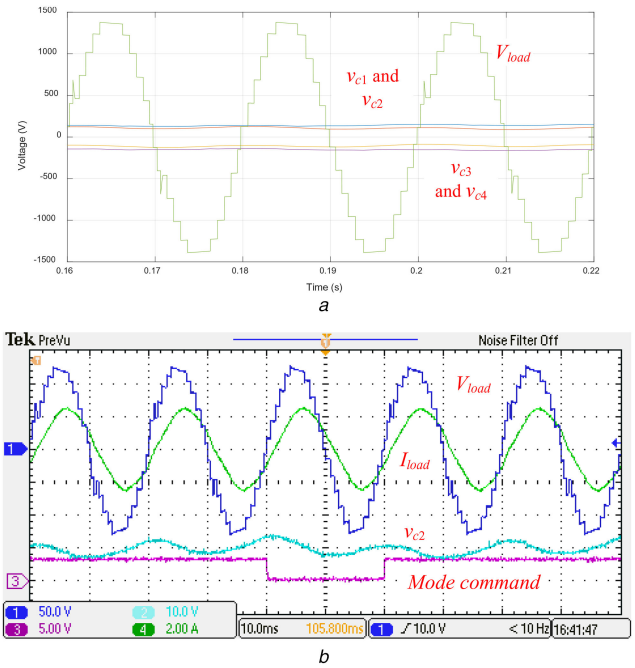

Fig. 9 *Simulation and test results for the 13-level hybrid inverter with 0.95 lagging PF load*
(a) Simulated transition from RM to DM, and back to RM, ***(b)*** Measured transition from RM to DM, and back to RM

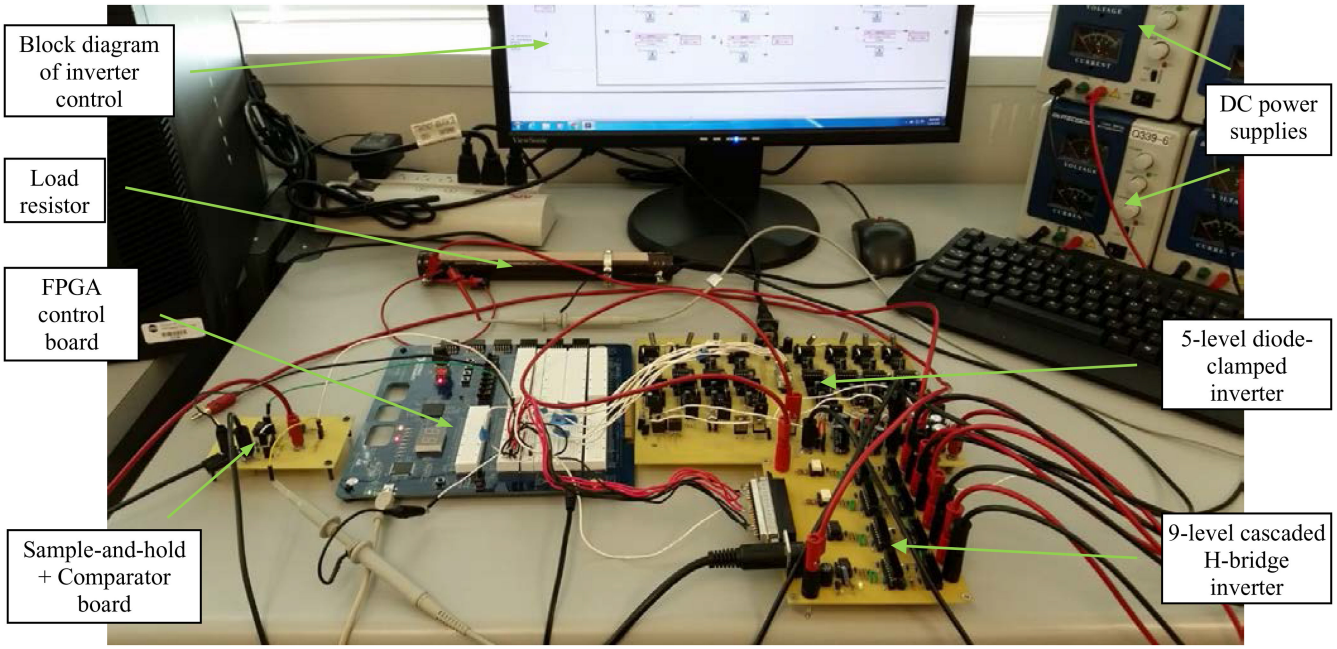

Fig. 10 *Photograph of 13-level hybrid inverter (five-level 1ϕ-DCMLI with nine-level 1ϕ-CHBMLI) lab prototype, sample-and-hold plus comparator board and FPGA board*

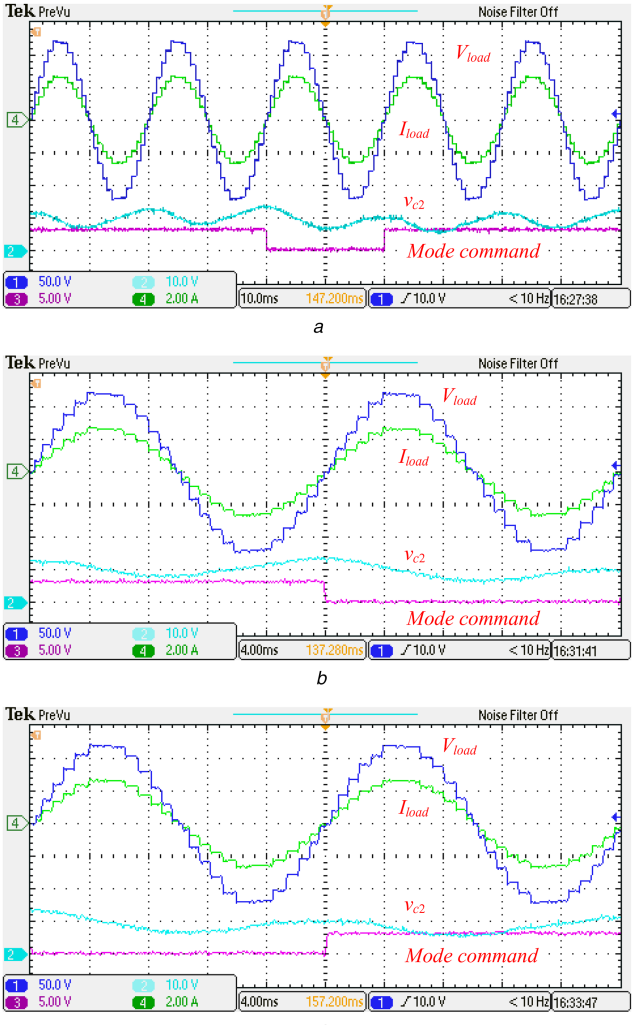

Fig. 11 *Oscilloscope traces of the 13-level hybrid inverter's V_{load}, load current, V_{c2}, and operating mode command*

(a) Transition from RM to DM, and back to RM operation, ***(b)*** Zoom-in of transition from RM to DM operation, ***(c)*** Zoom-in of transition from DM to RM operation

simulation results, one cycle of the DM was sufficient to cause a switch to the RM, whereas it took several cycles of the RM to cause a switch to the DM. In Fig. 12, the variations of capacitor voltages v_{c2} and v_{c3} are shown in greater detail; in particular, it can be observed that $|v_{c2}|$ and $|v_{c3}|$ are similar to each other (with a 180° phase difference). Moreover, that $v_{c2} = 13.5$ V at the transition from RM to DM, while $v_{c2} = 10.0$ V at the transition from DM to RM. The THD_{50} of the recharging cycle shown in Fig. 11*b* is 5.507%, whereas the THD_{50} of the discharging cycle shown in Fig. 11*b* is 6.366%; the THD_{50} of the recharging cycle shown in Fig. 11*c* is almost the same as for the corresponding cycle in Fig. 11*b*. Note that while the simulated control scheme and the implemented control scheme both have the switch-over between modes occurring at the rising zero crossings of the output voltage waveform, an alternative is to programme the switch-over to occur in the middle of the top levels of the output voltage waveform (i.e. at the angle of 90°) to reduce the potentially disruptive (distortive) effects of any real-world control circuit delays on transistor switching.

In Table 1, we compare the measured THD_{50} values to the corresponding theoretical (ideal case) and simulated values. In Fig. 6, we compare the amplitudes of the harmonic components for the measured RM waveform cycle, and for the measured DM waveform cycle, to the corresponding theoretical (ideal case) and simulated values. As expected, even harmonics are present in the simulated and measured waveforms due to the decrease in voltages across the discharging capacitors, thus causing the waveforms to not be quarter-wave symmetric as in the ideal case. Moreover, the harmonic spectra for the output voltages obtained during RM of operation for the ideal, simulated and measured cases are plotted as Fig. 6*a* to provide better insight, while the harmonic spectra for the output voltages obtained during DM of operation for the ideal, simulated and measured cases are plotted as Fig. 6*b*. Thus, Table 1 and Figs. 4, 6, 11, 12 indicate that the experiments verified the analysis and the simulations, including the test result shown in Fig. 9*b* for a load with PF angle of 18.19° (0.95 PF lagging).

5 Conclusions and future work

This paper has described the operation of a hybrid inverter comprised of a five-level 1ϕ-DCMLI with a semi-active front end connected in series with either a nine-level 1ϕ-CHBMLI or a seven-level 1ϕ-CHBMLI to produce a staircase waveform with either 13-levels or 11-levels, respectively. The key contribution is a

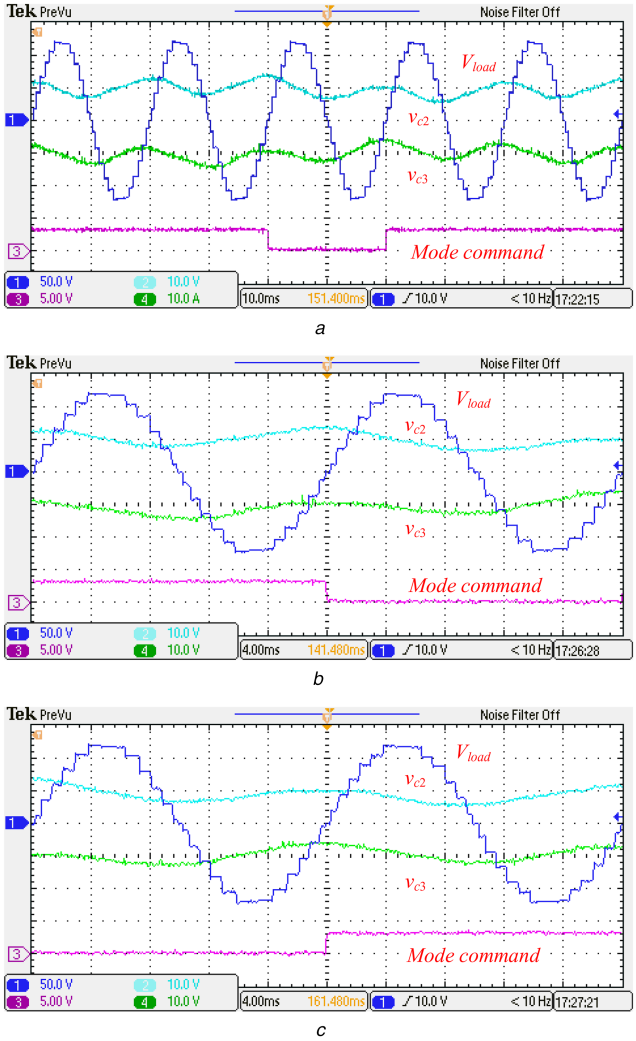

Fig. 12 *Oscilloscope traces of the 13-level hybrid inverter's V_{load}, V_{c2}, V_{c3}, and operating mode command*

(a) Transition from RM to DM, and back to RM operation, ***(b)*** Zoom-in of transition from RM to DM operation, ***(c)*** Zoom-in of transition from DM to RM operation

Table 1 Comparison of output voltage THD (THD_{50}) values for the 13-level hybrid inverter

	THD_{50} of 13-level recharging cycle, %	THD_{50} of 13-level discharging cycle, %
ideal case	5.161	5.526
simulated	5.257	6.175
measured	5.507	6.366

novel fundamental-frequency modulation scheme for the DCMLI's switches so as to charge up its inner dc-link capacitors from the CHBMLI's dc sources, and thereby achieve capacitor voltage balancing via an alternation between a RM and a DM based on capacitor voltage feedback with a hysteresis band. Both simulation and experimental results have been presented herein to substantiate this hybrid-topology inverter's good performance when operated using the proposed modulation and feedback control schemes at an optimal modulation index with unity PF loads. Furthermore, the scheme also achieves capacitor voltage balancing for modulation indices that span at least 10% above and below the optimal modulation index, and for a wide range of load PFs, albeit at the cost of increased output voltage distortion.

While (fundamental-frequency) staircase modulation of the DCMLI has the advantage of lower switching losses and higher power efficiency compared with (high-frequency) pulse-width modulation, the accompanying drawback is it requires large capacitances to prevent overcharging, and also too-rapid discharging, of the capacitors due to the long charging and discharging durations. Future work will consider pulse-width modulation of the hybrid inverter, especially for variable instead of fixed modulation index applications, and for supplying lagging PF loads.

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