Design of Low Power Magnitude Comparator

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***Abstract*— A low power two bit magnitude comparator has been proposed in the present work. The proposed magnitude comparator using the technology of coupling has been compared with the basic comparator circuit. The performance analysis of both the different comparators has been done for p ower consumption, delay and power delay-product (PDP) with VDD sweep. The simulations are carried on Mentor graphics (ELDO Spice) using 90nm CMOS technology at 1 V supply. The simulation results of the coupled magnitude comparator circuits is in good agreement in terms of power consumption at percentage of 60.26% in greater than function and 56.14% in lesser than f unction and 59.48% in equals to function comparators.**

Keywords*— magnitude comparator, full adder, PTL logic, GDI technique, CMOS, Domino logic.

I. INTRODUCTION

Now a days low power designing has become the need of an hour. As there is high demand of the fast electronic devices, focus is made more on optimizing the speed and consumption of less amount of power and decreasing the size of the chip [1]-[9]. A comparator is a circuit which makes use of various logic gates such as AND, NOR and NOT to com pare the various digital inputs.

A magnitude comparator (Fig.1) is a typ e of e lectronic device that take inputs in t he form of bi nary numbers and determines whether the one of the tw o number is less than, greater than or equal as compared to the other. There are many applications of m agnitude comparator including: microprocessor i.e. used for purp ose of decoding and for encryption devices.

Now the s peed of system can be managed very easily by reducing the l ength of the tra nsistor .The size is not decreased keeping in mind of the explosive factor .The designer produces a system consuming low amount of power keeping in mind of the fact that it is stable. Therefore we prefer Complementary Metal Oxide Semiconductor (CMOS). CMOS is a technology consisting of the integrating network i.e. combination of both n-MOS as well as p-MOS.

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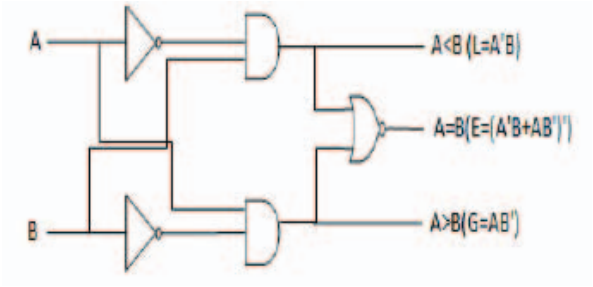

Fig. 1. Simple diagram of comparator using logic gates.

II. 2-BIT MAGNITUDE COMPARATOR DESIGN

A. Existing Design

Let us assume two binary numbers i.e. A and B, thus the most common way to represent our functions are A less than B(L), A greater than B(G), A equal to B(E). Thus the very first work is to find out the most significant bit.

Table I. TRUTH TABLE OF 2-BIT COMPARATOR

A1	A0	B1	B0	E	L	G
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0

Thus by studying this truth table, we can easily see that if A bit is greater than the bit B than G will be high and if A is

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less than the B then L will be high and if both the bits are equal then E will be high.

So by using above table (Table I), we can easily design a 2-bit magnitude comparator by using the full adder which consist 4-X-or gate, 2-AND gate, 2-MUX, 2-NOT gate. If we apply input to the X-or gate in the circuit, it will get inverted and starts acting like X-NOR gate with respect to the applied inputs. Thus to make the use of less number of transistors in following circuit, X-OR gets replaced by the X-NOR gate. Thus by using this logic diagram we can easily design a 2-bit magnitude comparator by using GDI technology.

B. Existing Circuits of 2 - Bit Comparators

The exiting circuit for 2-bit magnitude comparator is given in Fig. 2.1, Fig. 2.2 and Fig. 2.3.

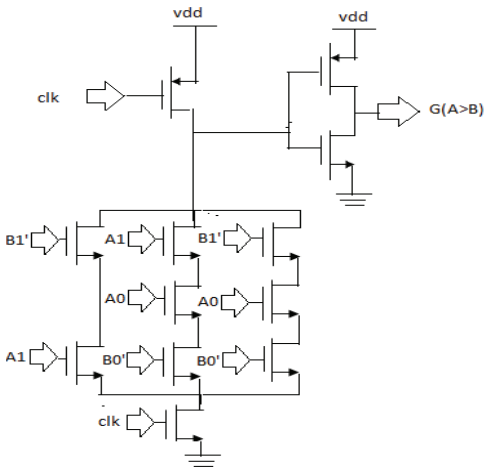

Fig 2.1.Greater than fuction circuit

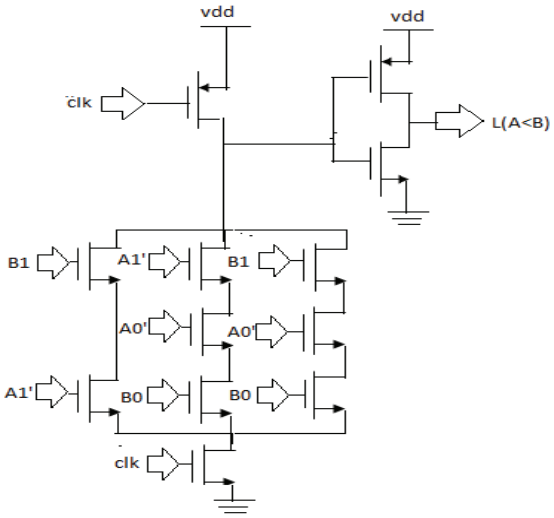

Fig 2.2 Less than fuction circuit

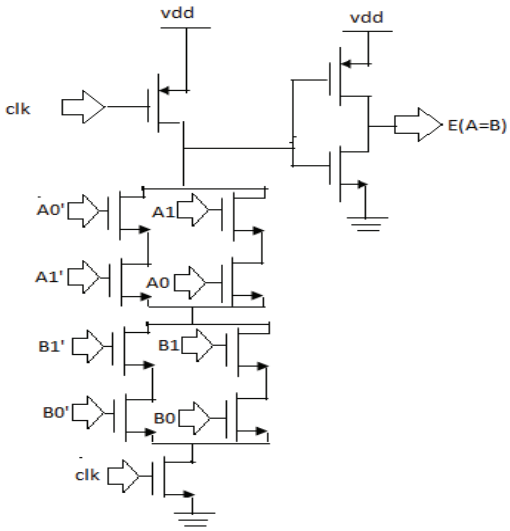

Fig 2.3 Equal to function circuit

C. Circuit Proposed

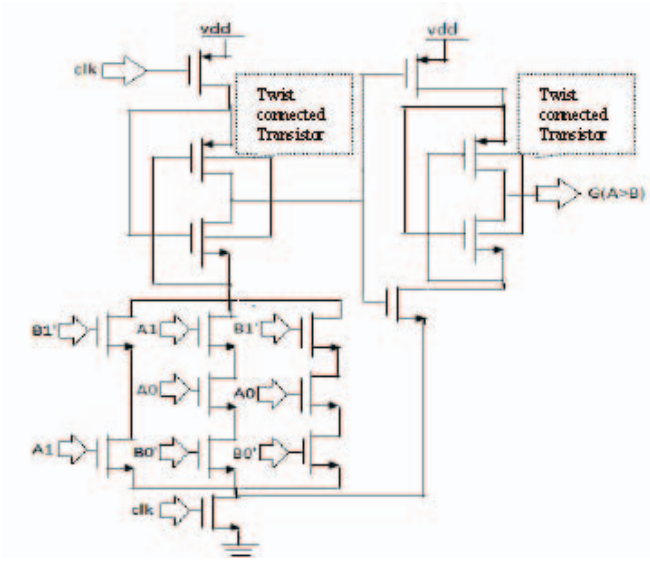

Fig 2.4 Coupler greater than function

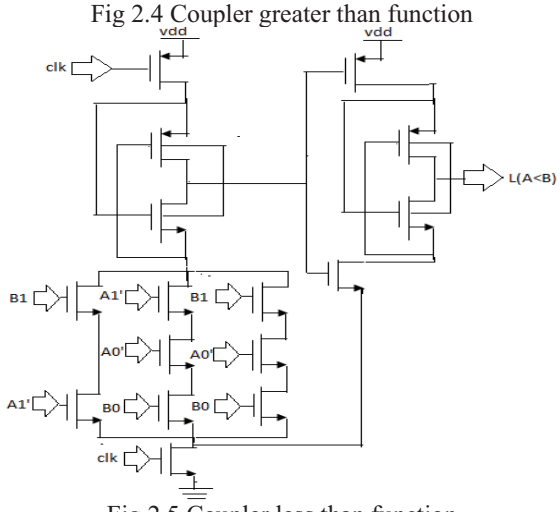

Fig 2.5.Coupler less than function

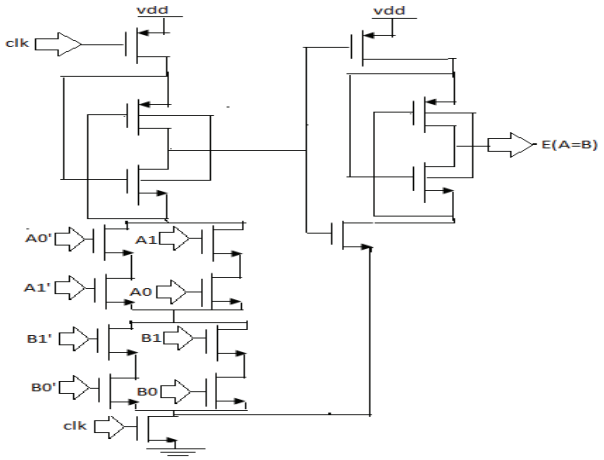

Fig 2.6.Coupler equal to function

The circuit for less than, greater than and equal to output is given in Fig. 2.4, Fig. 2.5 and Fig. 2.6 respectively. Three major sources to power dissipation in digital circuits are given in eq.1.

$$P = p_t f_c \left(C_L V_{DD} V_{sig}\right) + \left(I_{SC} V_{DD}\right) + \left(I_{leakage} V_{DD}\right) \quad (1)$$

Where $p_t f_c \left(C_L V_{DD} V_{sig}\right)$ = switching power,

$I_{SC} V_{DD}$ = short circuit power

$I_{leakage} V_{DD}$ = Leakage power.

For the dynamic power component $p_t f_c \left(C_L V_{DD} V_{sig}\right)$, every input transition between logic states '0' and '1' leads to switching activity at the output depending on the in put combinations. If the sw ing level of output signal is re duced then the dynamic power component is also reduced. If the swing level of signal V_{DD}, at output node is reduced then the power from first component in (1) is re duced by a ratio of $\left(\frac{V_{sig}}{V_{DD}}\right) \times 100$ %.

In the proposed circuit of comparator, a small swing domino logic with twisted transistor is incorporated. By this method the swing and so t he power consumption of the circuit get reduced. By the arrangement of the twisted transistors, the voltage at node 'OUT' should be lower than VDD even though it was at a logic level '1' in the pre-charge mode. The small-swing level of output at first stage and then at second stage reduces the dynamic power as compared with the full swing level.

III. Result and Analysis

In this section, Power, Delay and Power-delay Product analysis has been done. From the analysis, It is evident that the proposed comparator design consumed much less power compare to the basic design. Analysis of power, delay, power-delay product is given in Table II, III and IV respectively. In the last, a comparison of the simulation results with the existing low power comparator circuit designs is given in Table V to verify the leading result of the presented work. Graphical comparison of results for the given analysis are shown in Fig. 3.1.1, Fig. 3.1.2, Fig. 3.1.3, Fig. 3.2.1, Fig. 3.2.2, Fig. 3.2.3, Fig. 3.3.1, Fig. 3.3.2 and Fig. 3.3.3 respectively.

Table II. POWER ANALYSIS

VDD (Volts)	POWER (pW)					
	Greater than function		Lesser than function		Equals to function	
	BASIC	PROPOSED	BASIC P	ROPOSED	BASIC	PROPOSED
0.6	183.0187	48.8218	84.7116	48.8218	128.2382	80.7097
0.7	98.681	59.9012	105.9648	59.9012	164.2124	102.8573
0.8	121.6328	73.5868	130.6005	73.5868	205.4119	127.4835
0.9	149.0449	90.3958	159.9959	90.3958	253.0311	154.4954
0.1	183.0187	110.2903	196.4218	110.2903	309.1379	183.9015

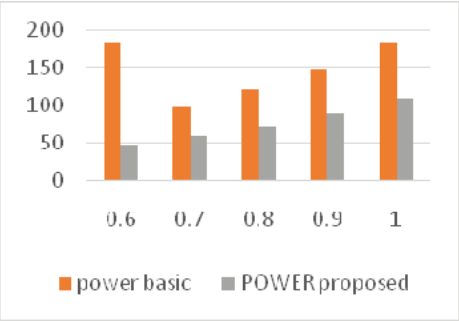

Fig. 3.1.1. Greater than function power

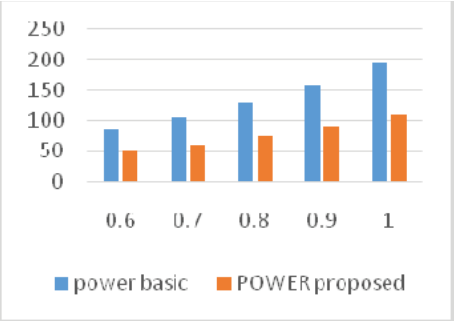

Fig. 3.1.2. Lesser than function

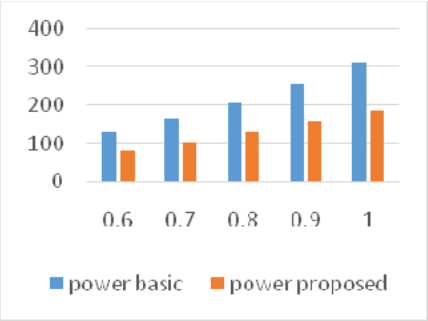

Fig. 3.1.3. Equals to function

Table III. DELAY ANALYSIS

VDD (Volts)	DELAY (ns)					
	Greater than function		Lesser than function		Equals to function	
	BASIC	PROPOSED	BASIC P	ROPOSED	BASIC	PROPOSED
0.6	51.241	53.098	50.999	53.098	1.3955	302.15
0.7	50.673	51.746	50.694	51.746	0.9688	301.15
0.8	50.476	51.267	50.484	51.267	0.75162	300.84
0.9	50.357	50.974	50.360	50.974	0.62329	300.65
1	50.273	50.745	50.287	50.754	0.53649	300.53

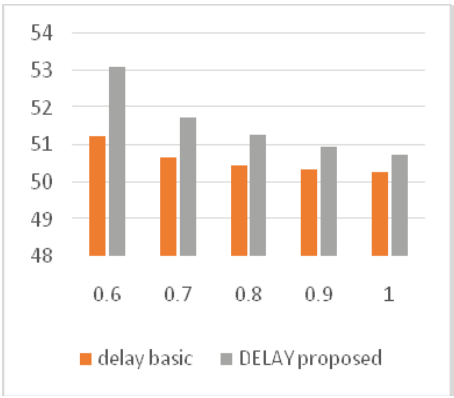

Fig. 3.2.1. Greater than function delay

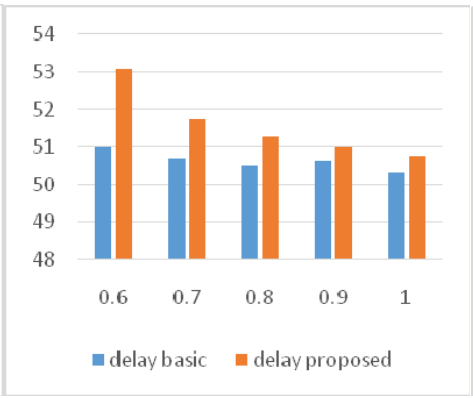

Fig. 3.2.2. Lesser than function delay

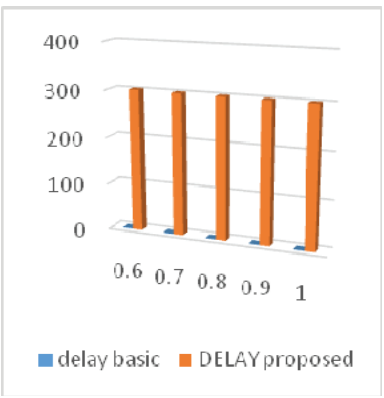

Fig. 3.2.3. Equals to function delay

Table IV. POWER-DELAY PRODUCT ANALYSIS

VDD (Volts)	PDP					
	Greater than function		Lesser than function		Equals to function	
	BASIC	PROPOSED	BASIC P	ROPOSED	BASIC	PROPOSED
0.6	9378.061	2592.34	4320.207	2592.34	178.9564	24386.44
0.7	5000.462	3099.647	5371.78	3099.647	159.089	30975.48
0.8	6139.537	3772.574	6593.236	3772.574	154.3917	38352.14
0.9	7505.454	4607.836	8100.592	4607.836	157.7118	46449.04
1	9200.899	5596.681	9877.463	5596.681	165.8494	55267.92

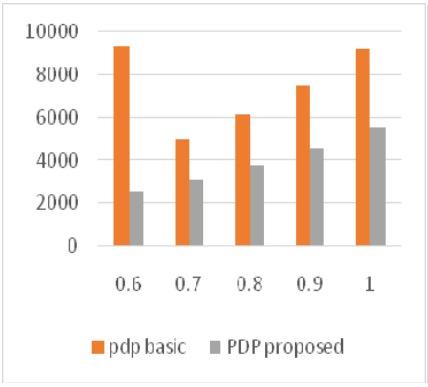

Fig. 3.3.1. Greater than function (PDP)

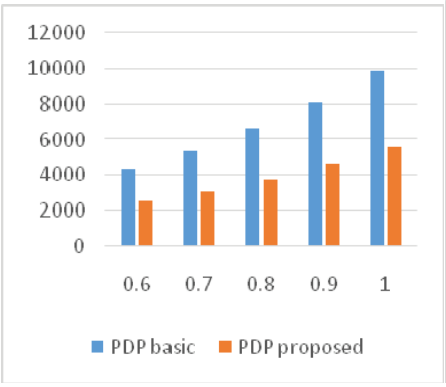

Fig. 3.3.2. Lesser than function (PDP)

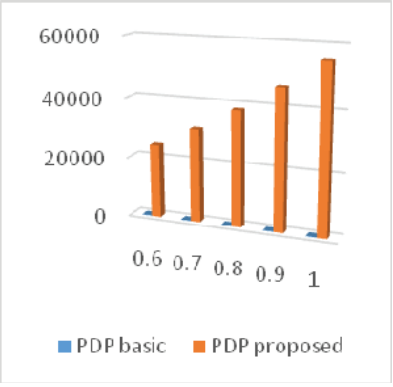

Fig. 3.3.3. Equals to function (PDP)

Table V. COMPARISON TABLE

VDD (Volt)	POWER CONSUMPTION OF VARIOUS HIGH PERFORMANCE TECHNIQUES							
	BASIC CMOS ($\times 10^{-6}$)	FULL ADDER[7] ($\times 10^{-6}$)	TRANSMISSION GATE [5] ($\times 10^{-6}$)	HYBRID FULL ADDER [3] ($\times 10^{-6}$)	PTL [5]($\times 10^{-6}$)	DOMINO [6] ($\times 10^{-6}$)	HYPBRID PTL/CMOS [3] ($\times 10^{-6}$)	This Work ($\times 10^{-12}$)
0.6	0.5	10.6	3.8	1.4	0.8	5.3	0.53	80.7097
0.8	1.3	33.4	10.7	4.1	3.7	22.8	1.41	127.4835
1	4.8	85.5	23.4	10.2	10.4	70.6	4.43	183.9015

IV. CONCLUSION

The concern of the design is power and delay optimization. In the present by increasing the value of VDD the power also goes on increasing but has much less compare to the existing designs. The simulation results of the coupled magnitude comparator circuit are in good agreement in terms of power consumption at percentage of 60.26%, 56.14% and 59.14% respectively for 'greater than function', 'lesser than Function' and 'equals to function' compare to basic Comparator design. Also the other parameter shows the improvement in the ir values.

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