High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop

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***Abstract*—Positron emission tomography (PET) is a nuclear functional imaging technique that produces a three-dimensional image of functional organs in the body. PET requires high resolution, fast and low power multichannel analog to digital converter (ADC). A typical multichannel ADC for PET scanner architecture consists of several blocks. Most of the blocks can be designed by using fast, low power D flip-flops. A preset-able true single phase clocked (TSPC) D flip-flop shows numerous glitches (noise) at the output due to unnecessary toggling at the intermediate nodes. Preset-able modified TSPC (MTSPC) D flip-flop have been proposed as an alternative solution to alleviate this problem. However, the MTSPC D flip-flop requires one extra PMOS to suspend toggling of the intermediate nodes. In this work, we designed a 7-bit preset-able gray code counter by using the proposed D flip-flop. This work involves UMC 180 nm CMOS technology for preset-able 7-bit gray code counter where we achieved 1 GHz maximum operation frequency with most significant bit (MSB) delay 0.96 ns, power consumption 244.2 µW (micro watt) and power delay product (PDP) 0.23 pJ (Pico joule) from 1.8 V power supply.**

Keywords—D flip-flop, 7-bit Gray code counter, TSPC D flip-flop, modified TSPC D flip-flop.

I. INTRODUCTION

As CMOS technology growing towards nanometer scale, the performance of any electronics devices become challenging task because there are several parameter gets affected due to scaled down the devices, researchers have developed various types of logic circuits to increase the performance of a electronics systems [1-4]. One of the most important categories of logic family which is required for design any types of electronics system is sequential logic circuits. D flip-flops (DFF) are the most important basic building blocks of any digital very large scale integrated circuits (VLSI).The performance of DFFs directly affect the overall performance of the digital circuits. In order to obtain higher performances of the circuits, researchers have developed different types of DFFs [5-11]. These structures can be divided into static and dynamic categories, however dynamic DFFs has better performance in terms of power delay product (PDP). D flip-flops finds application in low power analog to digital converter (ADC) in different blocks of Multichannel ADC for PET scanner [12]. Static D flip-flop is very slow when it has to be used in a MHz frequency range [1], so to avoid that, a TSPC D flip-flop in [13] is selected. However there are numerous glitches in the intermediate nodes, due to that the overall performance of the circuit gets degraded.

In this paper we proposed a modified positive edge triggered TSPC D flip-flop (MTSPC DFF) which is some extended version of positive edge triggered TSPC D flip-flop. The modified TSPC DFF suspends the toggling of the intermediate glitches of nodes. As a result, the overall performance of the circuit is improved.

The paper is organized as the following manner. In section II we describe the operation of the proposed positive edge triggered MTSPC D flip-flop and positive edge trigged TSPC D flip-flop. The maximum frequency of operation for both the proposed positive edge triggered MTSPC DFF and positive edge triggered TSPC DFF is also described in section II. In section III the simulation results are presented for both the proposed positive edge triggered MTSPC DFF and positive edge triggered TSPC DFF based 7-bit asynchronous gray code counter. Finally, in section IV conclusions are drawn.

II. THE PROPOSED D FLIP-FLOP

In this section the existing positive edge triggered TSPC DFF and the proposed positive edge triggered MTSPC DFF

are presented. The proposed MTSPC DFF is not only consumed low power but also it has a higher maximum frequency of oscillation and PDP compared to TSPC DFF, as we will discuss shortly.

A. Operation of the existing TSPC DFF

In the existing positive edge triggered TSPC D Flip-Flop in the Fig. 1, when the clock signal Clk is LOW, the input is isolated from the output Qb, since the node B pre-charged to HIGH, and Qb maintains its older value. When Clk is HIGH, node B will not be affected. Therefore when Clk is stable at either HIGH or LOW, the input is isolated from the output. When Clk makes a LOW-to-HIGH transition, the Qb will latch the complement of the input and Q will pass the input to the output. When the preset input (RESET) is LOW the preset PMOS will be ON and Qb maintains its value HIGH as long as RESET is LOW.

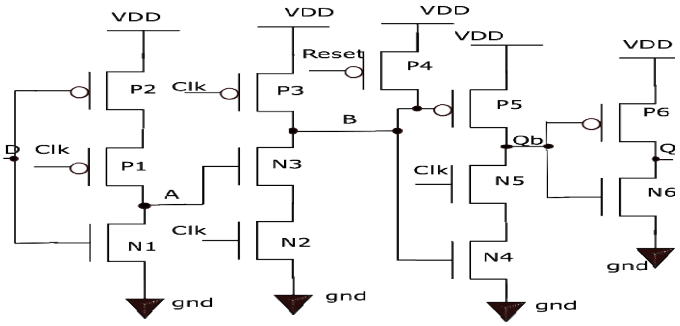

Fig. 1. Positive edge triggered TSPC DFF.

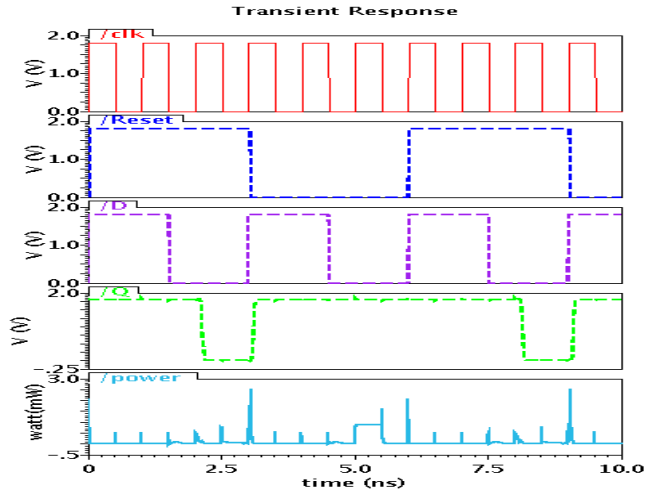

Fig. 2. Simulation results of TSPC DFF.

Fig. 2 shows simulation results of the existing positive edge triggered TSPC D Flip-Flop and in this regard we were used CADENCE Virtuoso UMC 180 nm technology tool with clock frequency 1GHz and simulation times of 10 ns. The power consumed by TSPC D flip-flop is 75.43 µW.

B. Operation of the proposed MTSPC DFF

Analysis of the behavior of node B reveals that for the times, when there is a path to ground, node B will always pre-charged to HIGH when clock (Clk) is LOW and will return back to LOW when Clk is HIGH. So, whenever the input D is at a stable LOW for a long time with respect to Clk, node B experiences continuous toggling. Such unnecessary behavior not only accounts for large power consumption but is also a source of noise on the output node, Q, caused by erroneous glitches caused every time Clk makes a LOW-to-HIGH transition. To solve this problem, the proposed MTSPC DFF architecture reveals that whenever the path to ground is ON, pre-charging node B should be suspended to prevent toggling. A simple technique that works here is to add a PMOS transistor that prevents the pre-charging phase to occur without affecting the global operation of the flip-flop. To prove this claim, consider the following Fig. 3.

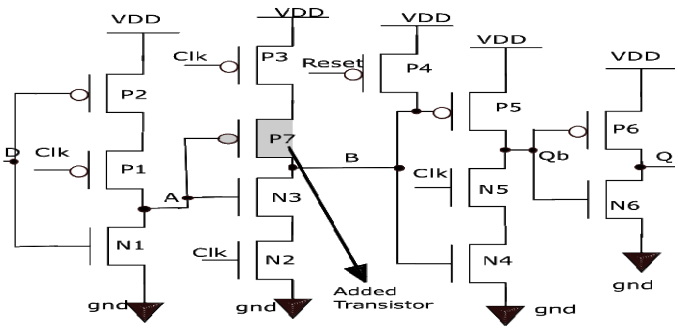

Fig.3. Positive edge triggered MTSPC DFF.

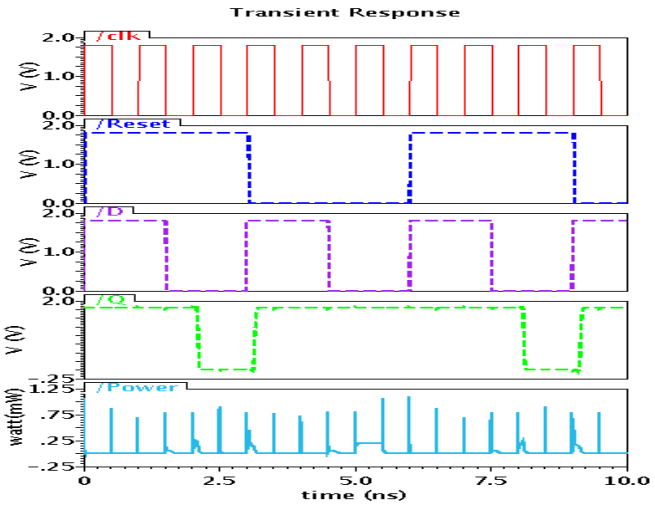

Fig.4. Simulation results of MTSPC DFF.

If Clk is LOW and D is LOW, node B, and consequently the node Qb, maintain their old values. If D changes to HIGH, node B pre-charge to HIGH; again, the output remains unaffected. Now, if Clk makes a LOW-to-HIGH transition, node B maintains its charge (HIGH), and the node Qb becomes LOW. After that, even if D becomes LOW again, the output will not be affected. If Clk makes a LOW-to-HIGH transition while D is LOW, node B will discharge, and the node Qb will be HIGH and Q will be low. Whenever the preset input (RESET) is low the preset PMOS will ON and the node Qb maintains HIGH. The simulation results of this

preset-able MTSPC D flip-flop is shown Fig. 4 and in this regard we were used CADENCE Virtuoso UMC 180 nm technology tool with clock frequency 1GHz and simulation times of 10nS.The power consumed by MTSPC D flip-flop is 21.83 µW.

C. Toggle mode Operation of the TSPC and MTSPC DFF

To test the toggle mode of operation, the output, Qb is connected to D input of the TSPC and MTSPC D flip-flop. The clock frequency applied for toggle mode operation is 2 GHz for TSPC and 4 GHz for MTSPC DFF. The simulation results of toggle mode TSPC DFF with clock frequency of 2 GHz and simulation time of 10 ns is shown in Fig. 5 and the simulation results of toggle mode MTSPC DFF with clock frequency of 4 GHz and simulation time of 10 ns is shown in Fig. 6.

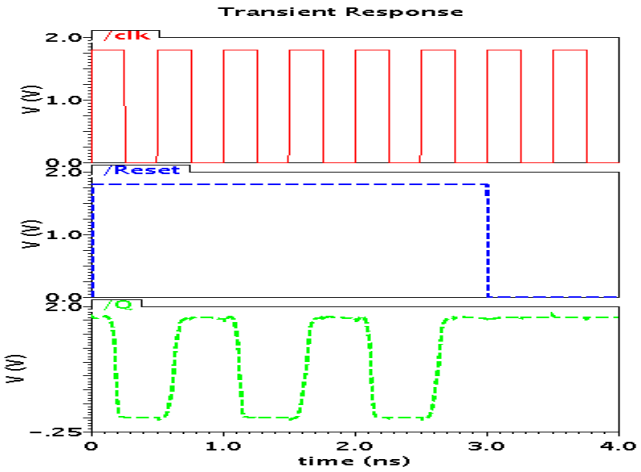

Fig. 5. Simulation results of toggle mode TSPC DFF.

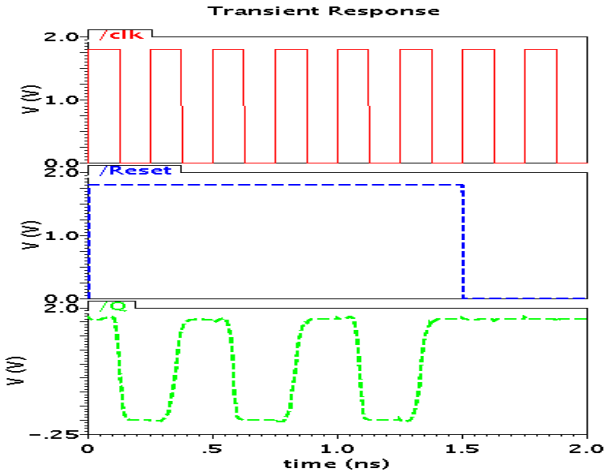

Fig. 6. Simulation results of toggle mode MTSPC DFF.

III. Simulation Results

In order to evaluate the performance of the proposed positive edge triggered MTSPC DFF and positive edge triggered TSPC DFF, a 7-bit gray code counter is designed using both the DFFs. The circuits are implemented in CADENCE virtuoso UMC 180 nm CMOS technology.

Gray code counter has wide application in Electronics world, like low power counter based analog-to-digital converter (ADC) [14]. Synchronous Gray counter toggle a single bit at each rising edge of clock pulse and it is required to add feedback path from MSB (most significant bit) to LSB (least significant bit) coupled to feed-forward path from LSB to MSB in order to continue counting properly. These requirements lead to complex design methodology and low frequency of operation. An Asynchronous Gray counter was proposed to counter these problems [15]. The gray code counter in Fig. 7 consists of two levels of Flip-Flops in toggle mode operation. The first level is asynchronous binary counter. Except MSB, outputs of first level counter goes to second level of toggle mode Flip-Flops. MSB bit of first level and outputs of second level build the Gray code. For high frequency gray-code counter implementation faster edge triggered Flip-Flops are needed. High frequency technique in CMOS is required in this context [16]. A preset-able Modified True-single-phase positive triggered flip-flop (MTSPC) is designed and proposed for high speed Gray code counter. The proposed technique improves speed, noise and power issue in high frequency gray code counter. The performance comparisons between TSPC and MTSPC DFF are shown in the table 1 and the performance comparison of TSPC DFF based and MTSPC DFF based gray code counter is given in table 2.

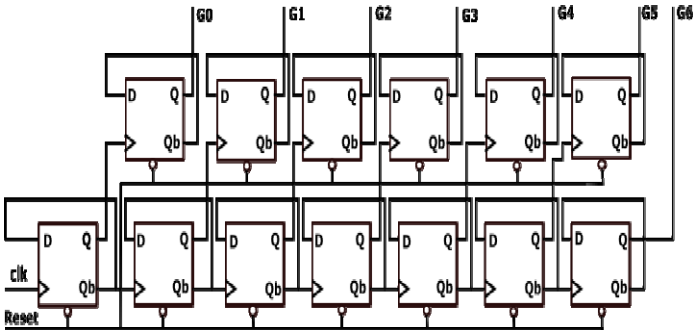

Fig. 7. 7-bit asynchronous gray code counter.

TABLE 1

Performance parameters	TSPC DFF	MTSPC DFF
Input clock frequency	1 GHz	1 GHz
Clock-to-Q delay (Low-to-High)	92.95 ps	61.08 ps
Clock-to-Q delay (High-to Low)	143.6 ps	122.9 ps
Average Clock-to-Q delay	118.27 ps	91.99 ps
Setup time(t_{setup})	70.13 ps	64.14 ps
Hold time(t_{hold})	≈ 0	≈ 0
Average power consumption	75.43 µW	21.83 µW

TABLE 2

Performance parameter	TSPC DFF based gray counter	MTSPC DFF based gray counter
Maximum frequency of operation	500 MHz	1 GHz
Maximum propagation delay of MSB	1.6 ns	0.96 ns
Power consumption	1.52 mW (1.52×E-3)	244.2 µW (244.2×E-6)
Power Delay Product(PDP)	2.4 pJ (2.4×E-12)	0.23 pJ (0.23×E-12)

IV. CONCLUSION

In this work, a new preset-able modified true single phase clocked (MTSPC) D flip-flop is proposed for the preset-able gray code counter design. The technique utilizes a clocked dynamic logic. The proposed preset-able 7-bit gray code counter can be used up to 1 GHz clock frequency, unlike a TSPC D flip-flop based preset-able 7-bit gray code counter which can be used up to 500 MHz clock frequency. The preset-able TSPC D flip-flop has more noise at the output, this noise not only affect the output but also consumed very large power. The Proposed preset-able MTSPC D flip-flop has very less noise at the output and consequently the power consumption is also very low. The proposed preset-able MTSPC D flip-flop can be use fast, low power electronics world. Using the above technique a preset-able Asynchronous 7-bit gray code counter is designed using UMC 180 nm CMOS technology. In this design maximum 1 GHz frequency of operation is achieved. Power consumption is reduced from 1.52 mW (which is the power consumption of preset-able TSPC based 7-bit gray code counter) to 244.2 µW by suspending the unnecessary toggling in the intermediate nodes of D flip-flop by adding one extra PMOS (as discussed in MTSPC D FF).

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