A Fast-Locking, Low-Jitter Pulsewidth Control Loop for High-Speed ADC

Zhangming Zhu, Maliang Liu, Jingyu Wang, and Yintang Yang

***Abstract*— A fast-locking, high-precision, and low-jitter pulsewidth control loop (PWCL) for high-speed high-resolution analog-to-digital converter is presented. Only through controlling the delay of rising edge to adjust duty cycle, the clock jitter could be suppressed greatly. An improved charge pump with a follower circuit and self-biased loop was designed to decrease the voltage ripples for higher accuracy and lower jitter. A startup circuit was adopted to enable the pulsewidth control loop lock rapidly. With the SMIC 0.18 μm 3.3 V CMOS process, the simulation and measured results show that within 180 ns the PWCL can lock the clock duty cycles for the accuracy of $50 \pm 1\%$ with 10%∼90% input duty cycle from 50 to 550 MHz. The rms-jitter is 73 fs at 250 MHz. The active area is about 0.023 mm^2.**

***Index Terms*— Charge pump, clock jitter, CMOS, pipelined analog-to-digital converter (ADC), pulsewidth control loop (PWCL).**

I. Introduction

To meet the demand of high-speed CMOS VLSI circuits, many high-speed analog-to-digital converters (ADCs) adopt double data rate technology [1]–[12] to get large data throughput. Compared with other ADCs, pipelined ADCs have an abroad application in many electronic systems with merits of high speed, good precision, and low power dissipation. In the design of pipelined ADCs, the jitter and accuracy of the system clock become more a concern as both ADC resolution and analog input frequency increase [10]. So the system clock optimization for low-jitter and high accuracy can be both challenging and rewarding. The pulsewidth control loop (PWCL) mechanism is developed to solve this problem perfectly.

The conventional PWCL [3] that adjusts the duty cycle by controlling the delay of rising and falling edges has a high jitter and long locking time. The fast-locking PWCL [4] modified from the conventional PWCL can achieve a fast locked and presentable output duty cycle. But it requires an exact 50% duty cycle of the clock signal and a voltage-difference-to-digital converter, which costs larger chip size and more power consumption. Another PWCL [10] using second-order passive loop filter has a lower power consumption, but chip area and loop stability are unavoidable problems.

In this brief, a new PWCL circuit is proposed, which introduce a startup circuit to obtain a fast locking. Moreover, an improved charge pump is used to reduce the ripple voltage for higher accuracy and lower jitter. The clock jitter could be greatly suppressed and the complication of circuit could also be reduced only through controlling the delay of rising edge to adjust duty cycle. The architecture of the proposed PWCL is discussed in Section II. The system analysis and design are discussed in Section III. The experimental results are illustrated in Section IV.

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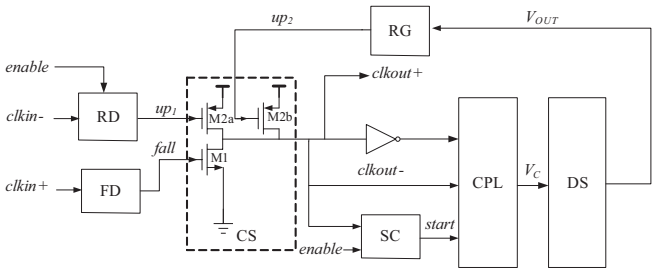


Fig. 1. Proposed PWCL architecture.

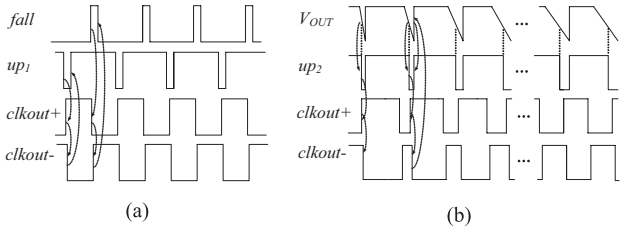


Fig. 2. (a) Duty-cycle tracking mode. (b) Duty-cycle correction mode different mode of proposed PWCL.

II. Architecture of Prospoed PWCL

The proposed PWCL architecture is shown in Fig. 1. It includes the control Stage (CS), charge pump loop (CPL), delay stage (DS), startup circuit (SC), rising edge generator (RG), rising edge differentiator (RD), and falling edge differentiator (FD). In different applications, the PWCL is used in either the duty-cycle tracking mode or the duty-cycle correction mode. The timing diagrams for duty-cycle tracking mode and duty-cycle correction mode are shown in Fig. 2(a) and (b). The choice for mode is controlled by the signal enable. In the duty-cycle tracking mode, the charge pump loop, delay stage, startup circuit, and rising edge generator do not work so as to reduce the power dissipation, and the output duty cycle is maintained to be the same as the input duty cycle. In the duty-cycle correction mode with the rising edge differentiator off, the falling edge differentiator generates a pulse at every rising edge of the input signal, while the pulse has specific width, equal to the transmission delay of several inverters [11]. The pulse triggers the control stage to generate the falling edge of output clock. With a fixed-delay falling edge, the PWCL initialized by startup circuit has the biggest duty cycle in the first correction period, and then adjusts the duty cycle by controlling the delay of a low pulse, which triggers the control stage to generate the rising edge. The low pulse up_2 generated from the rising edge generator is affected by the delay stage, which controlled by the voltage V_C generated from charge pump loop.

Compared with the conventional PWCL circuits which adjust duty cycle through double-edge modulating, the proposed PWCL could suppress the jitter of input clock to a half. To obtain a fast locking-time, a startup circuit is used to initialize the voltage of charge pump loop. The key circuits in the PWCL are discussed in detail below.

A. Charge Pump Loop

Fig. 3 shows the circuit structure of the charge pump loop, which mainly consists of an improved charge pump and low-pass filter and single-stage amplifier. The charge pump converts duty cycle into current, which charges or discharges capacitor CP of the low-pass filter. The low-pass filter changes the current signal to voltage signal V_{C1}, finishing a current-to-voltage conversion. Another function of low-pass filter is to reduce the ripples which resulting in clock jitter [6].

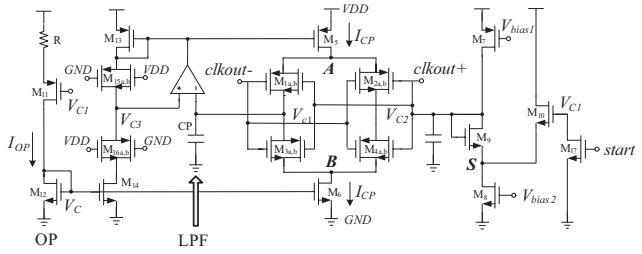


Fig. 3. Charge pump loop.

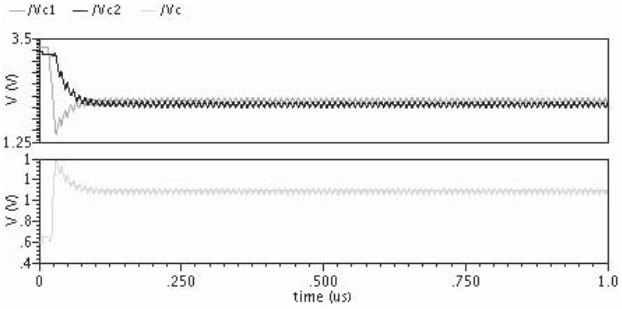


Fig. 4. Simulations of the voltages V_{C1}, V_{C2}, and V_C at a frequency of 100 MHz.

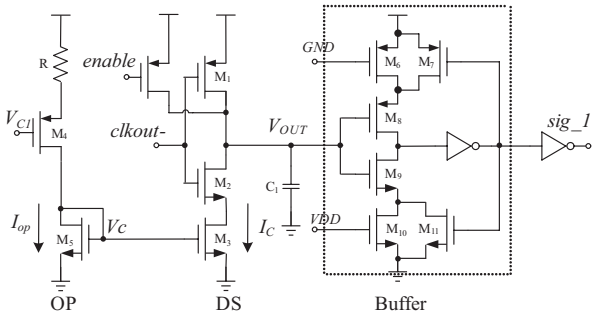


Fig. 5. Schematic of single-stage amplifier, delay stage, and the buffer of rising edge generator.

The voltage V_{C1} is applied on single-stage operational amplifier to produce a control voltage V_C to the delay stage, thereby generating delay time to change the duty cycle to the target ratio. The initial value of V_{C1} is decided by the startup circuit, and then the startup circuit won't function. During the initializing process of V_{C1}, the startup circuit generated a start signal to discharge the voltage of V_{C1}.

The ripple of control voltage V_C determines the jitter and the duty cycle error of the output clock. The performance of charge pump influences the ripple of V_C directly. Among all the nonideal factors affecting the performance of current pump, current mismatch, and charge sharing have a heavy effect.

To obtain a perfect current matching characteristic, we propose a new improved charge pump, which adopts combined charge pump and self-biasing technique to guarantee the sourcing/sinking current matching. Since the follower exists between the point V_{C1} and V_{C2}, the voltages of two points always keep the same. Meanwhile because of the feedback brought by amplifier existing in self-biasing loop, the point voltage V_{C3} is equal to V_{C1}. So $V_{C3} = V_{C1} = V_{C2}$. The combined charge pump structure uses the complementary signals clkout$^+$ and clkout$^-$ as inputs. Either the left side or the right side of the switches is turned on to charge or discharge V_{C1} and V_{C2}. The current I_{CP} always has one turn-on path, thus stabilizing the voltage of nodes A and B. So the voltages in nodes A and B can be kept nearly constant. Meanwhile through using the same size transmission gates M1, M2, M15, and M3, M4, M16, the drains of biasing MOSFET, current sink and current source in the charge pump keep the same voltage, avoiding being affected by short channel modulation, which caused the current mismatch.

In addition, using the self-biasing technique, the biasing voltage for current source/sink in charge pump is generated from current mirror loop composed by M5, M6, M13, and M14. Thus $I_{\mathrm{CP}} = kI_{\mathrm{OP}}$, where k equals the size ratio of M5 and M13, M6, and M14. Self-biasing avoids the necessity for external biasing, which can require special bandgap bias circuits, by generating all of the internal bias voltages from each other so that the bias levels are completely determined by the operating conditions.

In the ordinary charge pump, charge sharing effect could cause a jump phenomenon which brings the control voltage bigger ripples, resulting in worse jitter performance and duty-cycle accuracy. This brief gives a new structure with a follower circuit between two sides of charge pump. The voltage V_{C1} is applied as input of the M10, while M7 used as current source load. Diode-connected device M9 could give a voltage level shift to the node S. Since M9 and M10 have the same size, we have $V_{\mathrm{GS10}} = V_{C1} - V_S = V_{\mathrm{TH}} + V_{\mathrm{DSAT}}$, $V_{\mathrm{GS9}} = V_{C2} - V_S = V_{\mathrm{TH}} + V_{\mathrm{DSAT}}$, thus $V_{C1} = V_{C2}$. As a result, if all four switches turn off, the drain voltages of M1, M2, M3, and M4 will be held to equal. Therefore, it won't produce the jump phenomenon in the nodes A and B. So the charge sharing problem can be eliminated.

A SMIC 0.18 μm 3.3 V CMOS Spice model is used for simulation. Fig. 3 shows the wave forms of the voltages V_{C1} and V_{C2} and V_C at a frequency of 100 MHz. Since the usage of improved charge pump, the current mismatch and charge sharing effects are suppressed greatly. The error voltage between V_{C1} and V_{C2} is reduced leading to a smaller voltage ripple at V_C, lower jitter and high duty-cycle accuracy at output clock.

B. Single-Stage Amplifier and Delay Stage

The schematics of single-stage amplifier in charge pump loop, delay stage and buffer in rising edge generator are shown in Fig. 5. Single-stage amplifier, adopting common source with source degeneration, amplifies the input voltage V_{C1} into the control voltage V_C for driving delay stage to generate different delay time. By controlling the discharging speed of C_1 in delay stage, the PWCL can adjust the duty cycle of output clock to a precise 50% duty cycle.

The delay stage consists of the inverter with V_C as control voltage, the capacitor C_1. The buffer with positive feedback generates the pulse with steeper edges, which triggers the rising edge generator to give a low-level pulse that brings the rising edge of output clock. In this circuit, we have $I_{\mathrm{OP}} = k_1 I_C$, where I_C and I_{OP} represent discharging current of delay stage and current of single-stage amplifier, respectively. k_1 is ratio of size parameter of M5 and M3. When M3 and M5 have the same size, we have $I_C = I_{OP} = V_{C1}GM$. Where GM is transconductance of single-stage amplifier, and GM<0, so I_C is inverse to V_{C1}. Assumed that the node voltage V_{OUT} has a drop voltage ΔV_{OUT}, the PWCL generates the pulse which triggers the rising edge of clkout$^+$. So the delay time generated by delay stage in the n_{th} period can be expressed as

$$\begin{aligned} t &= \frac{2C1\Delta V_{\mathrm{OUT}}}{I_{\mathrm{ctrl}}} \\ &= \frac{2C1\Delta V_{\mathrm{OUT}}}{V_{C1}\mathrm{GM}} \\ &= \frac{2C1\Delta V_{\mathrm{OUT}}}{\mathrm{GM}(V_{\mathrm{initial}} + \Delta V_{C1}(n-1) + \Delta \mathrm{T}(n) k I_{\mathrm{OP}})} \end{aligned} \tag{1}$$

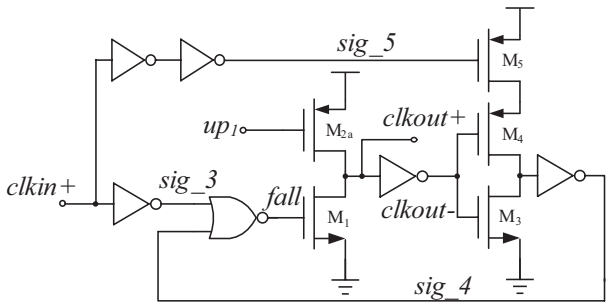


Fig. 6. Schematic of the falling edge differentiator.

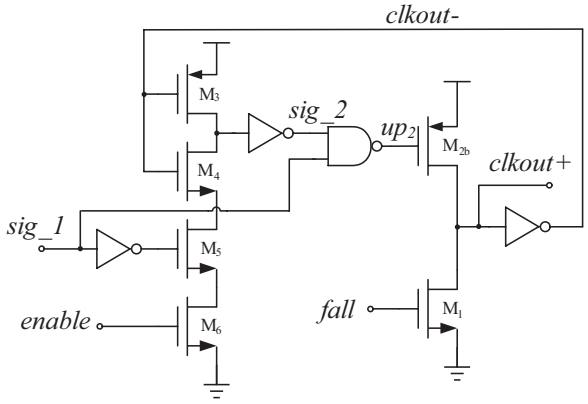


Fig. 7. Schematic of the rising edge generator.

where k is the ratio between I_{CP} and I_{OP}. $\Delta T(n) = T_1(n) - T_2(n)$, $T = T_1(n) + T_2(n)$, $T_1(n)$ and $T_2(n)$ represent the time of clkout$^+$ is logic 1 and 0, respectively. V_{initial} is the initial voltage of the charge pump after startup circuit gives a start signal pulse. $\Delta V_{C1}(n-1)$ is the variety of V_{C1} after $n-1$ periods. When the PWCL is locked, the duty cycle is 50%. And $T_1(n) = T_2(n) = T/2$, $\Delta T(n) = 0$, therefore V_{C1} maintains constant. Accordingly, the delay time is equal to $T/2$ and the PWCL keeps stable.

C. Rising Edge Generator, Falling Edge Differentiator, and Control Stage

The schematics of rising edge generator and falling edge differentiator are shown in Figs. 6 and 7. At every rising edge of clkin$^+$, the falling edge differentiator generates a high voltage pulse, which pulls down the clkout$^+$ through using the clkin$^+$ and the feedback signal as inputs of NOR gate. When the rising edge of clkin$^+$ arrives, sig_3 is pulled down from high voltage to low voltage. Meanwhile the sig_4 is still low voltage. So the output of NOR generates a narrow high-voltage pulse, and changes the logic state of clkout$^+$ through control stage. With the same theory, the rising edge generator generates the low-voltage pulse that triggers the control stage to pull up clkout$^+$, through detecting the output signal V_{OUT} of the delay stage.

The control stage of PWCL consists of M1, M_{2a}, and M_{2b}. In different work modes, M2 works with either M_{2a} or M_{2b}. In the duty-cycle tracking mode, M_{2b} shuts down because signal up2 stays high voltage. In duty-cycle correction mode, M_{2a} shuts down because signal up1 stays high voltage.

III. Loop Analysis of the Proposed PWCL

The linear model of the proposed PWCL is shown in Fig. 8, and D_{in} is the input duty cycle, D_{out} is the output duty cycle, K_{CP} is the charge pump gain, A_0 and w_P is the gain and dominant pole of the single-stage amplifier respectively, K_{CS} is the control stage gain, K_{DS} is the delay stage gain, K_{IC} is the gain of inverter, CP is the low-pass filter capacitor. Since w_P locates at very high frequency, the influence of w_P can be ignored. The locking time analysis approximates first-order system.

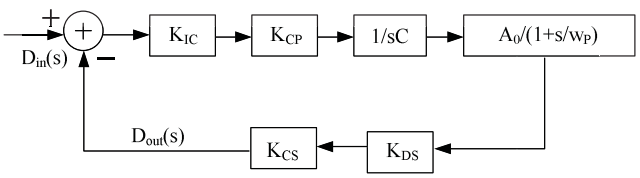


Fig. 8. Linear model of the proposed PWCL.

The closed-loop transfer function can be represented as follows:

$$H(s) = \frac{D_{\mathrm{out}}(s)}{D_{\mathrm{in}}(s)} = \frac{1}{s\dfrac{C}{K_{\mathrm{IC}} \times K_{\mathrm{CP}} \times A_0 \times K_{\mathrm{DS}} \times K_{\mathrm{CS}}} + 1}. \quad (2)$$

The step response for the first-order system can be expressed as follows:

$$\Delta D_{\mathrm{out}}(t) = \Delta D_{\mathrm{out}} \left[1 - e^{\dfrac{-K_{\mathrm{IC}} K_{\mathrm{CP}} A_0 K_{\mathrm{DS}} K_{\mathrm{CS}} t}{C}} \right] \quad (3)$$

where ΔD_{out} denotes the variety of output duty cycle in the step response. When the duty-cycle error is below 1% in 250 MHz, in the proposed PWCL, $I_{\mathrm{CP}} = 208\ \mu$A, $K_{\mathrm{CP}} = 2I_{\mathrm{CP}}$, $K = K_{IC} A_0 K_{\mathrm{DS}} K_{\mathrm{CS}} = 0.96\ \mathrm{V}^{-1}$. Considering of the demand of locking time and accuracy, the capacitor of the low-pass filter C = 8 pF. After being initialized by the startup circuit, the output duty cycle changed from 25% to $50 \pm 1\%$, the settling time T_S can be solved from (2).

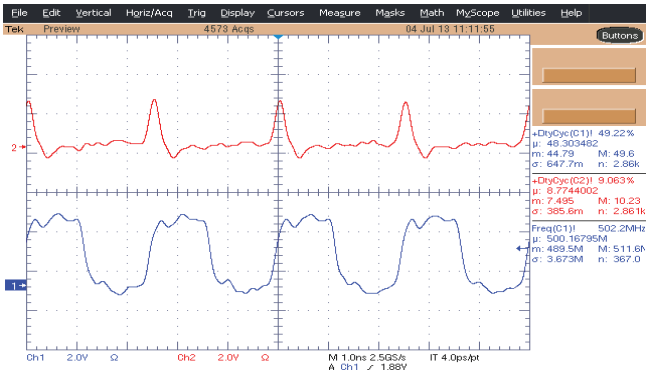
The locking time $T_{\mathrm{LOCK}} = T_{\mathrm{START}} + T_S$, where T_{START} is the pulse width of start from startup circuit. Because of the delay of startup circuit elements and input clock, in the real situation, for the different input duty cycle in different frequency, the locking time of PWCL is approximately below 180 ns when the duty cycle arrives at the accuracy of $50 \pm 1\%$.

IV. Experiment Results

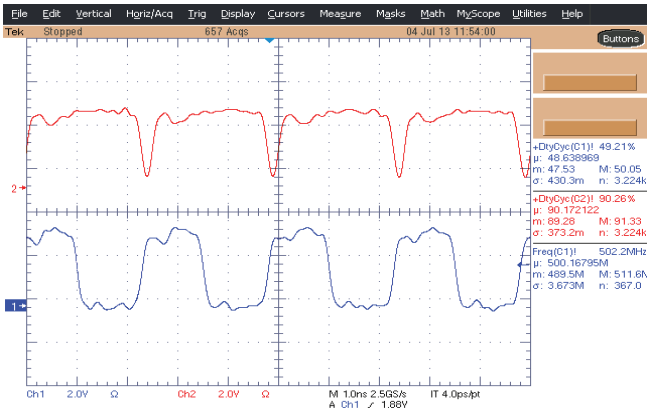
The proposed PWCL is implemented using the SMIC 0.18 μm 3.3 V CMOS process. The proposed PWCL can modulate the input clock with 10%∼90% input duty cycle from 50 to 550 MHz, and get the output clock for the accuracy of $50 \pm 1\%$. Fig. 9 shows the PWCL adjusts the output duty cycle to $50 \pm 1\%$ when the input clock has different duty cycle at 500 MHz.

Fig. 10 shows the peak-to-peak and rms-jitter for the 250 MHz output clock at 640 and 73 fs through eyeDiagram analysis. With the simulation and experiment results, the proposed PWCL can operate correctly at different frequencies and duty cycles of the input clock and produce the clock with accuracy of $50 \pm 1\%$, and achieve fast locking and low jitter. It can satisfy the applications of the ADC with high-speed and high-precision perfectly. This circuit has finished the layout design, and through the dummy MOSFET, the mismatch has been decreased heavily. The proposed PWCL die micro-photo is shown in Fig. 11, the active area is about 0.023 mm^2.

On the comparison with other PWCLs, which have been realized, the proposed PWCL has the obvious advantages at the range of input



(a)



(b)

Fig. 9. (a) Frequency = 500 MHz, Clkin = 90%. (b) Frequency = 500 MHz, Clkin = 10% Frequency = 500 MHz, the output clock is 50% for the input clock in different duty cycle.

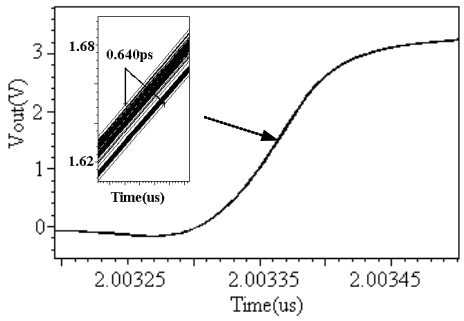


Fig. 10. EyeDiagram analysis in 250 MHz.

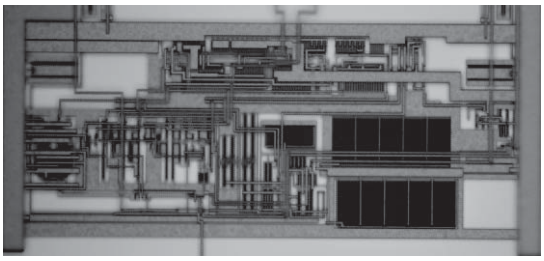


Fig. 11. Microphoto of the proposed PWCL.

clock duty cycle, locking-time and jitter characteristic and chip area. Table I presents the performance comparison of the proposed PWCL and the others.

TABLE I
PERFORMANCE COMPARISON OF PWCLS

	This Work	[7]	[8]	[9]	[10]
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply Voltage(V)	3.3	1.8	1.8	1.8	1.8
Locking Time(ns)	180	N/A	600	<36 cycles	<405
Input Duty(%)	10~90	40~60	30~70	30~70	10~80
Output Duty(%)	50±1	50±1	30~70	50±1	30~60
Clock Jitter	rms jitter 73fs@ 250M Hz	p-p jitter 3.2ps @1 GHz	rms jitter 1.9ps @1.3 GHz	p-p jitter 28.9ps @250 MHz	N/A
Active Area	0.023 mm^2	N/A	0.057 mm^2	0.09 mm^2	N/A

V. CONCLUSION

For the high-speed and high-resolution ADC, a fast-locking, high-precision, and low-jitter system clock has an important influence to the characteristics of the ADC. Mended from the conventional PWCL, the system presented in this brief uses the single edge to adjust the duty cycle accurately. An improved charge pump is used to reduce the jitter and error of duty cycle greatly. The locking-time is shorted by utilizing the startup circuit to initialize the charge pump voltage. The proposed PWCL can modulate the input clock with 10%~90% input duty cycle from 50 to 550 MHz, and get the output clock for the accuracy of 50 ± 1%. The proposed PWCL can be used in various applications, especially in the high-speed and high-resolution ADC.

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