Input Offset Estimation of CMOS Integrated Circuits in Weak Inversion

Meysam Akbari, Omid Hashemipour, and Farshad Moradi

***Abstract*— This brief studies the current mismatch of MOS transistors operating in weak inversion region. Explicit formulas are derived from the drain-current relationship of a long-channel MOS transistor. By referring the drain-current variance to the gate terminal under the small-signal conditions, the dependence of the gate–source voltage on the design parameters and sources of mismatch can be considered. This will help designers to choose the optimum sizes and the efficient gm/I_D ratio for current offset reduction of transistors that their mismatch affects the circuit performance, significantly. In order to confirm the accuracy of the calculated drain-current variance, the hand analysis results are compared with MATLAB simulator outputs. In addition, the input offset of a conventional folded-cascode amplifier is estimated by hand analysis, and the results are compared with SPICE simulator outputs through Monte Carlo analysis.**

***Index Terms*— Current variance, mismatch, MOS transistor, weak inversion.**

I. Introduction

The rapid growth of portable and wearable applications is the main reason for gaining a wide interest in the ultralow-power and ultralow-voltage analog and digital circuits. In such applications, transistors are forced to operate in the weak inversion region to keep the energy consumption as low as possible [1]. The weak inversion region provides better energy efficiency compared to the other operating regions (strong and moderate inversions) due to its high gm/I_D ratio without requiring a high supply voltage [2]. Nonetheless, many problems and design challenges are raised once the transistors operate under low supply voltages and nanolevel currents. Some of the circuit topology-related issues can be solved by proposing new circuit techniques such as self-biasing structures [2], [3]. However, some of these constraints are related to the region of operation, i.e., weak inversion, due to the exponential dependence of current on different parameters that may lead to a nonignorable input offset [4].

Basically, input offset is caused by undesirable fabrication process errors. The performance of the integrated circuits, especially analog circuits, is heavily influenced by the accuracy of the elements matching during the implementation process [5]. The source of mismatch is divided to two kinds: 1) systematic error that can be reduced by some matching techniques and 2) the random error that is not the same for all elements. Therefore, the latter cannot be easily improved. The dominant sources of the random errors are threshold-voltage variations ΔV_T and current factor variations $\Delta\beta$, as the basic components of the drain-current relationship [5]. Based on these components, there are some mismatch models of simple MOS drain-current relationship that have been calculated by hand analysis in the strong inversion [6], [7]. These models have been reanalyzed for a more complex drain-current relationship to increase the accuracy of the models and have a continuity from strong inversion to the weak inversion [8], [9]. Besides, they are not much applicable in the weak inversion, because there is still a discontinuity in slopes of models from strong inversion to the weak inversion [9].

In addition, some other mismatch characteristics have been also extracted based on physical basis and measurement results to increase the accuracy of models in all bias conditions [10], [11]. Despite increasing the use of ultralow-power circuits in recent years, a precise mismatch model in the weak inversion region has not been provided. Moreover, the complexity of the drain-current relationship does not let designers to provide a straightforward design methodology in this region. Therefore, an accurate hand analysis for the drain-current relationship in the weak inversion region is still noteworthy for designers from circuit point of view in order to estimate the input offset.

In this brief, the drain-current variance of a MOS transistor is calculated based on hand analysis of a long-channel drain-current relationship in the weak inversion region. The calculated variance includes two adjustable components, current factor β, and gm/I_D ratio of the corresponding transistors. The total offset of each circuit can be estimated by referring the drain-current variance of each transistor to the input node in order to choose the best values of β and gm/I_D, and reduce the input offset.

This brief is organized as follows. Section II describes a summary of MOS transistor mismatch and considers the drain-current relationship of a long-channel MOS transistor in the weak inversion region and provides an accurate hand analysis of its variance. In addition, the calculated relationships are compared to those in the strong inversion and their accuracy is evaluated by MATLAB simulator. In Section III, the input offset of a conventional folded cascode amplifier is estimated based on the calculated drain-current variance in the weak inversion region and the results are compared to SPICE simulator outputs. Finally, Section V concludes this brief.

II. Drain-Current Variance in Weak Inversion

A MOS device biased in the weak inversion is sensitive to some parameters such as noise, variability, and mismatch [1], [4]. The noise and mismatch can be improved by designers if they be able to choose the optimum sizes for MOS devices. To consider a hand analysis-based mismatch model, the following equation represents the drain-current relationship (I–V characteristic) of a long-channel MOS transistor in the weak inversion [1]:

$$I_D = \left(2nU_T^2\beta\right)\exp\left(\frac{V_{GS}-V_T}{nU_T}\right)\left[1-\exp\left(\frac{-V_{DS}}{U_T}\right)\right] \quad (1)$$

where β represents $\mu C_{ox}W/L$, U_T is the thermal voltage with a value of 26 mV at room temperature, and n is the slope factor of the weak inversion, which is dependent on technology parameters. The other symbols have their usual meanings. The critical transistors in terms of mismatch are usually biased in saturation region of the weak inversion by setting $V_{DS} > 3U_T$, so, (1) can be simplified to

$$I_D = \left(2nU_T^2\beta\right)\exp\left(\frac{V_{GS}-V_T}{nU_T}\right). \quad (2)$$

Manuscript received January 11, 2018; revised March 15, 2018; accepted April 23, 2018. *(Corresponding author: Omid Hashemipour.)*

M. Akbari and O. Hashemipour are with the Faculty of Electrical Engineering, Shahid Beheshti University, Tehran 1983969411, Iran (e-mail: me_akbari@sbu.ac.ir; hashemipour@sbu.ac.ir).

F. Moradi is with the Department of Engineering, Aarhus University, 8200 Aarhus, Denmark (e-mail: moradi@eng.au.dk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2018.2830749

It shows that the drain current of a MOS transistor has a linear dependence on the current factor β and an exponentially dependence on the threshold voltage V_{T}. Therefore, a small variation of these parameters results in a severe change in the value of drain-current and consequently a large input offset. As mentioned before, the existence of low supply voltages in ultralow-power applications, some circuitry approaches like self-biasing configurations [3] can be employed to ease the control of such offset voltages. Besides, in some of the more sensitive cases in which the use of circuit-level techniques may not be possible, designers have to use design methodologies to increase the accuracy of their circuits to achieve minimum input offset. In this way, calculating the drain-current variance is applicable to refer the offset of circuit transistors to the input node.

Basically, the value of P (a sample parameter) includes a fixed part and a random part. To find the contribution of each part, based on the Pelgrom mismatch model [7], the variance of ΔP for two rectangular devices with equal area can be given by

$$\sigma^2(\Delta P) = \frac{A_{\mathrm{p}}^2}{WL} + S_{\mathrm{p}}^2 D_x^2 \tag{3}$$

where A_{p} is the area proportionality constant for P, and S_{p} describes the variation of P with spacing while the distance between two devices along x-axis is modeled by D_x. The role of some matching techniques is to interdigitate critical devices such as input differential pairs and current mirrors, which leads value of D_x to zero. Thus, to predict the mismatch variance of a circuit, the proportionality constant can be measured [6], [15]. Therefore, by considering β and V_{T} as two random variables with means $\overline{\beta}$ and $\overline{V}_{\mathrm{T}}$, respectively, (2) can be rewritten by

$$I_{\mathrm{D}} = \left(2nU_{\mathrm{T}}^2\beta\right)\exp\left(\frac{V_{\mathrm{GS}} - \overline{V}_{\mathrm{T}}}{nU_{\mathrm{T}}}\right) \times \exp\left(-\frac{V_{\mathrm{T}} - \overline{V}_{\mathrm{T}}}{nU_{\mathrm{T}}}\right). \tag{4}$$

Using the Taylor expansion, (4) can be simplified as

$$I_{\mathrm{D}} = \left(2nU_{\mathrm{T}}^2\beta\right)\exp\left(\frac{V_{\mathrm{GS}} - \overline{V}_{\mathrm{T}}}{nU_{\mathrm{T}}}\right) \times \left(1 - \frac{V_{\mathrm{T}} - \overline{V}_{\mathrm{T}}}{nU_{\mathrm{T}}} + \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2}{2!(nU_{\mathrm{T}})^2} - \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^3}{3!(nU_{\mathrm{T}})^3} + \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^4}{4!(nU_{\mathrm{T}})^4} - \ldots\right). \tag{5}$$

To calculate the drain-current variance, the expression $\sigma^2(I_{\mathrm{D}}) = E\{I_{\mathrm{D}}^2\} - E^2\{I_{\mathrm{D}}\}$ is used [13], where E is the expectation of I_{D}. Thus, first of all, $E\{I_{\mathrm{D}}^2\}$ and $E^2\{I_{\mathrm{D}}\}$ must be calculated. For simplicity, by assuming $\tilde{I}_s = (2nU_{\mathrm{T}}^2)\exp[(V_{\mathrm{GS}} - \overline{V}_{\mathrm{T}})/nU_{\mathrm{T}}]$, the expectation of I_{D} is given by

$$E\{I_{\mathrm{D}}\} = E\left\{\tilde{I}_s\beta \times \left(1 - \frac{V_{\mathrm{T}} - \overline{V}_{\mathrm{T}}}{nU_{\mathrm{T}}} + \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2}{2!(nU_{\mathrm{T}})^2} - \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^3}{3!(nU_{\mathrm{T}})^3} + \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^4}{4!(nU_{\mathrm{T}})^4} - \ldots\right)\right\}. \tag{6}$$

Based on the measurement results [7], the correlation between β and V_{T} is weak and can be ignored. So, (6) is modified to

$$E\{I_{\mathrm{D}}\} = \tilde{I}_s\overline{\beta} \times \left(1 - E\left\{\frac{V_{\mathrm{T}} - \overline{V}_{\mathrm{T}}}{nU_{\mathrm{T}}}\right\} + E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2}{2!(nU_{\mathrm{T}})^2}\right\} - E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^3}{3!(nU_{\mathrm{T}})^3}\right\} + E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^4}{4!(nU_{\mathrm{T}})^4}\right\} - \ldots\right). \tag{7}$$

Note that $\overline{V}_{\mathrm{T}}$ is the mean of V_{T} and $E\{V_{\mathrm{T}}\} = \overline{V}_{\mathrm{T}}$, it is concluded that $E\{V_{\mathrm{T}} - \overline{V}_{\mathrm{T}}\} = 0$. In order to decrease the complexity of mathematic analyses, higher order terms are dropped because of their low impact on the expectation of I_{D}. Therefore, (7) can be simplified to

$$E\{I_{\mathrm{D}}\} \approx E\{\beta\}\tilde{I}_s \times \left(1 + E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2}{2!(nU_{\mathrm{T}})^2}\right\}\right). \tag{8}$$

Based on the presented expression of expectation in [13], $\sigma^2(V_{\mathrm{T}}) = E\{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2\}$, (8) is rewritten as

$$E\{I_{\mathrm{D}}\} \approx E\{\beta\}\tilde{I}_s \times \left(1 + \frac{1}{2(nU_{\mathrm{T}})^2}\sigma^2(V_{\mathrm{T}})\right) \tag{9}$$

where $\sigma^2(V_{\mathrm{T}})$ is the variance of random variable V_{T}. In a similar way, $E\{I_{\mathrm{D}}^2\}$ can be given by

$$E\{I_{\mathrm{D}}^2\} = \tilde{I}_s^2 E\{\beta^2\} \times E\left\{\left(1 - \frac{V_{\mathrm{T}} - \overline{V}_{\mathrm{T}}}{nU_{\mathrm{T}}} + \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2}{2!(nU_{\mathrm{T}})^2} - \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^3}{3!(nU_{\mathrm{T}})^3} + \frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^4}{4!(nU_{\mathrm{T}})^4} - \ldots\right)^2\right\}. \tag{10}$$

Using expression $(a+b+c)^2 = a^2 + b^2 + c^2 + 2ab + 2ac + 2bc$, (10) is rewritten as

$$E\{I_{\mathrm{D}}^2\} = \tilde{I}_s^2 E\{\beta^2\} \times \left(E\{1\} - 2E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})}{nU_{\mathrm{T}}}\right\} + 2E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2}{(nU_{\mathrm{T}})^2}\right\} - \frac{4}{3}E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^3}{(nU_{\mathrm{T}})^3}\right\} + \frac{2}{3}E\left\{\frac{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^4}{2!2!(nU_{\mathrm{T}})^4}\right\} - \ldots\right). \tag{11}$$

By dropping higher order terms and considering $\sigma^2(V_{\mathrm{T}}) = E\{(V_{\mathrm{T}} - \overline{V}_{\mathrm{T}})^2\}$ and $E\{V_{\mathrm{T}} - \overline{V}_{\mathrm{T}}\} = 0$, (11) can be approximated as

$$E\{I_{\mathrm{D}}^2\} \approx E\{\beta^2\}\tilde{I}_s^2 \times \left(1 + \frac{2}{(nU_{\mathrm{T}})^2}\sigma^2(V_{\mathrm{T}})\right). \tag{12}$$

From (9) and (12), the variance of (2) is achieved as

$$\sigma^2(I_{\mathrm{D}}) = E\{\beta^2\}\tilde{I}_s^2 \times \left(1 + \frac{2}{(nU_{\mathrm{T}})^2}\sigma^2(V_{\mathrm{T}})\right) - E^2\{\beta\}\tilde{I}_s^2\left(1 + \frac{1}{(nU_{\mathrm{T}})^2}\sigma^2(V_{\mathrm{T}}) + \frac{1}{4(nU_{\mathrm{T}})^2}\sigma^2(V_{\mathrm{T}})\right). \tag{13}$$

It is clear that the last term of (13) has a low impact compared to the other terms and can be dropped. The result is

$$\sigma^2(I_{\mathrm{D}}) = +\tilde{I}_s^2 E^2\{\beta\} \times \left(\frac{1}{(nU_{\mathrm{T}})^2}\sigma^2(V_{\mathrm{T}})\right) + \tilde{I}_s^2(E\{\beta^2\} - E^2\{\beta\}) \times \left(1 + \frac{2}{(nU_{\mathrm{T}})^2}\sigma^2(V_{\mathrm{T}})\right). \tag{14}$$

By replacing $\tilde{I}_s = \overline{I}_{\mathrm{D}}/\overline{\beta}$ in (14) and considering $\sigma^2(\beta) = E\{\beta^2\} - E^2\{\beta\}$, $E^2\{\beta\} = \overline{\beta}^2$, $\overline{I}_{\mathrm{D}} \approx I_{\mathrm{D}}$ & $\overline{\beta} \approx \beta$, by assuming that $\sigma^2(V_{\mathrm{T}})$ and $\sigma^2(\beta)$ are uncorrelated [7], the drain-current variance in the weak inversion is given by

$$\sigma^2(I_{\mathrm{D}}) = \left(\frac{I_{\mathrm{D}}}{\beta}\right)^2\sigma^2(\beta)\left(1 + 2\frac{\sigma^2(V_{\mathrm{T}})}{(nU_t)^2}\right) + \left(\frac{I_{\mathrm{D}}}{nU_t}\right)^2\sigma^2(V_{\mathrm{T}}). \tag{15}$$

Equation (15) is very useful from the circuit analysis point of view. By considering $nU_t = I_{\mathrm{D}}/gm$ in the weak inversion region, the gate–source voltage variance is obtained by referring (15) to the

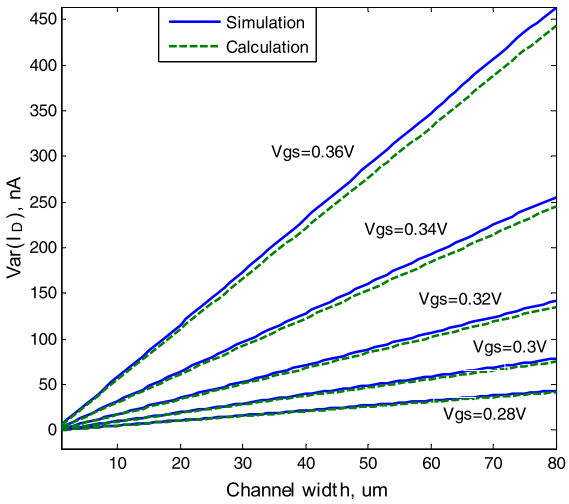

Fig. 1. Comparison between the drain-current variances calculated by hand analysis and MATLAB simulator versus channel width changes for different gate–source voltages in 0.18-μm CMOS technology.

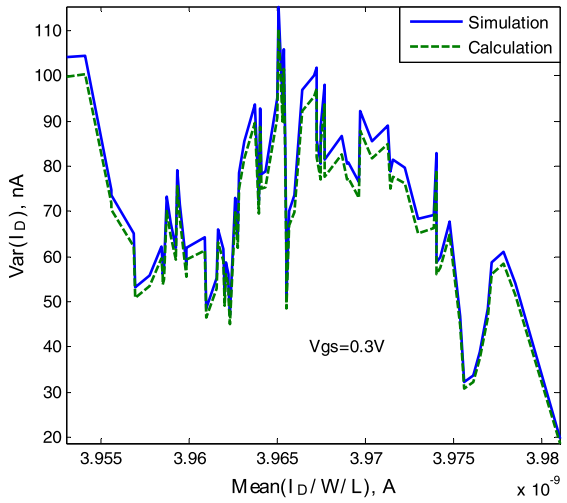

Fig. 2. Comparison between the drain-current variances calculated by hand analysis and MATLAB simulator versus the mean of normalized drain current $In = I_D/(W/L)$ for a constant gate–source voltage.

gate terminal through its transconductance gm under the small-signal conditions

$$\sigma^2(V_{GS}) = \left(\frac{I_D}{gm}\right)^2 \frac{\sigma^2(\beta)}{\beta^2} + 2\sigma^2(\beta)\frac{\sigma^2(V_T)}{\beta^2} + \sigma^2(V_T). \quad (16)$$

To evaluate the accuracy of (15) and (16), MATLAB simulator is used. By considering $n = 1.3$, $V_T = 0.5$ V, and $U_T = 26$ mV for all equations in a 0.18-μm complementary metal–oxide–semiconductor (CMOS) technology, Fig. 1 shows the comparison between the drain-current variances calculated by hand analysis expressed as (15) and what MATLAB simulates from (2). In this case, V_T and channel width W have about 50-mV and 50-nm random changes, respectively, while W variation directly affects on β. In order to have a sense of comparison between two drain-current variances, the channel width of MOS device is swept from 0.18 to 80 μm for different gate–source voltages (from 0.28 to 0.36 V). It is obvious that there is just a constant difference equals 4% between calculation and simulation results, which can be easily removed by considering an additional factor as offset term.

In addition, Fig. 2 shows the drain-current variances of calculation and simulation results versus the mean of normalized drain current

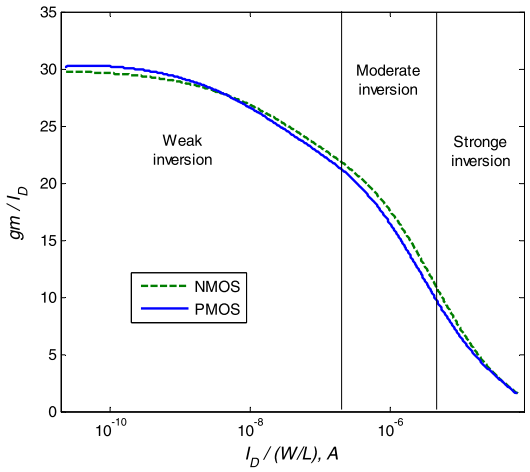

Fig. 3. Simulated gm/I_D characteristic versus normalized drain current $In = I_D/(W/L)$ in 0.18-μm CMOS technology for gate–source voltage variations from 0.1 to 1.3 V.

$In = I_D/(W/L)$ while $V_{GS} = 0.3$ V, and V_T and β have the above-mentioned changes. Fig. 2 also shows a more accurate comparison where it can be seen that the drain-current variance calculated by hand analysis follows exactly the results of MATLAB simulator. It is concluded from Figs. 1 and 2 that the constant difference between the calculation and simulation results is because of the dropped higher order terms of the Taylor expansion during the simplification of hand analyses.

Considering (16) and the drain-current variance in the strong inversion presented in [7], it can be seen that the drain-current variance in the weak inversion has an additional term compared to the strong inversion that is because of the exponential dependence of this region on the threshold voltage. Nonetheless, two terms of (16) have low impact on the drain-current variance and can be ignored. Fig. 3 shows the simulated gm/I_D characteristic curves for both nMOS- and pMOS-type transistors in 0.18-μm CMOS technology versus $In = I_D/(W/L)$ for gate–source voltage variations from 0.1 to 1.3 V. Since the highest rate of gm/I_D is achieved in the weak inversion and analog circuit designers try to maximize it for better mixed-mode circuit performance [14], the effect of the first term of (16) can be diminished. In addition, the threshold-voltage variance in the second term of (16) is multiplied by a small amount and can be eliminated compared to the third term. These simplifications can be also confirmed by MATLAB simulator. Therefore, based on (3) and its explanations, (16) can approximated as

$$\sigma^2(V_{GS}) \cong \sigma^2(V_T) = A_{V_T}^2 \Big/ WL. \quad (17)$$

Here, A_{V_T} is the area proportionality constant for the threshold voltage V_T, which is provided by process characterization. Equation (17) can be used to express the input offset variance of each circuit in the weak inversion region.

III. Input Offset Estimation of an Amplifier

Fig. 4 shows a conventional folded-cascode (FC) transconductance amplifier. Based on explanations presented in [12], transistors M5–M8 have not a significant contribution in the small-signal transconductance of the amplifier. Therefore, the drain-current variance of these transistors referred to the input can be ignored. In addition, the input offset variance is expressed as the sum of all device drain-current variances seen at the output, and then referred to the input through the amplifier's transconductance gm [12]. The results

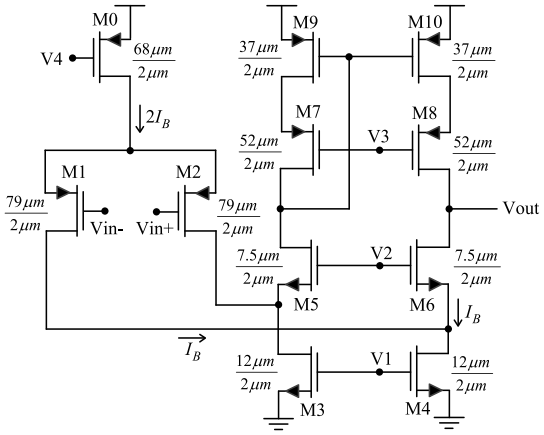

Fig. 4. Conventional FC transconductance amplifier.

for half-circuit topology of Fig. 4 is given by

$$\sigma^2(V_{\rm OS}) = \sigma^2(V_{\rm GS1}) + \left(\frac{gm_3}{gm_1}\right)^2 \sigma^2(V_{\rm GS3}) + \left(\frac{gm_9}{gm_1}\right)^2 \sigma^2(V_{\rm GS9}) \tag{18}$$

where gm_i denotes the small-signal transconductance values of the corresponding transistors. In order to estimate an accurate input offset of the FC amplifier, general equation presented as (16) is used. Note that $gm = I_{\rm D}/nU_{\rm T}$, and considering $I_{\rm D3} = 2I_{\rm D1} = 2I_{\rm D9}$, (18) can be rewritten as

$$\begin{aligned}\sigma^2(V_{\rm OS}) &= \left(\sigma^2(V_{\rm T1}) + 4\frac{n_1^2}{n_3^2}\sigma^2(V_{\rm T3}) + \frac{n_1^2}{n_9^2}\sigma^2(V_{\rm T9})\right) \\ &\quad + \left(\frac{I_{\rm D1}}{gm_1}\right)^2\left(\frac{\sigma^2(\beta_1)}{\beta_1^2} + 4\frac{\sigma^2(\beta_3)}{\beta_3^2} + \frac{\sigma^2(\beta_9)}{\beta_9^2}\right) \\ &\quad + 2\left(\begin{array}{l}\sigma^2(\beta_1)\dfrac{\sigma^2(V_{\rm T1})}{\beta_1^2} + 4\dfrac{n_1^2}{n_3^2}\sigma^2(\beta_3)\dfrac{\sigma^2(V_{\rm T3})}{\beta_3^2} + \\ \dfrac{n_1^2}{n_9^2}\sigma^2(\beta_9)\dfrac{\sigma^2(V_{\rm T9})}{\beta_9^2}\end{array}\right).\end{aligned} \tag{19}$$

By replacing (17) and $\beta = \mu {\rm C_{ox}} W/L$ in (19) and doing some simplifications, the input offset variance of FC amplifier is given by

$$\begin{aligned}\sigma^2(V_{\rm OS}) &= \left(\frac{A_{V_{\rm T1}}^2}{W_1L_1} + 4\frac{n_1^2}{n_3^2}\frac{A_{V_{\rm T3}}^2}{W_3L_3} + \frac{n_1^2}{n_9^2}\frac{A_{V_{\rm T9}}^2}{W_9L_9}\right) + \left(\frac{I_{\rm D1}A_{\beta_1}}{gm_1\mu_{\rm p}C_{ox}}\right)^2 \\ &\quad \times\left(\frac{L_1}{W_1^3} + 4\left(\frac{\mu_{\rm p}A_{\beta_3}}{\mu_nA_{\beta_1}}\right)^2\frac{L_3}{W_3^3} + \left(\frac{A_{\beta_9}}{A_{\beta_1}}\right)^2\frac{L_9}{W_9^3}\right) \\ &\quad + 2\left(\frac{A_{\beta_1}A_{V_{\rm T1}}}{\mu_{\rm p}C_{ox}}\right)^2\left(\begin{array}{l}\dfrac{1}{W_1^4} + 4\left(\dfrac{n_1\mu_{\rm p}A_{\beta_3}A_{V_{\rm T3}}}{n_3\mu_nA_{\beta_1}A_{V_{\rm T1}}}\right)^2\dfrac{1}{W_3^4} \\ + \left(\dfrac{n_1A_{\beta_9}A_{V_{\rm T9}}}{n_9A_{\beta_1}A_{V_{\rm T1}}}\right)^2\dfrac{1}{W_9^4}\end{array}\right).\end{aligned} \tag{20}$$

Here, A_β is the area proportionality constant for the current factor, β. Equation (20) helps designers to see the contribution of all device parameters in the input referred offset and the best values of β and $gm/I_{\rm D}$ can be chosen to have the minimum input offset in the weak inversion circuits. As was presented in [14] and [16], increasing the $gm/I_{\rm D}$ ratio of transistors M1 and M2 will improve the dc gain and the gain bandwidth of the FC amplifier, while it is clear from the second term of (20) that it also decreases the input offset by a power of 2.

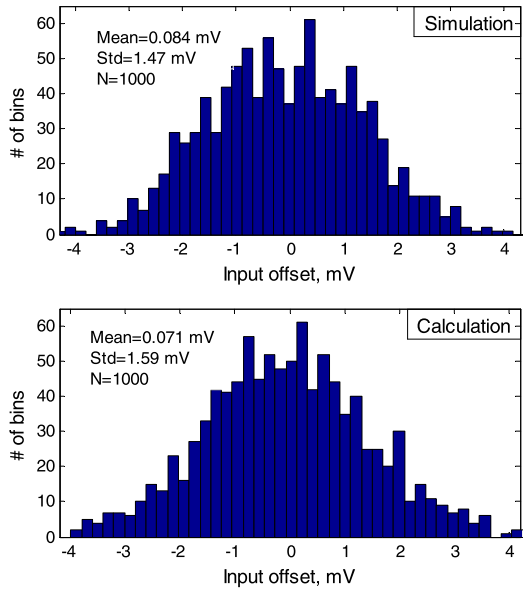

Fig. 5. Input offset distributions resulted by SPICE simulator and calculation.

In addition, all terms of (20) show that the increase of the transistor sizes results lower input offset. In addition, the second and third terms are significantly influenced by the channel width W of transistors M1, M3, and M9, and increasing their W will decrease the input offset regarding to these terms, respectively. Besides, increasing the size of transistors M9 and M10 may limit the frequency response and the slew rate of the amplifier because of enlarging the parasitic capacitors in their gate terminals.

In order to confirm the accuracy of the estimated input offset, the FC amplifier shown in Fig. 4 was designed and simulated in a 0.18-μm CMOS technology under a 0.6-V supply with 200-nA current consumption ($I_{\rm B}$ = 50 nA). The amplifier has a 56-dB dc gain, 77.5-kHz gain bandwidth, and 83° phase margin, while drives a capacitive load of 2 pF. The gate–source voltages of all transistors have been chosen equal 0.3 V to make sure they operate in the weak inversion region based on EKV model considered in [17]. Simulation results show that this value of the gate–source voltage is the best choice in 0.18-μm CMOS technology to have a high matching between (2) and operation of the transistors. In addition, to decrease the input referred flicker noise and increase the dc gain of analog circuits especially amplifiers that operate in the weak inversion region, designers usually increase the size of transistors (both W and L) so over 1 μm. Therefore, it also leads to higher matching between (2) and operation of the transistors in simulation results, because the validity of (2) is greater for a long-channel MOS transistor.

Monte-Carlo analysis of 1000 runs has been done to consider the input offset of the amplifier and compare the results of SPICE simulator and hand analysis. By extracting n, μ, $C_{\rm ox}$, $A_{\rm VT}$, and A_β from technology model [6], [7], [15], [16], and replacing in (20), Monte-Carlo analysis can be also done for (20). The results are summarized in Fig. 5, while the offset standard deviation is similar for both simulation and calculation. This consideration can be applied on most of integrated circuits especially analog cases. In addition to the FC amplifier, a current mirror amplifier has been also considered and its results showed a good matching.

IV. Conclusion

Based on the drain-current relationship in the weak inversion region, an accurate hand analysis is presented in order to calculate

the current mismatch of a MOS device. The calculated drain-current variance is useful to estimate the input offset of ultralow-power integrated circuits, which operate in the weak inversion region. Simulation results show a high matching between two drain-current variances that are calculated by hand analysis and MATLAB simulator.

REFERENCES

[1] M. Alioto, "Understanding DC behavior of subthreshold CMOS logic through closed-form analysis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 7, pp. 1597–1607, Jul. 2012.

[2] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1609–1617, Jun. 2014.

[3] M. Akbari and O. Hashemipour, "Enhancing transconductance of ultra-low-power two-stage folded cascode OTA," *Electron. Lett.*, vol. 50, no. 21, pp. 1514–1516, Oct. 2014.

[4] F. Forti and M. E. Wright, "Measurement of MOS current mismatch in the weak inversion region," *IEEE J. Solid-State Circuits*, vol. 29, no. 2, pp. 138–142, Feb. 1994.

[5] J. B. Shyu, G. C. Temes, and F. Krummenacher, "Random error effects in matched MOS capacitors and current sources," *IEEE J. Solid-State Circuits*, vol. SSC-19, no. 6, pp. 948–956, Dec. 1984.

[6] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterisation and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SSC-21, no. 6, pp. 1057–1066, Dec. 1986.

[7] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[8] J. Bastos *et al.*, "Mismatch characterization of small size MOS transistors," in *Proc. Int. Conf. Microelectron. Test Struct. (ICMTS)*, Mar. 1995, pp. 271–276.

[9] J. A. Croon, M. Rosmeulen, S. Decoutere, W. Sansen, and H. E. Maes, "An easy-to-use mismatch model for the MOS transistor," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1056–1064, Aug. 2002.

[10] P. G. Drennan and C. C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 450–456, Mar. 2003.

[11] J. Bastos, M. Steyaert, A. Pergoot, and W. Sansen, "Mismatch characterization of submicron MOS transistors," *Analog Integr. Circuits Signal Process.*, vol. 12, no. 2, pp. 95–106, 1997.

[12] R. S. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2535–2542, Sep. 2009.

[13] A. Papoulis and S. U. Pillai, *Probability, Random Variables, and Stochastic Processes*. New York, NY, USA: McGraw-Hill, 2002.

[14] J. Ou and P. M. Ferreira, "A g_m/I_D-based noise optimization for CMOS folded-cascode operational amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 10, pp. 783–787, Oct. 2014.

[15] T. Mizuno, J.-I. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216–2221, Nov. 1994.

[16] M. Akbari, M. Shokouhifar, O. Hashemipour, A. Jalali, and A. Hassanzadeh, "Systematic design of analog integrated circuits using ant colony algorithm based on noise optimization," *Analog Integr. Circuits Signal Process.*, vol. 86, no. 2, pp. 327–339, 2016.

[17] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, 1995.