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A Low-Power and High-Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull-Up Network

Saideh Kabirpour and Mohsen Jalali[1]

Abstract— **In this brief, a fast and very low power voltage level shifter (LS) is presented. By using a new regulated cross-coupled (RCC) pull-up network, the switching speed is boosted and the dynamic power consumption is highly reduced. The proposed (LS) has the ability to convert input signals with voltage levels much lower than the threshold voltage of a MOS device to higher nominal supply voltage levels. The presented LS occupies a small silicon area owing to its very low number of elements and is ultra-low-power, making it suitable for low-power applications such as implantable medical devices and wireless sensor networks. Results of the post-layout simulation in a standard 0.18-µm CMOS technology show that the proposed circuit can convert up input voltage levels as low as 80 mV. The power dissipation and propagation delay of the proposed level shifter for a low/high supply voltages of 0.4/1.8 V and input frequency of 1 MHz are 123.1 nW and 23.7 ns, respectively.**

Index Terms— **Dual-supply, level shifter, differential cascade voltage switch (DCVS), subthreshold circuit, low-power.**

I. Introduction

POWER efficient digital and mixed-mode circuits and systems take benefits from supply scaling to reduce the short circuit current and the circuit's dynamic power. However, scaling down the supply voltage reduces circuit speed and the efficiency of analog circuits. Consequently, in applications requiring different blocks at different speeds two or more power supply voltages are utilized [1, 2]. This type of design is more common in medium speed systems and applications such as wireless sensor networks, miniature healthcare devices and environmental monitoring systems [3].

In systems operating with two or more different supply voltages interconnection between sub-blocks requires voltage level shifting of the signals. The voltage level shifters (LS) must have the ability to convert low logic levels, even subthreshold voltage levels, to higher and acceptable voltage levels for the next block. Since there might be a need for a large number of LSs in a system, power consumption and propagation delay as well as silicon area are the main concerns in the design of LSs. Hence, in this brief, a fast and power-efficient voltage level shifter is proposed, which is able to convert extremely low values of the input voltages to nominal supply voltage levels. The rest of the brief is as follows: in Section II conventional LS circuits including recent high-performance ones are reviewed. Section III describes how the proposed architecture works. In Section IV, simulation results are presented. In the end, conclusions are provided in Section V.

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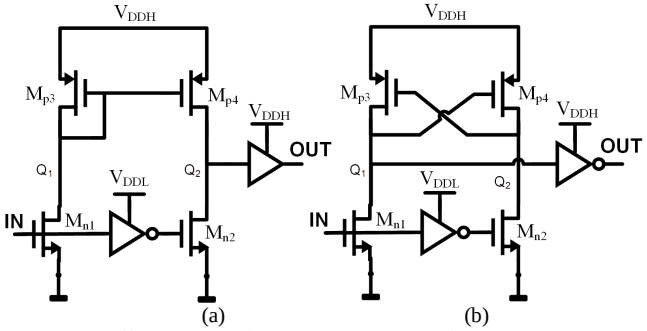

Fig. 1. Two different types of conventional level shifters; (a) current mirror (CM) based architecture, (b) differential cascode voltage switch (DCVS) architecture.

II. Literature Review

Two different types of conventional level shifters are shown in Fig. 1 where Fig. 1(a) shows type I level shifter that employs a basic current mirror (CM) as pull-up network. In this type of architecture, there is almost no regenerative interaction between pulling down and up networks as well as left and right branches of the circuit. Thereby, the operation speed is low. Furthermore, it has a relatively large standby power, which is mainly due to the static current flowing through one of the circuit branches depending on the input state. As shown in Fig. 1(b), the differential cascode voltage switch (DCVS) architecture is based on a cross-coupled pull-up network so that the regenerative process intensifies the Q_1 and Q_2 difference to switch faster. During the input rising edge, M_{n1} turns on and M_{n2} turns off. In this time, M_{n1} tries to pull the voltage of Q_1 down. As a result, M_{p4} gradually turns on pulling V_2 toward the high supply voltage (V_{DDH}) which helps to turn M_{p3} off resulting in faster discharging of Q_1. This architecture has a very low power in standby mode, as none of the both circuit branches consume static power. However, when the low supply voltage (V_{DDL}) is smaller than the nominal threshold voltage of the process, the pull-down transistors (M_{n1}, M_{n2}) are unable to easily overcome pull-up transistors (M_{p3}, M_{p4}). Thus, for boosting pull down network, we should increase the sizes of the pull-down transistors which in turn reduces the overall efficiency in terms of larger delay and power.

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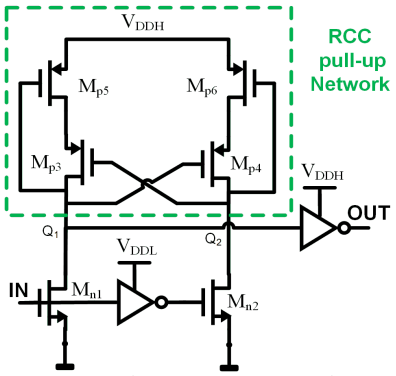

Fig. 2. Simplified schematic of the proposed level shifter.

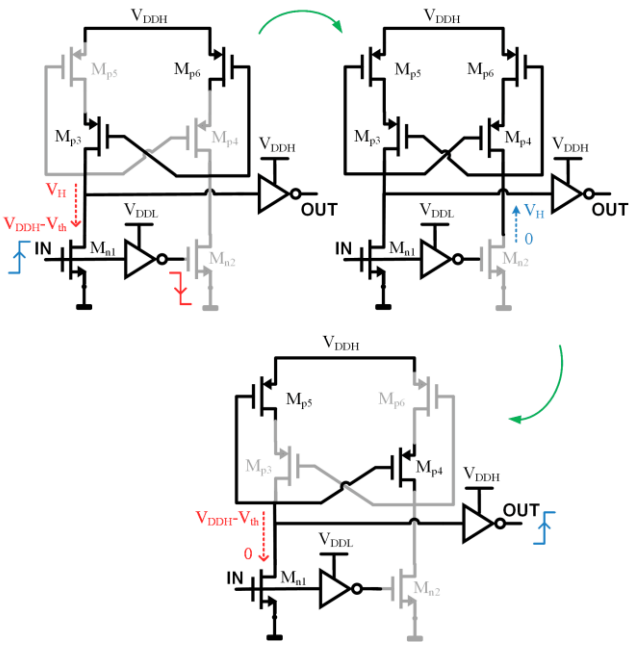

Fig. 3. Operation of the proposed LS for L→H transition.

In prior researches, different LS architectures have been introduced to overcome the constraints of the conventional LSs operating in subthreshold region. The CM-based architecture are used in [4-9]. The topology presented in [4], tries to reduce low-to-high transition delay using a level-shifting capacitor frequently charged to V_{DDH} and V_{DDL} differences. In the circuit presented in [5], when pulling down the output node, the current of the pull-up device is reduced while the pull-down device is strengthened using an auxiliary circuit, resulting in higher conversion speed. The suggested LS in [6] is a hybrid structure that contains generic CMOS logic gates and the modified Wilson current mirror to increase the voltage conversion range. The circuits presented in [7, 9] utilize a self-controlled current limiter to reduce static power. The architecture in [8] uses a two-stage conventional comparator to generate the output levels. The topologies presented in [10- 14] are based on DCVS architecture. In [10] and [13], it has been tried to decrease the strength of the pull-up device by limiting their currents. A self-adapting pull-up network and a split-input inverting buffer are utilized in [11] for increasing the switching speed and reducing the dynamic energy consumption. The [12] and [14], take gain of multi-threshold CMOS technique with three different threshold voltages to optimize the circuit delay.

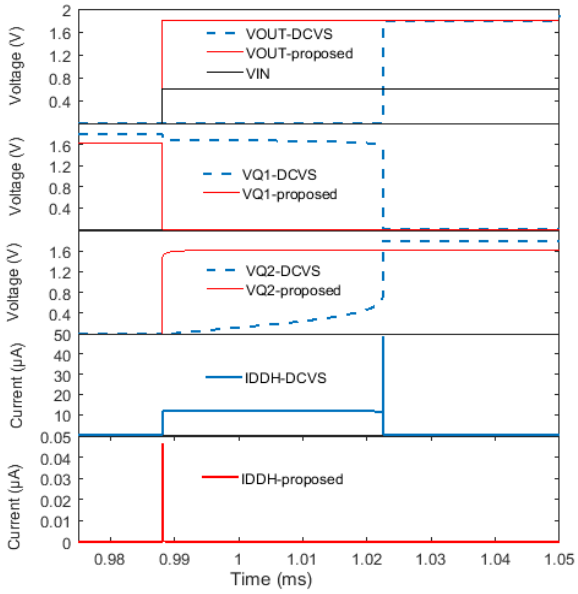

Fig. 4. Transient waveforms of the conventional DCVS and the proposed LS with RCC pull-up network assuming a rising edge at input (V_{DDL}=0.6 V and V_{DDH}=1.8 V).

III. Proposed Level Shifter

The schematic of the proposed level shifter is shown in Fig. 2. Our design is a modified DCVS structure, which includes a new regulated cross-coupled (RCC) pair for pull-up part. The proposed technique regulates the strength of the pull-up network and reduces the charge or discharge time of the critical internal nodes, which consequently increases the switching speed and reduces the dynamic power dissipation. For a better understanding of the proposed LS, the operation of the circuit for a low-to-high transition is shown in Fig. 3, in three steps. At the initial moment, the voltage of the node Q_1 is high at V_H (which is normally less than V_{DDH}) whereas the voltage of Q_2 is low. Hence, the M_{p3} and M_{p6} are on and the M_{p4} and M_{p5} are off. At first step, a low-to-high input transition causes M_{n1} to switch on and M_{n2} to switch off. So, the parasitic capacitors in the Q_1 node begin to discharge and since the pull-up current through M_{p3} is quite low by M_{p5}, node Q_1 is discharged very fast. This condition continues until Q_1 reaches approximately to V_{DDH}–V_{th} where M_{p4} and M_{p5} begin to turn on. Thus, at second step, as M_{p4} turns on, Q_2 voltage starts to increase and causes M_{p3} and M_{p6} to turn off gradually. In this step, the regenerative process of the pull-up network is enabled and makes the voltage of Q_2 to increase very fast. Obviously, M_{p6} is turned off before Q_2 reaches V_{DDH} and thus Q_2 stays at V_H. Thus, the maximum voltage level in the intermediate nodes (Q_1 and Q_2) is always less than V_{DDH}, which helps reduce dynamic power. It is worth noting that the transistors in the pull-up network never turn off completely always entering deep subthreshold region as their gate-source voltage acquires the difference of V_{DDH} and V_H. This fact helps the transistors in the pull-up network to change state more quickly further increasing the circuit speed.

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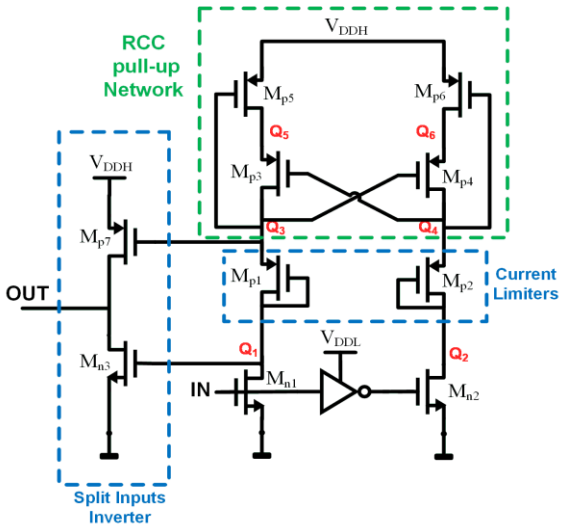

Fig. 5. Schematic of the complete proposed level shifter.

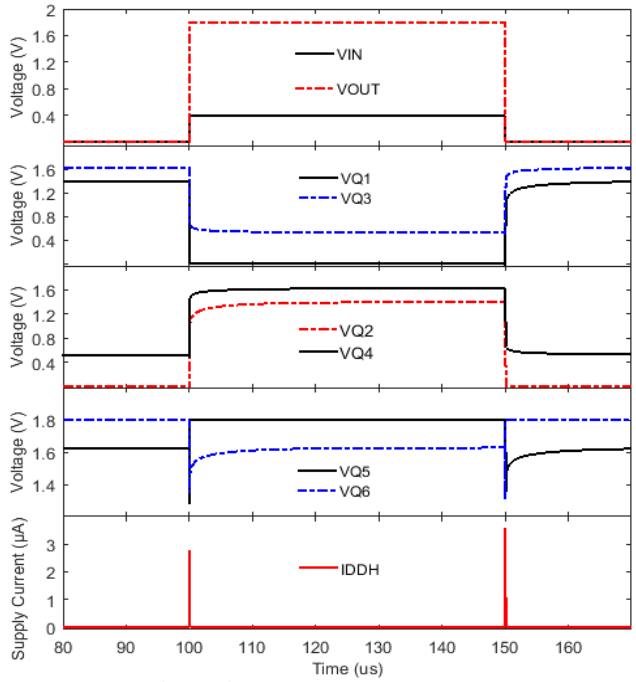

Fig. 6. Transient waveforms of the proposed LS.

At third step, when M_{p3} turns off, M_{n1} would be capable of lowering the voltage of node Q_1, even for input voltages below its threshold voltage. By turning off M_{p3} and M_{p6}, in the end, no static current flows through the left and right branches. Thus the result of RCC pull-up part in the proposed LS is that the power dissipation and transition times are significantly reduced. Similarly, when the input signal switches from high to low, the operating states of the circuit are reversed.

Fig. 4. compares transient waveforms of the conventional DCVS and the proposed LS assuming a rising edge at input with voltage levels of 0.6 V and 1.8 V for V_{DDL} and V_{DDH}, respectively (The V_{DDL} is chosen higher than V_{th} because the conventional circuit cannot operate well at subthreshold voltage levels). The corresponding transistor sizes in both designs are the same and are set to the smallest possible values. As can be observed, the proposed RCC pull-up network makes the proposed LS circuit to operate much faster

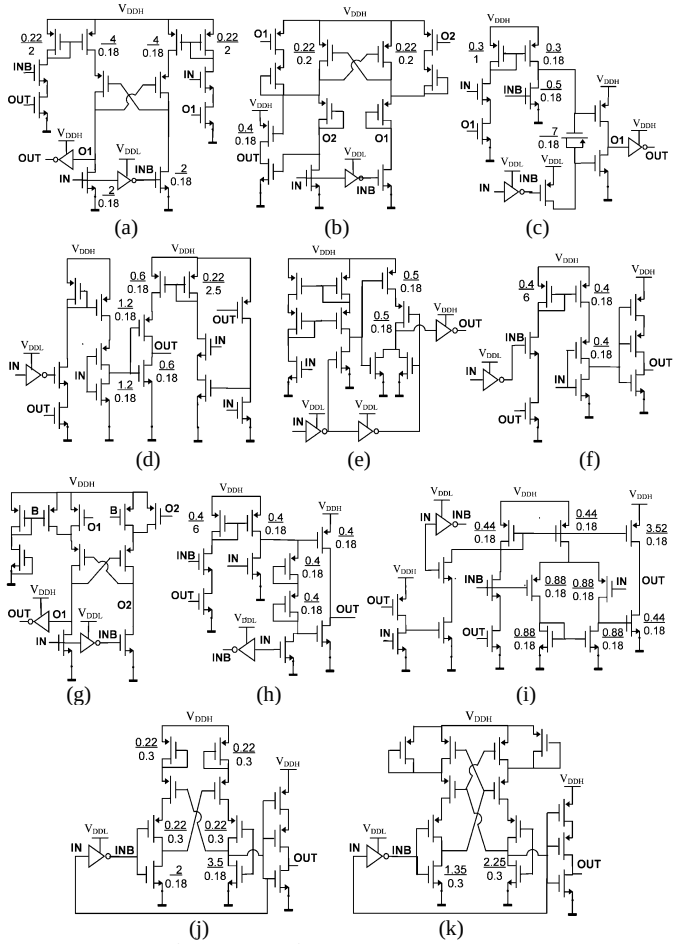

Fig. 7. Schematic of the level shifters presented in (a) [10], (b) [11], (c) [4], (d) [5], (e) [6], (f) [9], (g) [13], (h) [7], (i) [8], (j) [14] and (k) [12]. The transistors are mainly minimum sized except for those explicitly indicated.

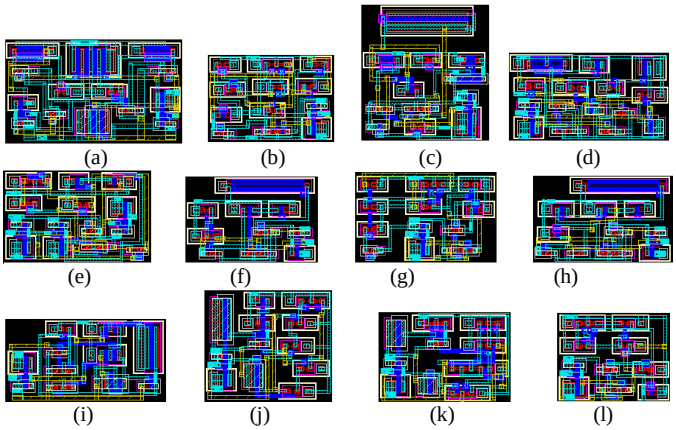

Fig. 8. Layout of the level shifters presented in (a) 14.9μm×8.4μm [10], (b) 10.5μm×7.1μm [11], (c) 11.7μm×11.3μm [4], (d) 13.4μm×7.1μm [5], (e) 12μm×7.5μm [6], (f) 10.9μm×7μm [9], (g) 11.6μm×7.4 [13], (h)11.5μm×7μm [7], (i) 13.2μm×6.6μm [8] , (j) 10.5μm×8.8μm [14] (k) 11μm×7.4μm [12] and (l) the proposed level shifter (Fig. 5) 9μm×7μm.

than the conventional circuit. In addition, the drawn current from the supply (i.e. V_{DDH}) is noticeably lower than the conventional one.

The complete schematic circuit of the proposed LS is depicted in Fig. 5. The transient waveforms at supply voltage levels of 0.4 V and 1.8 V for V_{DDL} and V_{DDH}, respectively, are shown in Fig. 6. In order to further reduce the power

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TABLE I
TRANSISTOR SIZES

Transistor	W/L (μm)	Transistor	W/L (μm)
M_{n1}, M_{n2}, M_{n3}, M_{p1}, M_{p2}, M_{p3}, M_{p4}, M_{p5}, M_{p6}	0.22/0.18	M_{p7}	0.4/0.18

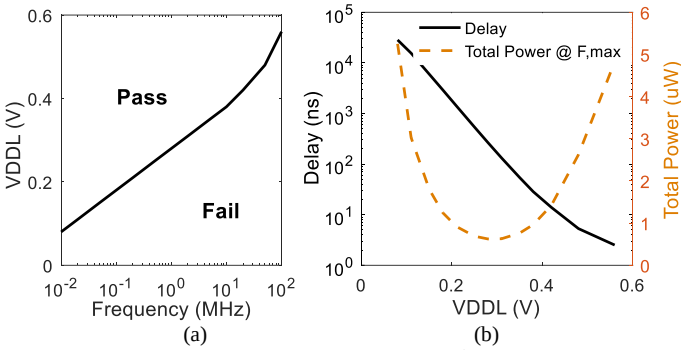

Fig. 9. (a) The minimum operating V_{DDL} versus input frequency and; (b) the delay and power consumption as functions of the minimum operating V_{DDL}.

consumption, two p-MOS diodes are used in series with pull-down network [8]. In addition, a split-inputs inverter is utilized to reduce the short circuit current during transitions in the output inverter [8]. The pMOS diodes (M_{p1} and M_{p2}) set the low voltage level in nodes Q_3 and Q_4 at a voltage higher than zero. The voltage difference between Q_1 and Q_3 nodes prevents the pull-up and the pull-down transistors in the output inverter (M_{n3} and M_{p7}), from turning on at the same time, thereby limiting the short-circuit current and thus reducing the power consumption of the circuit. In addition, as mentioned in Section II, in subthreshold LS circuits where the V_{DDL} is less than the nominal threshold voltage of the devices, the pull-down transistors should be upsized compared to pull-up transistors to make enable level conversion from subthreshold to above threshold. In the proposed RCC pull-up network, the transistors M_{P5} and M_{P6} (please refer to Fig. 5) regulate and reduce the strength of the main pull-up devices (i.e. M_{P3} and M_{P4}). As a result, choosing the size of the pull-down network is greatly relaxed compared with the previous works with DCVS based configuration. So, to reduce the size of internal capacitors, which can decrease power delay product (PDP), the sizes of the most transistors are chosen minimum. The transistor sizes are reported in Table I.

IV. SIMULATION RESULTS

In order to verify fairly the performance of the proposed LS, the proposed structure (Fig. 5), as well as some of the prior work, are simulated in a standard 0.18-μm CMOS technology. The schematic of all other structures and the size of their transistors are shown in Fig. 7. The proposed structure has the lowest number of elements. Fig. 8 presents the layout of all level shifters. The area occupied by the proposed design is 63μm^2, which is the smallest among all designs mainly owing to relatively lower number of transistors. It should be noted that all the following results are obtained from the post-layout simulation in presence of an inverter as the load circuit to all the circuits. Fig. 9(a) shows the minimum possible V_{DDL} of the proposed circuit for different input frequencies assuming a

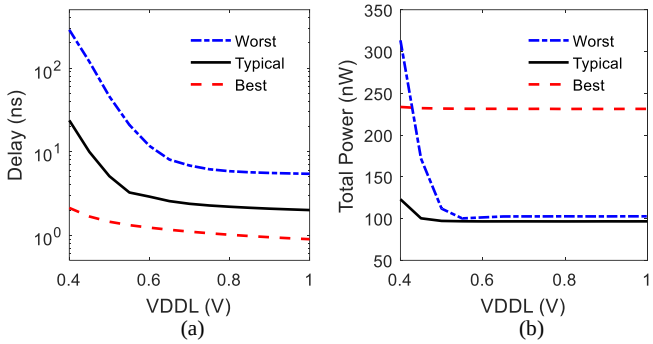

Fig. 10. (a) Delay and (b) power characteristics of the proposed level shifter (Fig. 5) versus V_{DDL} for V_{DDH} = 1.8 V and an input frequency of 1 MHz evaluated for the best, typical and the worst conditions regarding to PVT variations.

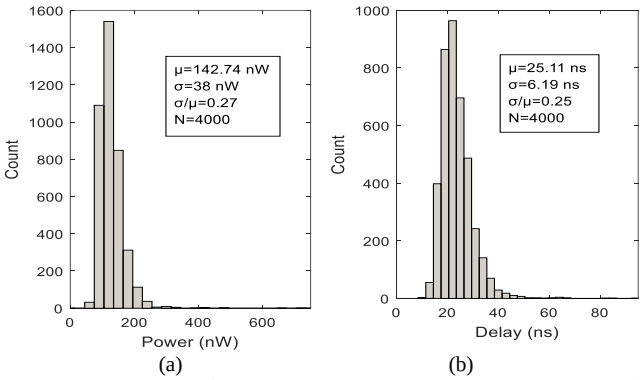

Fig. 11. Distribution of the (a) power and (b) delay characteristics of the proposed LS (Fig. 5).

typical corner that includes typical transistors, a temperature of 27°C and V_{DDH}=1.8 V. It can be seen that by increasing the V_{DDL}, the maximum operating frequency (F_{max}) of the circuit increases. The minimum value of V_{DDL} is 80mV which the LS operates at 10 kHz. The power consumption at F_{max} and the delay are reported for each minimum possible V_{DDL} in Fig. 9(b).

The impact of the PVT variations on the propagation delay and the total power dissipation of the circuit for various values of the V_{DDL} at an input frequency of 1 MHz are shown in Fig. 10(a) and (b), respectively. A fast nMOS and a fast pMOS result in the least delay. In addition, a decreased V_{DDH} improves this condition. Finally, a high temperature increases the subthreshold device currents. Thus, in view of propagation delay, fast nMOS, fast pMOS, −10% V_{DDH}, and a temperature of 125 °C is the best corner. Contrarily, slow nMOS, slow pMOS, +10% V_{DDH}, and a temperature of 0 °C lead to the worst corner.

To evaluate the proposed LS performance against device and process mismatches, a Monte Carlo simulation of 4000 points is carried out for a high supply voltage of V_{DDH}=1.8 V, a low supply voltage of V_{DDL} = 0.4 and input frequency of 1MHz, The results are shown in Fig. 11 where the normalized standard deviation values (σ /μ) of the dissipated power and the propagation delay are 0.27 and 0.25, respectively.

To compare the proposed LS performance with other works, Fig. 12(a) and (b) shows the results of the propagation delay and total power dissipation of the proposed LS and the LSs presented in [4], [5], [7] and [11-13] for different V_{DDL}

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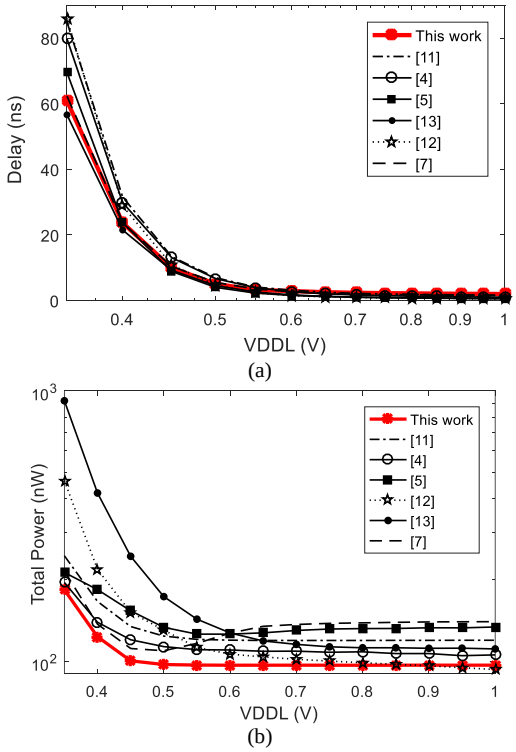

Fig. 12. Simulated (a) propagation delays and (b) total power consumption of the level shifter structures as a function of V_{DDL} at V_{DDH} = 1.8 V and frequency of 1 MHz.

values. All designs are simulated in the same conditions (typical corner, 27°C) for an input frequency of 1 MHz and the V_{DDH} =1.8 V. The proposed LS exhibits remarkable performance in terms of power consumption. Regarding the propagation delay, the proposed design is one of the lowest when V_{DDL} is in the subthreshold range. Table II presents a performance summary of the proposed structure and compares it with other designs. In this table, P_s denotes static power and P_t stands for total power. For a better comparison, power-delay product (PDP) can be used as a figure of merit. Obviously, the proposed design has the lowest PDP and lowest area while converting up very low voltage levels.

TABLE II
COMPARISON WITH PREVIOUS WORK (V_{DDH}=1.8 V, F=1 MHz)

		V_{DDL} =0.4 V				
Ref.	Min. V_{DDL}	Delay (ns)	P_s (nW)	P_t (nW)	PDP* (nW.ns)	Area (μm^2)
Fig. 5	0.28	23.69	0.3	123.1	2916	63
[10]	0.31	31.29	0.23	326.7	10222	125.16
[11]	0.28	31.54	0.27	166.3	5245	74.55
[4]	0.29	29.85	0.06	139.3	4158	132.2
[5]	0.28	23.75	1	183.9	4368	95.1
[6]	0.3	29.59	0.78	631.4	18683	90
[12]	0.3	28.83	0.23	218.3	6293	81.4
[13]	0.27	21.49	0.26	418.7	8998	85.84
[7]	0.29	25.23	1.76	137	3456	80.5
[8]	0.28	22.32	0.5	347	7745	87.12
[14]	0.38	41.12	0.13	228.1	9379	92.4
[9]	0.28	24.31	1.06	150	3646	76.3

* PDP:Power-Delay Product, PDP=P_t (nW)×Delay (ns).

V. CONCLUSION

We have implemented a power, delay, and area efficient level shifter based on a novel regulated cross-coupled pull-up network. The proposed LS up-converts signals from the deep subthreshold regime to the high and nominal supply voltages. Post-layout simulation results of the proposed LS and prior work using a 0.18-µm CMOS technology, indicate the efficiency of the proposed regulated cross-coupled pull-up network. The results show that the proposed circuit can convert up the input signals as low as 80 mV to about 1.8 V and while having lowest area and power-delay product.

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