High-performance engineered gate transistor-based compact digital circuits

S. Kumar, S.A. Loan✉ and A.M. Alamoud

A novel method for designing and realising compact digital circuits by engineering MOSFET gate electrode is proposed. The novelty is the use of gate engineered single devices in the pull-up (PU) and pull-down (PD) paths of a static CMOS gate instead of multiple transistors as used in conventional CMOS implementations of circuits. Herein, two input NAND, NOR, and exclusive-OR (XOR) gates employing the proposed gate engineering concept are designed and simulated. Engineered gate N-type MOS and P-type MOS are used for PD and pull-up circuits, respectively. Since only two devices are used for a complete circuit: one in PU network and other in PD network; therefore, area and power of the proposed circuits get reduced significantly in comparison with the conventional static CMOS circuits. Mixed mode simulations have shown that the proposed technique realises NAND, NOR and XOR operations perfectly and it can be extended to realise other combinational and sequential circuits easily.

Introduction: The scaling of device dimensions has been used till date to improve the performance of devices. The scaling has improved the speed, power consumption, and packing density of integrated circuits. However, the further scaling of devices below 22/18 nm is extremely difficult due to severe short channel effects [1]. An alternative approach is to go for the multifunctional devices, wherein a transistor even can perform a circuit action. For example, a single transistor realising an inverter action or a transmission gate action results in significant area reduction [2, 3]. A typical two input static CMOS NAND/NOR gate needs four transistors and an exclusive-OR (XOR)/XNOR gate needs eight transistors for their realisations using the conventional static CMOS technology. Various design techniques are available to reduce the transistor count of logic gates such as ratioed logic, pseudo-N-type MOS (NMOS), transmission gate-based logic, differential cascade voltage switch logic, dynamic gates [4] etc. Most of these techniques need either *n*-logic or *p*-logic blocks for evaluation of inputs wherein *p*-logic and *n*-logic blocks are same as used in the static CMOS-based gates. Sordan *et al.* [5] designed logic gates with a single graphene transistor. Although this structure designs a two input NAND, XOR, and OR logic gates with a single transistor but it needs an input stage to ensure that applied gate voltage is average of two input voltages. This input stage leads to an extra area in the design of the circuit. In addition to that the operating voltage of 50 V is used, which is significantly large than the operating voltage of currently used sub-micron technology. Xu *et al.* [6] also uses similar concept to design logic gates with single molecular FETs, except the operating voltage is in smaller ranging from −2 to 2 V. Furthermore, XOR/XNOR gates can be designed with four transistors only [7, 8].

The prior art does not come across any device design method that uses gate electrode engineering to implement a complete static CMOS logic gate. In this work, we propose, for the first time, a novel method for designing and realising logic circuits employing engineered gate transistors. Our proposed method uses engineered gate transistors to implement digital circuits with two transistors only. One engineered gate transistor is used to implement the complete pull-down network (PDN), whereas the other one is used to realise the complete pull-up network (PUN) of the CMOS logic gate. It is similar to static CMOS type logic gates, except each PDN and PUN employ single engineered gate device. The use of single devices in the PD and pull paths has resulted in a significant reduction in area and space requirement. The proposed technique has resulted in a significant enhancement in the performance of the digital circuits, as transistor count requirement and power consumption has got significantly reduced. The proposed technique has been used to realise two input NAND, NOR, and XOR gates in this work.

A 2D calibrated simulation of the proposed and conventional gates are performed using Silvaco Atlas simulator. Model calibration has been performed for NMOS with the experimental data as reported by Horstmann *et al.* [9] and for P-type MOS (PMOS) with the experimental data as reported by Chau *et al.* [10]. A good agreement has been observed between the simulated and the experimental data, as shown in Fig. 1. The extracted values out of model calibration are used in simulating all the devices. The values of various models used include bandgap narrowing parameter (BGN.E) of 6.5×10^{-3}, carrier life time of 1.5×10^{-7} s is used for both electrons and holes, and density of states used is 6×10^{19} and 8×10^{18} cm^{-3} for NC300 and NV300, respectively. The various other models used are Shockley–Read–Hall, field-dependent mobility (DMOB), concentration DMOB, BGN, drift diffusion, and auger.

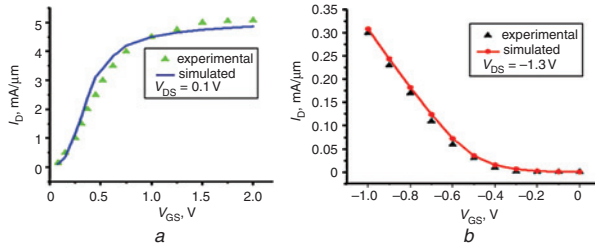

Fig. 1 *Model calibration*
a For NMOS with experimental data as reported by Horstmann *et al.* [7]
b For PMOS with experimental data as reported by Chau *et al.* [10]

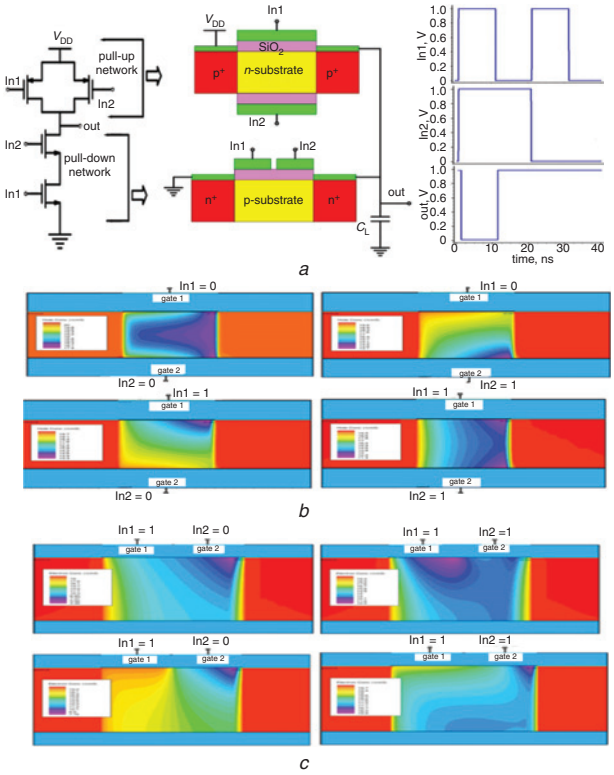

Fig. 2 *Operational mechanism of the proposed 2-input NAND gate*
a Schematic diagram of proposed gate engineered NAND gate and its transient analysis
b Hole concentration contour for PUN of NAND gate for different inputs
c Electron concentration contour for PDN of NAND gate for different inputs

Fig. 2*a* shows the schematic diagram of the proposed NAND gate employing the engineered gate transistor technique. Here, the parallel combination of two PMOS transistors in the PUN of the conventional NAND gate has been replaced by a double gate MOSFET, with inputs In1 and In2 applied to its two gates in the proposed structure. Similarly, the series combination of two NMOS transistors in the PDN of the conventional NAND gate has been replaced by a single MOSFET, with engineered gate. The PD engineered gate MOSFET has two sub-gates which actually realise the series combination of two NMOS transistors in the PDN. The transient analysis clearly shows the NAND functional of the proposed structure. For In1=In2=1, the output is '0' and for all other combinations the output is '1'. For In1=In2=1, the double gate PMOS in the PUN is in the OFF state and the engineered gate NMOS in the PDN is conducting and is in the ON state. With the result output gets grounded for this combination of inputs. For the other combinations of In1 and In2, the double gate PMOS transistor in the PUN is in ON state and the gate engineered MOSFET in the PDN is in OFF state, as no electron channel gets created in the engineered gate transistor in the PDN. With the result

output is being pulled up through the double gate PMOS transistor in the PUN to V_{DD}. Figs. 2*b* and *c* show the electron and hole concentrations profiles in the PDN and PUN of the proposed structure. It clearly shows the channel creation and channel breaking for different input combinations. For In1=In2='1', a complete electron channel is created in the gate engineered MOSFET in the PDN and the device is ON state and the output is being pulled down to ground. For this combination, there is no hole channel creation in the double gate MOSFET in the PUN and the device is in OFF state. The proposed engineered gate transistor concept has been also used to realise two input NOR and XOR gates, as shown in Fig. 3. In case of an NOR gate, the series combination of two PMOS transistors in the PUN of the conventional technology-based NOR gate has been replaced by an engineered gate PMOS transistor in the PUN and the parallel combination of NMOS transistors have been replaced by a double gate NMOS transistor in the PDN. The transient analysis clearly shows the NOR gate action in the proposed device, as shown in Fig. 3*a*.

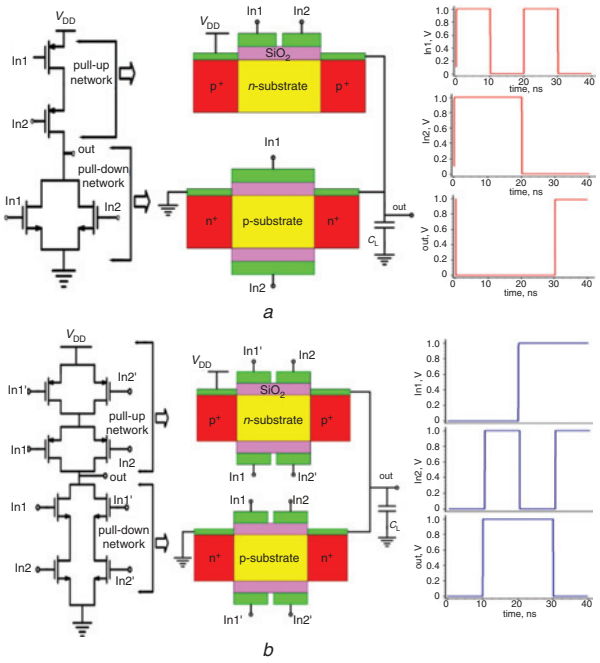

Fig. 3 *Schematic diagrams of proposed*
a NOR gate
b XOR gate along with their transient analyses

Fig. 3*b* shows the realisation of a two input XOR gate using the proposed technique, along with the transient analysis. Here, both pull-up (PUN) and PDNs are realised by gate engineered NMOS and PMOS transistors. For In1=In2='1' and In1=In2='0' combinations, engineered gate PMOS in the PUN is OFF and the engineered gate NMOS in the PDN is ON. The top channel (or bottom) of the PDN conducts and it pulls the output node down to ground. On the other hand for In1='0'; In2='1' and In1='1'; and In2='0' combinations, engineered gate PMOS in the PUN is ON, as the top and bottom channels get created for these combinations in the gate engineered gate transistor in PUN. However, for these combinations the engineered gate NMOS in the PDN is OFF, as no channel gets created in the PDN. With the result the output is being pulled up to V_{DD}. In this way, the proposed XOR gate works similar to a static XOR gate with reduced transistor counts. By interchanging input patterns of PUN and PDN of XOR gate, an XNOR function can be obtained. The mixed mode analysis of all the gates is performed with 1 ff load capacitance and 20 ps rise/fall time of inputs. On comparing the proposed gate realisation with the conventional one, it is clear that a reduced transistor count is needed to realise these gates using the proposed engineered gate technology. A comparative analysis of delay and power consumption has been performed and is shown in Table 1. The comparative analysis shows that the proposed technology results in lower power consumption but slightly higher delay. However, the power–delay product of the proposed gates is better than the conventional gates.

Table 1: Performance comparison of proposed NAND and NOR gates with conventional NAND and NOR gates (Gate length = 50 nm, source/drain doping = 1×10^{20}/cm^3, substrate doping = 10^{17}/cm^3)

Parameter	NOR gate		NAND gate	
	Conventional	Proposed	Conventional	Proposed
Transistor count	4	2	4	2
Average delay (ps)	12.5	12.75	15.5	19.5
Total power (nW)	181.25	146.25	186.75	122.5
Power–delay product (10^{-19} J)	22.65	18.64	28.94	23.88

Conclusion: We have proposed compact NAND, NOR, and XOR logic gates by engineering gate electrode of NMOS and PMOS transistors. The proposed gates required only two transistors for realising a complete logic gate function. An engineered PMOS replaces PUN and an engineered NMOS replaces PD of the static CMOS logic. The proposed logic gates achieve functions of static CMOS logic gate with significantly lesser circuit area, power consumption, and power–delay product.

Acknowledgment: The authors thank the Visiting Professor Program 'VPP' at King Saud University (KSU) for their support.

Submitted: *22 October 2016* E-first: *16 December 2016*
doi: 10.1049/el.2016.3899
One or more of the Figures in this Letter are available in colour online.

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